

DLPC2020 Display Controller

1 Features

- Display controller for DLP2020
 - Supports input image sizes up to 720p and scales to WVGA
 - Low-power DMD interface with interface training
- Input frame rates up to 120 Hz
- Pixel data processing:
 - IntelliBright™ suite of image processing algorithms
 - Content adaptive illumination control (CAIC)
 - Local area brightness boost (LABB)
 - Image resizing (scaling)
 - 1D Keystone correction
 - Color coordinate adjustment
 - Active power management processing
 - Programmable degamma
 - Color space conversion
 - 4:2:2 to 4:4:4 chroma interpolation
- 24-Bit, input pixel interface support:
 - Parallel or BT656, interface protocols
 - Pixel clock up to 155 MHz
 - Multiple input pixel data format options
- MIPI® DSI (display serial interface) Type 3:
 - 1-4 lanes, up to 470 Mbps lane speed
- External flash support
- Auto DMD parking at power down
- Embedded frame memory (eDRAM)
- System Features:
 - I²C device control
 - Programmable splash screens
 - Programmable LED current control
 - Display image rotation
 - One frame latency
- Pair with IC1000 PMIC (power management integrated circuit) and LED driver

2 Applications

- Mobile projector
- Smart display
- Smartphone
- Augmented reality glasses
- Smart home displays
- Pico projectors

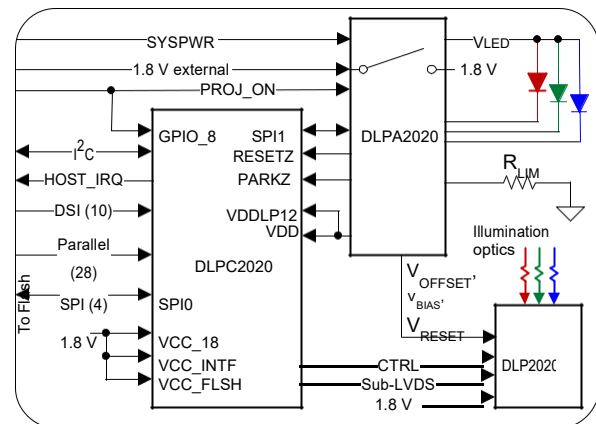
3 Description

DLPC2020 is a digital controller which enables operation of the digital micromirror devices (DMDs). The controller provides a convenient, multi-functional interface between user electronics and the DMD, enabling small form factor and low power display applications.

Device Information⁽¹⁾⁽²⁾

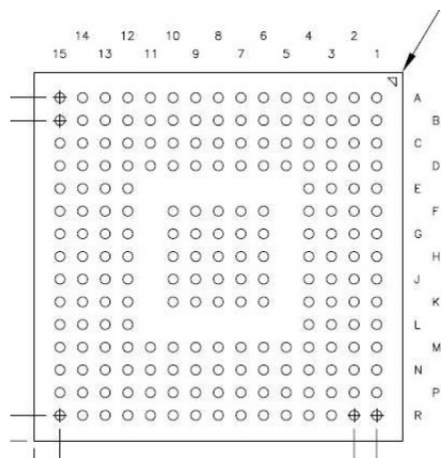
PART NUMBER	PACKAGE	BODY SIZE (NOM)
IC2000	NFBGA (201)	13.00 × 13.00 mm ²

Typical, Simplified System



4 Pin Configuration and Functions

**ZEZ Package
201-Pin NFBGA
Bottom View**



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DMD_LS_C LK	DMD_LS_W DATA	DMD_HS_W DATAH_P	DMD_HS_W DATAG_P	DMD_HS_W DATAF_P	DMD_HS_W DATAE_P	DMD_HS_CLK_P	DMD_HS_W DATAD_P	DMD_HS_W DATAC_P	DMD_HS_W DATAB_P	DMD_HS_W DATAA_P	CMP_OUT	SPI0_CLK	SPI0_CSZ0	CMP_PWM
B	DMD_DEN_ARSTZ	DMD_LS_R DATA	DMD_HS_W DATAH_N	DMD_HS_W DATAG_N	DMD_HS_W DATAF_N	DMD_HS_W DATAE_N	DMD_HS_CLK_N	DMD_HS_W DATAD_N	DMD_HS_W DATAC_N	DMD_HS_W DATAB_N	DMD_HS_W DATAA_N	SPI0_DIN	SPI0_DOUT	LED_SEL_1	LED_SEL_0
C	DD3P	DD3N	VDDL P12	VSS	VDD	VSS	VCC	VSS	VCC	HWTEST_E_N	RESETZ	SPI0_CSZ1	PARKZ	GPIO_00	GPIO_01
D	DD2P	DD2N	VDD	VCC	VDD	VSS	VDD	VSS	VDD	VSS	VCC FL SH	VDD	VDD	GPIO_02	GPIO_03
E	DCLKP	DCLKN	VDD	VSS								VCC	VSS	GPIO_04	GPIO_05
F	DD1P	DD1N	RREF	VSS		VSS	VSS	VSS	VSS	VSS		VCC	VDD	GPIO_06	GPIO_07
G	DD0P	DD0N	VSS_PLLM	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VSS	GPIO_08	GPIO_09
H	PLL_REFCLK_I	VDD_PLLM	VSS_PLLD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VDD	GPIO_10	GPIO_11
J	PLL_REFCLK_O	VDD_PLLD	VSS	VDD		VSS	VSS	VSS	VSS	VSS		VDD	VSS	GPIO_12	GPIO_13
K	PDATA_1	PDATA_0	VDD	VSS		VSS	VSS	VSS	VSS	VSS		VSS	VCC	GPIO_14	GPIO_15
L	PDATA_3	PDATA_2	VSS	VDD								VDD	VDD	GPIO_16	GPIO_17
M	PDATA_5	PDATA_4	VCC_INTF	VSS	VSS	VDD	VCC_INTF	VSS	VDD	VDD	VCC	VSS	JTAGTMS1	GPIO_18	GPIO_19
N	PDATA_7	PDATA_6	VCC_INTF	PDM_CVS_TE	HSYNC_CS	3DR	VCC_INTF	HOST_IRQ	IIC0_SDA	IIC0_SCL	JTAGTMS2	JTAGTDO2	JTAGTDO1	TSTPT_6	TSTPT_7
P	VSYNC_WE	DATEN_CM D	PCLK	PDATA_11	PDATA_13	PDATA_15	PDATA_17	PDATA_19	PDATA_21	PDATA_23	JTAGTRSTZ	JTAGTCK	JTAGTDI	TSTPT_4	TSTPT_5
R	PDATA_8	PDATA_9	PDATA_10	PDATA_12	PDATA_14	PDATA_16	PDATA_18	PDATA_20	PDATA_22	IIC1_SDA	IIC1_SCL	TSTPT_0	TSTPT_1	TSTPT_2	TSTPT_3

Note: The lower image view is from the top.

Pin Functions – DMD Reset and Bias Control

PIN		I/O	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.			
DMD_DEN_ARSTZ	B1	O	2	DMD driver enable (active high). DMD reset (active low). When corresponding I/O power is supplied, the controller drives this signal low after the DMD is parked and before power is removed from the DMD. If the 1.8-V power to the DLPC34xx is independent of the 1.8-V power to the DMD, then TI recommends including a weak, external pulldown resistor to hold the signal low in case DLPC34xx power is inactive while DMD power is applied.
DMD_LS_CLK	A1	O	3	DMD, low speed (LS) interface clock
DMD_LS_WDATA	A2	O	3	DMD, low speed (LS) serial write data
DMD_LS_RDATA	B2	I	6	DMD, low speed (LS) serial read data

(1) See Table 2 for type definitions.

Pin Functions – DMD Sub-LVDS Interface

PIN		I/O	TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.			
DMD_HS_CLK_P DMD_HS_CLK_N	A7 B7	O	4	DMD high speed (HS) interface clock
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	A3 B3 A4 B4 A5 B5 A6 B6 A8 B8 A9 B9 A10 B10 A11 B11	O	4	DMD sub-LVDS high speed (HS) interface write data lanes. The true numbering and application of the DMD_HS_WDATA pins depend on the software configuration.

(1) See Table 2 for type definitions.

Table 2. I/O Type Subscript Definition

SUBSCRIPT	I/O DESCRIPTION	SUPPLY REFERENCE	ESD STRUCTURE
1	1.8-V LVCMOS I/O buffer with 8-mA drive	V _{CC18}	ESD diode to GND and supply rail
2	1.8-V LVCMOS I/O buffer with 4-mA drive	V _{CC18}	ESD diode to GND and supply rail
3	1.8-V LVCMOS I/O buffer with 24-mA drive	V _{CC18}	ESD diode to GND and supply rail
4	1.8-V sub-LVDS output with 4-mA drive	V _{CC18}	ESD diode to GND and supply rail
5	1.8-V, 2.5-V, 3.3-V LVCMOS with 4-mA drive	V _{CC_INTF}	ESD diode to GND and supply rail
6	1.8-V LVCMOS input	V _{CC18}	ESD diode to GND and supply rail
7	1.8-V, 2.5-V, 3.3-V I ² C with 3-mA drive	V _{CC_INTF}	ESD diode to GND and supply rail
8	1.8-V I ² C with 3-mA drive	V _{CC18}	ESD diode to GND and supply rail
9	1.8-V, 2.5-V, 3.3-V LVCMOS with 8-mA drive	V _{CC_INTF}	ESD diode to GND and supply rail
10	DSI LVDS I/O	V _{DD} for high speed transmit, high speed receive, and low power receive. V _{DDL12} for low power transmit	ESD diode to GND and supply rail
11	1.8-V, 2.5-V, 3.3-V LVCMOS input	V _{CC_INTF}	ESD diode to GND and supply rail
12	1.8-V, 2.5-V, 3.3-V LVCMOS input	V _{CC_FLSH}	ESD diode to GND and supply rail
13	1.8-V, 2.5-V, 3.3-V LVCMOS with 8-mA drive	V _{CC_FLSH}	ESD diode to GND and supply rail

Pin Functions – Power and Ground

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDD	C5, D5, D7, D12, J4, J12, K3, L4, L12, M6, M9, D9, D13, F13, H13, L13, M10, D3, E3	—	PWR	Core 1.1-V power (main 1.1 V)
VDDL P12	C3	—	PWR	DSI PHY Low Power mode driver supply. It is recommended to externally tie this pin to VDD.
VSS	Common to all package types C4, D6, D8, D10, E4, E13, F4, G4, G12, H4, H12, J3, J13, K4, K12, L3, M4, M5, M8, M12, G13, C6, C8 Only available on DLPC3435 F6, F7, F8, F9, F10, G6, G7, G8, G9, G10, H6, H7, H8, H9, H10, J6, J7, J8, J9, J10, K6, K7, K8, K9, K10	—	GND	Core ground (eDRAM, DSI, I/O ground, thermal ground)
VCC18	C7, C9, D4, E12, F12, K13, M11	—	PWR	All 1.8-V I/O power: (1.8-V power supply for all I/O pins except the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ, LED_SEL, CMP_OUT, GPIO, IIC1, TSTPT, and JTAG pins)
VDD_PLLM	H2	—	PWR	MCG PLL (master clock generator phase lock loop) 1.1-V power
VSS_PLLM	G3	—	RTN	MCG PLL return
VDD_PLLD	J2	—	PWR	DCG PLL (DMD clock generator phase lock loop) 1.1-V power
VSS_PLLD	H3	—	RTN	DCG PLL return

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
SUPPLY VOLTAGE⁽²⁾				
V _(VDD)		−0.3	1.21	V
V _(VDDL12)		−0.3	1.32	V
V _(VCC18)		−0.3	1.96	V
DMD Sub-LVDS Interface (DMD_HS_CLK_x and DMD_HS_WDATA_x_y)		−0.3	1.96	V
V _(VDD_PLLM)	(MCG PLL)	−0.3	1.21	V
V _(VDD_PLLD)	(DCG PLL)	−0.3	1.21	V
GENERAL				
T _J	Operating junction temperature	−30	125	°C
T _{stg}	Storage temperature	−40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to VSS (GND).

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _(VDD)	Core power 1.1 V (main 1.1 V)	1.045	1.10	1.155	V
V _(VDDL12)	DSI PHY low power mode driver supply See (1)(2)	1.045	1.10	1.155	V
V _(VCC18)	All 1.8-V I/O power: (1.8-V power supply for all I/O pins except the host or parallel interface and the SPI flash interface. This includes RESETZ, PARKZ LED_SEL, CMP_OUT, GPIO, IIC1, TSTPT, and JTAG pins.)	1.64	1.80	1.96	V
V _(VDD_PLLM)	MCG PLL 1.1-V power See (4)	1.025	1.100	1.155	V
V _(VDD_PLLD)	DCG PLL 1.1-V power See (4)	1.025	1.100	1.155	V
TA	Operating ambient temperature ⁽⁵⁾	−30		85	°C
T _J	Operating junction temperature	−30		105	°C

- (1) It is recommended that VDDL12 rail is tied to the VDD rail. The DSI LP supply (VDDL12) is only used for read responses from the controller which are not supported. Because of this, a separate 1.2-V rail is not required. If a separate 1.2-V supply is already being used to power this rail, a voltage tolerance of ±6.67% is allowed on this separate 1.2-V supply.
- (2) When the DSI-PHY LP supply (VDDL12) is fed from a supply separate from VDD, the VDDL12 power must sequence ON after the 1.1-V core supply and must sequence OFF before the 1.1-V core supply.
- (3) These supplies have multiple valid ranges.
- (4) The minimum voltage is lower than other 1.1-V supply minimum to enable additional filtering. This filtering may result in an IR drop across the filter.
- (5) The operating ambient temperature range assumes 0 forced air flow, a JEDEC JESD51 junction-to-ambient thermal resistance value at 0 forced air flow (R_{θJA} at 0 m/s), a JEDEC JESD51 standard test card and environment, along with minimum and maximum estimated power dissipation across process, voltage, and temperature. Thermal conditions vary by application, and this affects R_{θJA}. Thus, maximum operating ambient temperature varies by application.
- (a) $T_{a_min} = T_{J_min} - (P_{d_min} \times R_{\theta JA}) = -30^{\circ}\text{C} - (0.0\text{ W} \times 30.3^{\circ}\text{C/W}) = -30^{\circ}\text{C}$
- (b) $T_{a_max} = T_{J_max} - (P_{d_max} \times R_{\theta JA}) = +105^{\circ}\text{C} - (0.348\text{ W} \times 30.3^{\circ}\text{C/W}) = +94.4^{\circ}\text{C}$

5.4 Thermal information

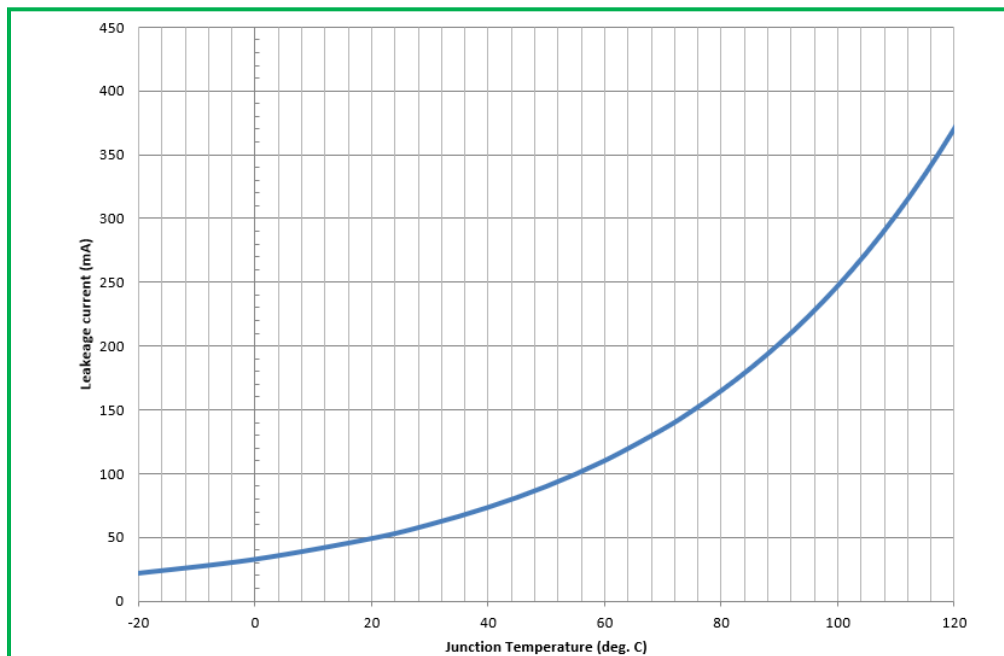
THERMAL METRIC		DLPC2020	UNIT
		ZVB (NFBGA)	
		201 PINS	
$R_{\theta JC}$	Junction-to-case top thermal resistance	11.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.7	°C/W

5.5 Power Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽⁴⁾	MAX ⁽⁵⁾	UNIT
$I_{leak}(VDD)$	1.1V rails Idle	Temperature dependent, see chart		600	mA
$I_{(VDD)}$ + $I_{(VDD_PLLM)}$ + $I_{(VDD_PLLD)}$	1.1V rails Dynamic current (up to 20MHz) Frame rate = 60 Hz		111	160	mA
	Frame rate = 120 Hz		132	196	
$I_{(VDD_PLLM)}$	MCG PLL 1.1-V current ⁽⁶⁾ Frame rate = 60 Hz		6		
	Frame rate = 120 Hz		6		
$I_{(VDD_PLLD)}$	DCG PLL 1.1-V current ⁽⁶⁾ Frame rate = 60 Hz		6		
	Frame rate = 120 Hz		6		
$I_{(VCC18)}$	All 1.8-V I/O current: (1.8-V power supply for all I/O other than the host or parallel interface and the SPI flash interface) Frame rate = 60 Hz		27	36	
	Frame rate = 120 Hz		27	36	

- (1) For the measured cases, all pins using 1.1 V were tied together (including VDDL12), and programmable host and flash I/O are at the minimum nominal voltage (that is 1.8 V).
- (2) Input image is 854 × 480 (WVGA) 24-bits using reduced VESA timings on the parallel interface at the frame rate shown with the 0.2-inch WVGA DMD. The controller has the CAIC and LABB algorithms turned off.
- (3) The measured values do not take into account software updates or customer changes that may affect power performance.
- (4) If measured on a system, typical PVT (process, voltage, and temperature) conditions (i.e. nominal process, typical voltage, and 25°C nominal ambient temperature) and various input images were used.
- (5) Measured on a system with worst case PVT condition(s) (i.e. corner process, high voltage, and high temperature of 65°C) and white noise input image.
- (6) This rail was not measured due to board limitations. Simulation values are used instead. Simulations assume 12.5% activity factor, 30% clock gating on appropriate domains, and mixed SVT (standard threshold voltage) or HVT (high threshold voltage) cells.



5.6 DMD Sub-LVDS Interface Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CM} Common mode voltage		0.5		1.0	V
$V_{CM} (pp)^{(1)}$ V_{CM} change peak-to-peak (during switching)				75	mV
$V_{CM} (ss)^{(1)}$ V_{CM} change steady state		-10		10	mV
$ VOD ^{(2)}$ Differential output voltage magnitude		150	250	350	mV
VOD VOD change (between logic states)		-10		10	mV
V_{OH} Single-ended output voltage high		0.825	1.025	1.175	V
V_{OL} Single-ended output voltage low		0.625	0.775	0.975	V
T_{Xload} 100- Ω differential PCB trace (50- Ω transmission lines)		0.5		6	inches

- (1) See Figure 1
- (2) VOD is the differential voltage measured across a 100- Ω termination resistance connected directly between the transmitter differential pins. $VOD = V_P - V_N$, where P and N are the differential output pins. $|VOD|$ is the magnitude of the peak-to-peak voltage swing across the P and N output pins (see Figure 2). V_{CM} cancels out between signals when measured differentially, thus the reason VOD swings relative to zero.

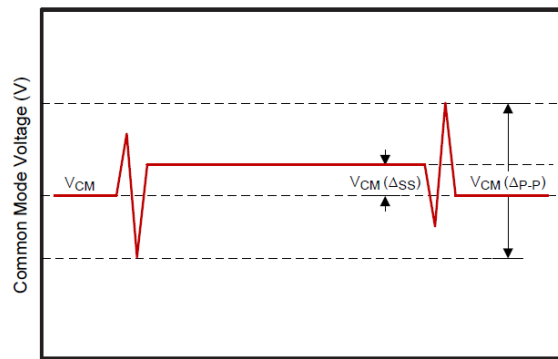


Figure 1. Common Mode Voltage

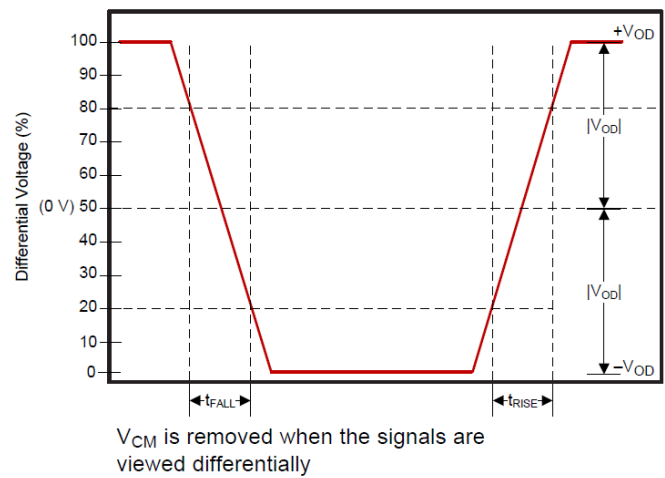


Figure 2. Differential Output Signal

5.7 DMD Sub-LVDS Interface Switching Characteristics

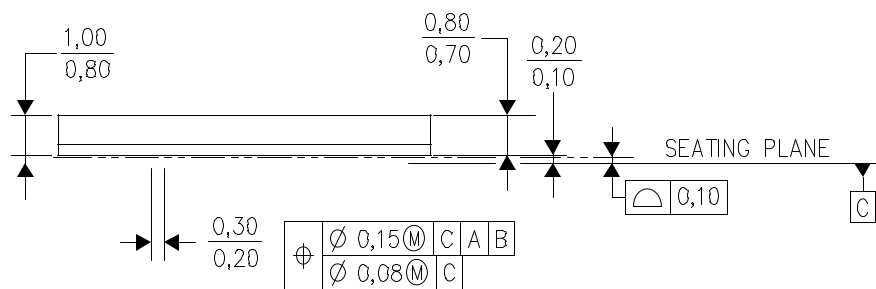
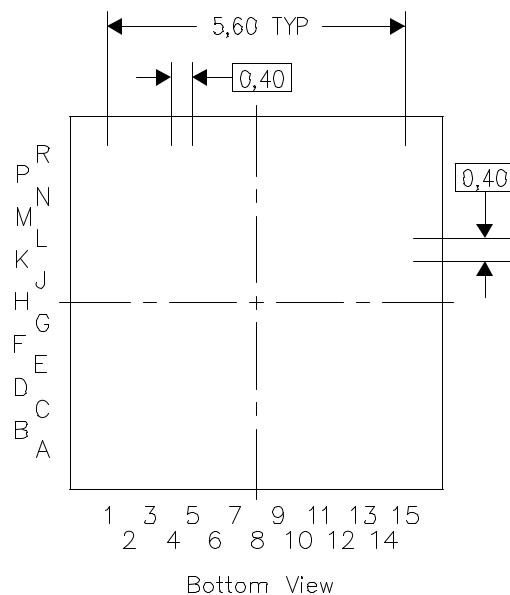
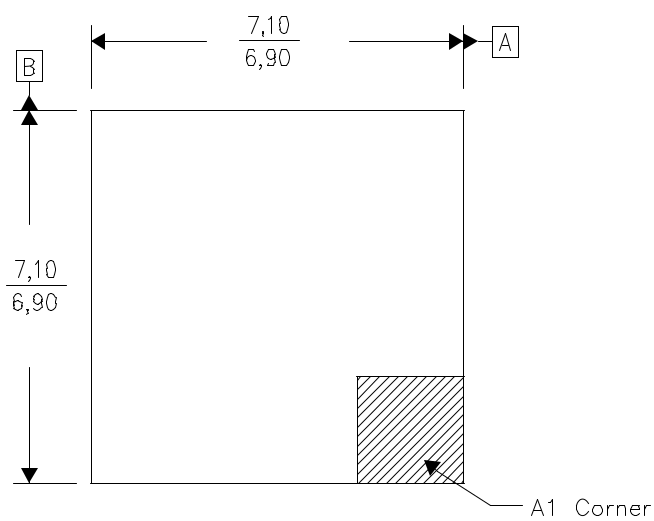
over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_R^{(1)}$ Differential output rise time				250	ps
$t_F^{(1)}$ Differential output fall time				250	
t_{switch} DMD HS Clock switching rate			1200		Mbps
f_{clock} DMD HS Clock frequency			600		MHz
DCout DMD HS Clock output duty cycle		45%	50%	55%	

- (1) Rise and fall times are defined for the differential VOD signal as shown in Figure 2.

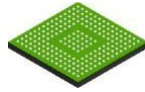
ZVB (S-PBGA-N176)

PLASTIC BALL GRID ARRAY



4211613/A 03/11

- B. This drawing is subject to change without notice.
C. This package is Pb-free.

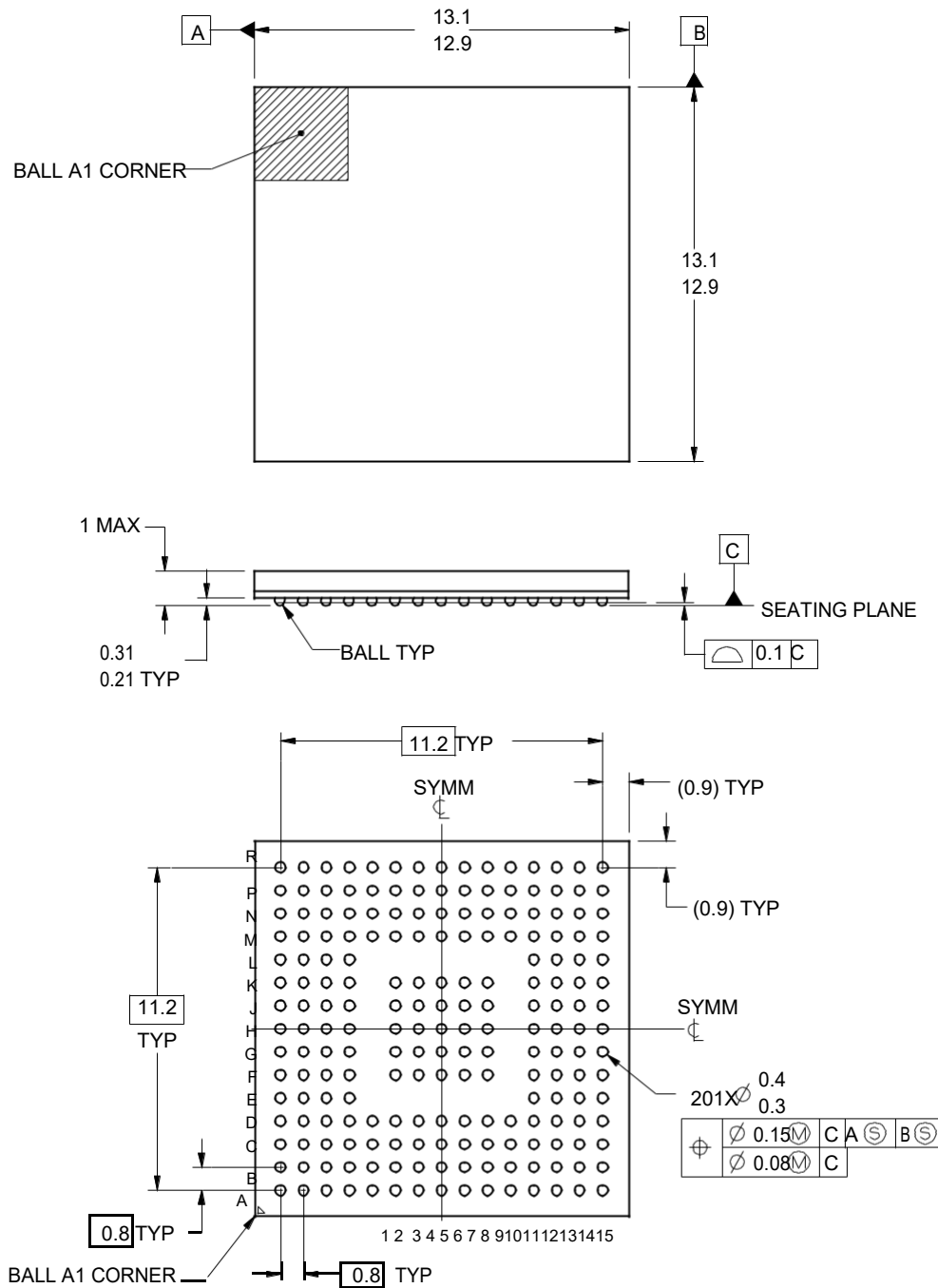


PACKAGE OUTLINE

ZEZO201A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



10/2020

NOTES:

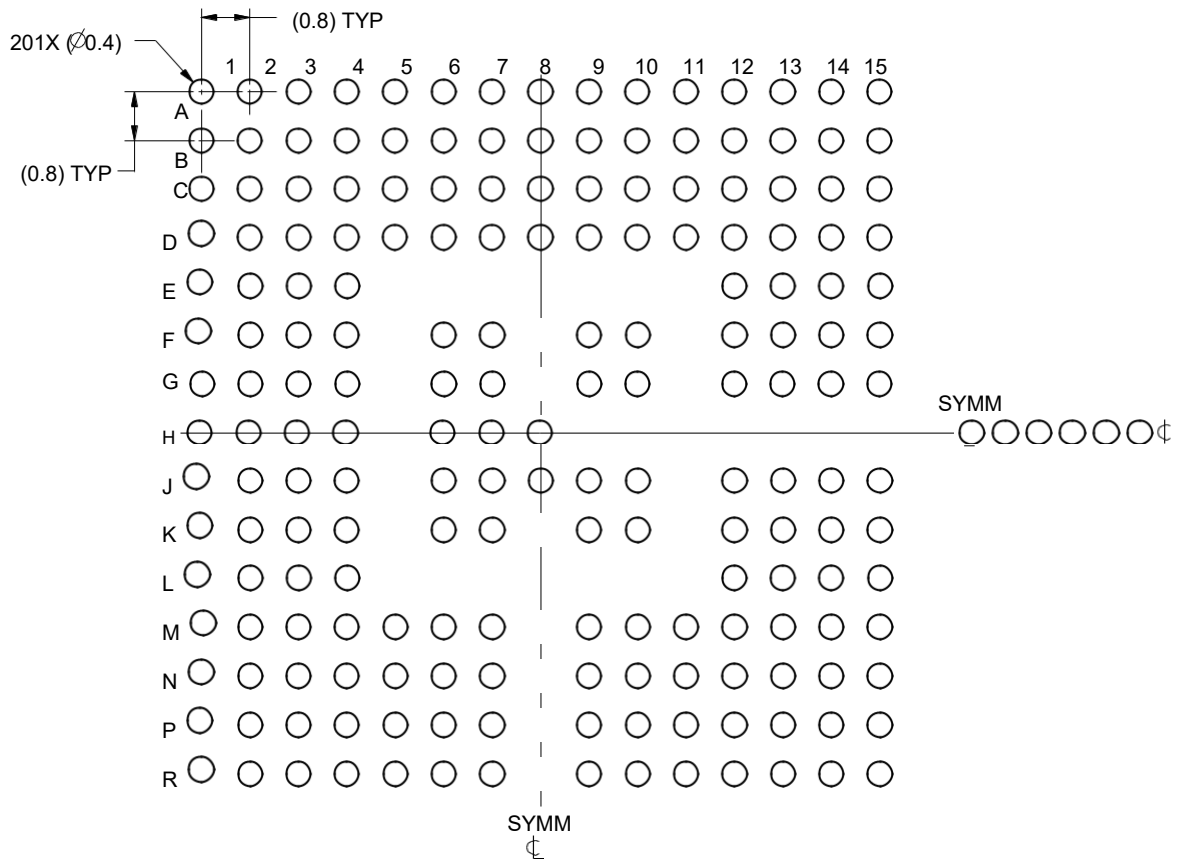
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

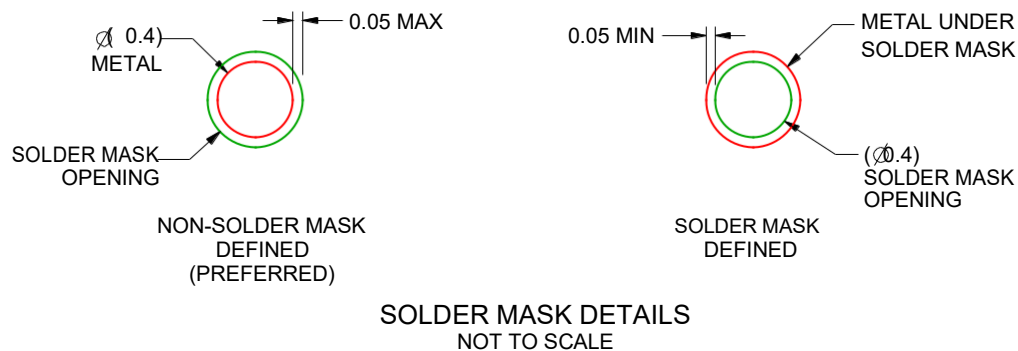
ZEZ0201A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

10/2020

NOTES: (continued)

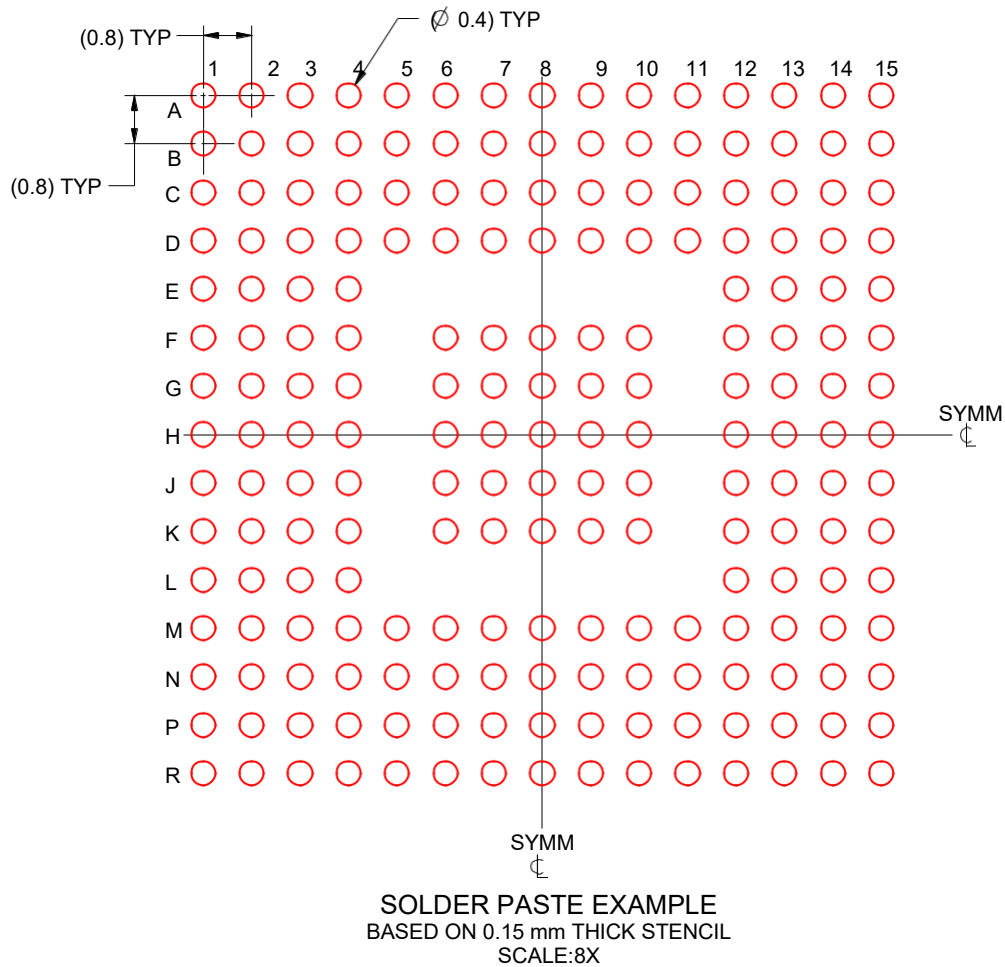
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.

EXAMPLE STENCIL DESIGN

ZEZ0201A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.