

DLP2020 0.2 WVGA DMD

1 Features

- 0.2-Inch (5.29-mm) diagonal micromirror array
 - Displays 854 × 480 pixel array, in an orthogonal layout
 - 5.4-micron micromirror pitch
 - ±17° micromirror tilt (relative to flat surface)
 - Side illumination for optimal efficiency and optical engine size
 - Polarization-independent aluminum micromirror surface
- 4-Bit SubLVDS input data bus
- Dedicated DLPC2020 display and light controller and DLPA2020 PMIC and LED driver for reliable operation

2 Applications

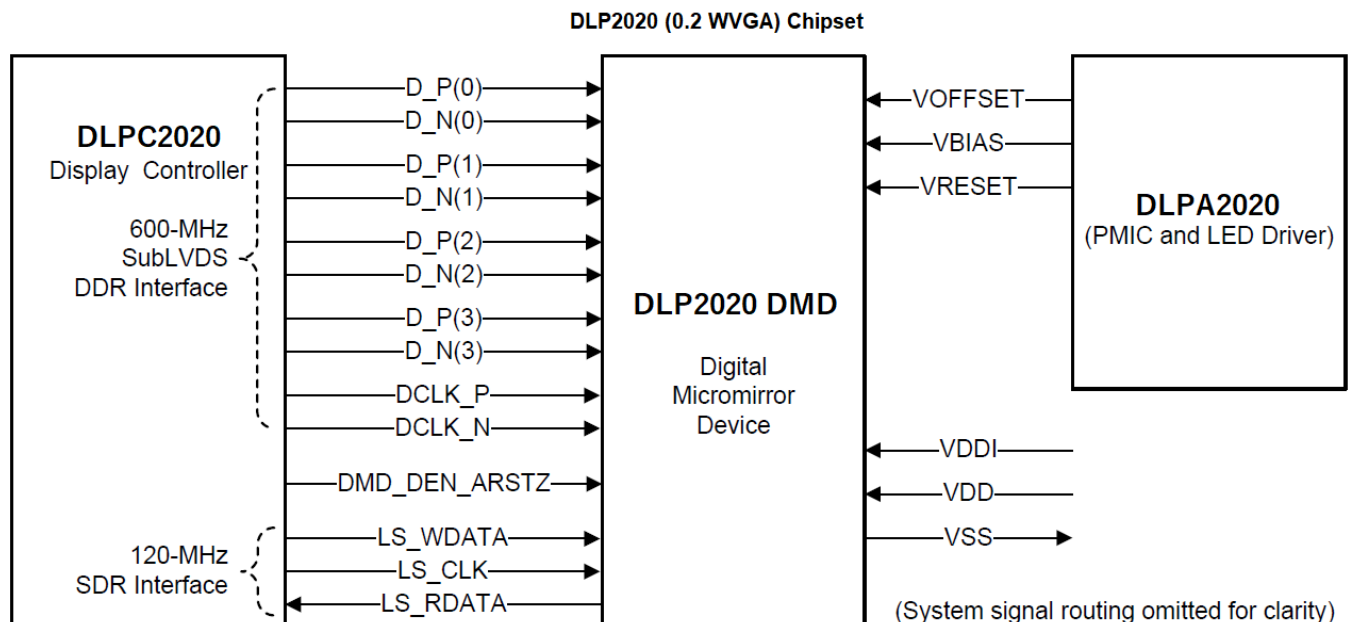
- Embedded Displays for Products Including:
 - Tablets, Mobile Phones
 - Artificial Intelligence (AI) Assistants, Smart Speakers
- Control Panels, Security Systems, and Thermostats
- Wearable Displays
- Integrated Display and 3D Depth Capture
- 3D Depth Capture: 3D Camera, 3D Reconstruction, AR/VR, Dental Scanner
- 3D Machine Vision: Robotics, Metrology, In-line Inspection (AOI)
- Light Exposure: 3D Printers, Laser Marking

3 Description

The [DLP2020](#) digital micromirror device (DMD) is a digitally controlled micro-opto-electromechanical system (MOEMS) spatial light modulator (SLM). When coupled to an appropriate optical system, this DMD is capable of displaying images, video, and patterns. The DLP2020 is part of the chipset that is composed of the DLP2020 DMD, [DLPC2020](#) controller and [DLPA2020](#) PMIC and LED driver. The compact physical size of this DMD can be used in portable equipment where small form factor and low power is important. The compact package compliments the small size of the LEDs for space-constrained light engines.

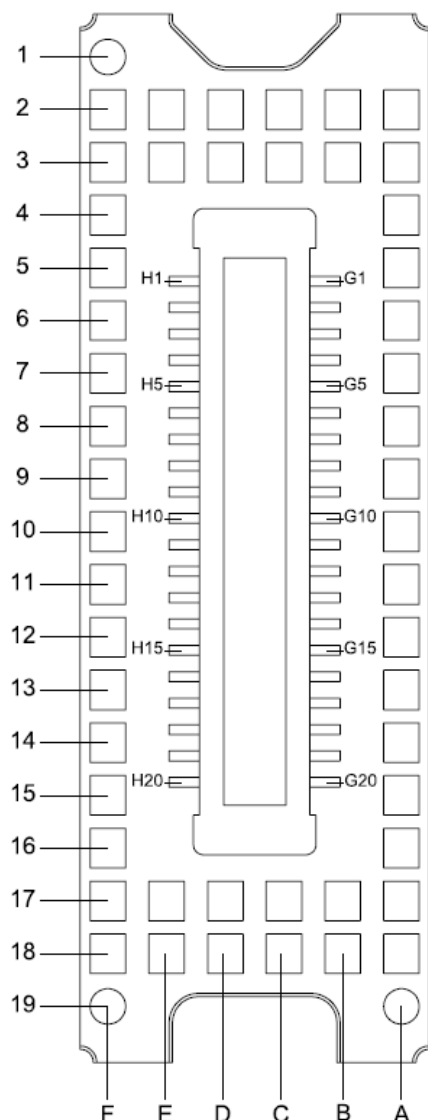
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP2010	FQJ (40)	15.9 mm × 5.3 mm



4 Pin Configuration and Functions

FQJ Package
40-Pin LGA
Bottom View



Pin Functions – Connector Pins⁽¹⁾

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH ⁽²⁾ (mm)
NAME	NO.					
DATA INPUTS						
D_N(0)	G4	I	SubLVDS	Double	Data, Negative	7.03
D_P(0)	G3	I	SubLVDS	Double	Data, Positive	7.03
D_N(1)	G8	I	SubLVDS	Double	Data, Negative	7.03
D_P(1)	G7	I	SubLVDS	Double	Data, Positive	7.03
D_N(2)	H5	I	SubLVDS	Double	Data, Negative	7.02
D_P(2)	H6	I	SubLVDS	Double	Data, Positive	7.02

- (1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* [JESD209B](#).
- (2) Net trace lengths inside the package:
Relative dielectric constant for the FQJ ceramic package is 9.8.
Propagation speed = $11.8 / \sqrt{9.8} = 3.769$ inches/ns.
Propagation delay = 0.265 ns/inch = 265 ps/inch = 10.43 ps/mm.

Pin Functions – Connector Pins⁽¹⁾ (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH ⁽²⁾ (mm)
NAME	NO.					
D_N(3)	H1	I	SubLVDS	Double	Data, Negative	7.00
D_P(3)	H2	I	SubLVDS	Double	Data, Positive	7.00
DCLK_N	H9	I	SubLVDS	Double	Clock, Negative	7.03
DCLK_P	H10	I	SubLVDS	Double	Clock, Positive	7.03
CONTROL INPUTS						
DMD_DEN_ARSTZ	G12	I	LPSDR ⁽¹⁾		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	5.72
LS_CLK	G19	I	LPSDR	Single	Clock for low-speed interface	3.54
LS_WDATA	G18	I	LPSDR	Single	Write data for low-speed interface	3.54
LS_RDATA	G11	O	LPSDR	Single	Read data for low-speed interface	8.11
POWER						
VBIAS ⁽³⁾	H17	Power			Supply voltage for positive bias level at micromirrors	
VOFFSET ⁽³⁾	H13	Power			Supply voltage for HVCMOS core logic. Includes: supply voltage for stepped high level at micromirror address electrodes and supply voltage for offset level at micromirrors	
VRESET ⁽³⁾	H18	Power			Supply voltage for negative reset level at micromirrors	
VDD ⁽³⁾	G20	Power			Supply voltage for micromirror low voltage CMOS core logic includes supply voltage for LPSDR inputs and supply voltage for normal high level at micromirror address electrodes.	
VDD	H14	Power				
VDD	H15	Power				
VDD	H16	Power				
VDD	H19	Power				
VDD	H20	Power			Supply voltage for SubLVDS receivers	
VDDI ⁽³⁾	G1	Power				
VDDI	G2	Power				
VDDI	G5	Power				
VDDI	G6	Power			Ground. Common return for all power.	
VSS ⁽³⁾	G9	Ground				
VSS	G10	Ground				
VSS	G13	Ground				
VSS	G14	Ground				
VSS	G15	Ground				
VSS	G16	Ground				
VSS	G17	Ground				
VSS	H3	Ground				
VSS	H4	Ground				
VSS	H7	Ground				
VSS	H8	Ground				
VSS	H11	Ground				
VSS	H12	Ground				

(3) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

			MIN	MAX	UBIT
Supply voltage	VDD	for LVC MOS core logic ⁽²⁾ Supply voltage for LPSDR low speed interface	−0.5	2.3	V
	VDDI	for SubLVDS receivers ⁽²⁾	−0.5	2.3	
	VOFFSET	for HVC MOS and micromirror electrode ⁽²⁾⁽³⁾	−0.5	10.6	
	VBIAS	for micromirror electrode ⁽²⁾	−0.5	19	
	VRESET	for micromirror electrode ⁽²⁾	−15	0.5	
	VDDI−VDD	delta (absolute value) ⁽⁴⁾		0.3	
	VBIAS−VOFFSET	delta (absolute value) ⁽⁵⁾		11	
	VBIAS−VRESET	delta (absolute value) ⁽⁶⁾		34	
Input voltage	for other inputs LPSDR ⁽²⁾		−0.5	VDD + 0.5	V
	for other inputs SubLVDS ⁽²⁾⁽⁷⁾		−0.5	VDDI + 0.5	
Input pins	VID	SubLVDS input differential voltage (absolute value) ⁽⁷⁾		810	mV
	IID	SubLVDS input differential current		8.1	mA
Clock frequency	f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high speed interface DCLK		620	

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above or below the *Recommended Operating Conditions* for extended periods may affect device reliability.
- (2) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.
- (3) VOFFSET supply transients must fall within specified voltages.
- (4) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw.
- (5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.
- (6) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw.
- (7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾⁽²⁾⁽³⁾

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE⁽⁴⁾					
VDD	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
VDDI	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode ⁽⁵⁾	9.5	10	10.5	V
VBIAS	Supply voltage for mirror electrode	17.5	18	18.5	V
VRESET	Supply voltage for micromirror electrode	-14.5	-14	-13.5	V
VDDI-VDD	Supply voltage delta (absolute value) ⁽⁶⁾			0.3	V
VBIAS-VOFFSET	Supply voltage delta (absolute value) ⁽⁷⁾			10.5	V
VBIAS-VRESET	Supply voltage delta (absolute value) ⁽⁸⁾			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK ⁽⁹⁾	108		120	MHz
f_{clock}	Clock frequency for high speed interface DCLK ⁽¹⁰⁾	300		600	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE⁽¹⁰⁾					
VID	SubLVDS input differential voltage (absolute value) Figure 8 , Figure 9	100	150	300	mV
V_{CM}	Common mode voltage Figure 8 , Figure 9	450		1100	mV
V_{SUBLVDS}	SubLVDS voltage Figure 8 , Figure 9	300		1250	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω

(1) [Recommended Operating Conditions](#) are applicable after the DMD is installed in the final product.

(2) The functional performance of the device specified in this datasheet is achieved when operating the device within the limits defined by the [Recommended Operating Conditions](#). No level of performance is implied when operating the device above or below the [Recommended Operating Conditions](#) limits.

(3) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.

(4) All voltage values are with respect to the ground pins (VSS).

(5) VOFFSET supply transients must fall within specified maximum voltages.

(6) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.

(7) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.

(8) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit.

(9) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.

(10) Refer to the SubLVDS timing requirements in [Timing Requirements](#).

5.4 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP	MAX	UNIT
CURRENT						
I _{DD}	Supply current: VDD ⁽³⁾⁽⁴⁾	VDD = 1.95 V			34.7	mA
		VDD = 1.8 V		27.5		
I _{DDI}	Supply current: VDDI ⁽³⁾⁽⁴⁾	VDDI = 1.95 V			9.4	mA
		VDD = 1.8 V		6.6		
I _{OFFSET}	Supply current: VOFFSET ⁽⁵⁾⁽⁶⁾	VOFFSET = 10.5 V			1.7	mA
		VOFFSET = 10 V		0.9		
I _{BIAS}	Supply current: VBIAS ⁽⁵⁾⁽⁶⁾	VBIAS = 18.5 V			0.4	mA
		VBIAS = 18 V		0.2		
I _{RESET}	Supply current: VRESET ⁽⁶⁾	VRESET = −14.5 V			2	mA
		VRESET = −14 V		1.2		
POWER ⁽⁷⁾						
P _{DD}	Supply power dissipation: VDD ⁽³⁾⁽⁴⁾	VDD = 1.95 V			67.7	mW
		VDD = 1.8 V		49.5		
P _{DDI}	Supply power dissipation: VDDI ⁽³⁾⁽⁴⁾	VDDI = 1.95 V			18.3	mW
		VDD = 1.8 V		11.9		
P _{OFFSET}	Supply power dissipation: VOFFSET ⁽⁵⁾⁽⁶⁾	VOFFSET = 10.5 V			17.9	mW
		VOFFSET = 10 V		9		
P _{BIAS}	Supply power dissipation: VBIAS ⁽⁵⁾⁽⁶⁾	VBIAS = 18.5 V			7.4	mW
		VBIAS = 18 V		3.6		
P _{RESET}	Supply power dissipation: VRESET ⁽⁶⁾	VRESET = −14.5 V			29	mW
		VRESET = −14 V		16.8		
P _{TOTAL}	Supply power dissipation: Total			90.8	140.3	mW
CAPACITANCE						
C _{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			20	
C _{OUT}	Output capacitance	f = 1 MHz			10	pF
C _{RESET}	Reset group capacitance	f = 1 MHz; (480 × 108) micromirrors	95		113	pF

(1) Device electrical characteristics are over [Recommended Operating Conditions](#) unless otherwise noted.

(2) All voltage values are with respect to the ground pins (VSS).

(3) To prevent excess current, the supply voltage delta |VDDI – VDD| must be less than specified limit.

(4) Supply power dissipation based on non-compressed commands and data.

(5) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.

(6) Supply power dissipation based on 3 global resets in 200 μs.

(7) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.

5.5 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

			MIN	NOM	MAX	UNIT
SubLVDS						
t_R	Rise slew rate	20% to 80% reference points, Figure 4	0.55	1		V/ns
t_F	Fall slew rate	80% to 20% reference points, Figure 4	0.55	1		V/ns
t_C	Cycle time DCLK,	Figure 6	1.61	1.67		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, Figure 6	0.71			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, Figure 6	0.71			ns
t_{SU}	Setup time	D(0:3) valid before DCLK \uparrow or DCLK \downarrow , Figure 6	0.355			ns
t_H	Hold time	D(0:3) valid after DCLK \uparrow or DCLK \downarrow , Figure 6	0.355			ns
t_{WINDOW}	Window time	Setup time + Hold time, Figure 6 , Figure 7	0.71			ns

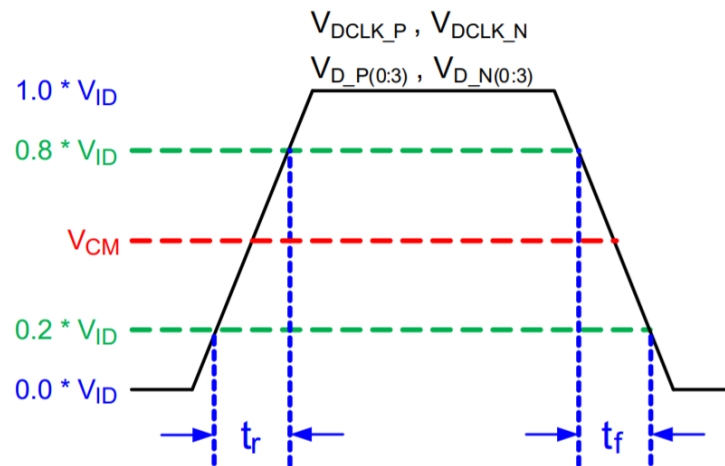


Figure 4. SubLVDS Input Rise and Fall Slew Rate

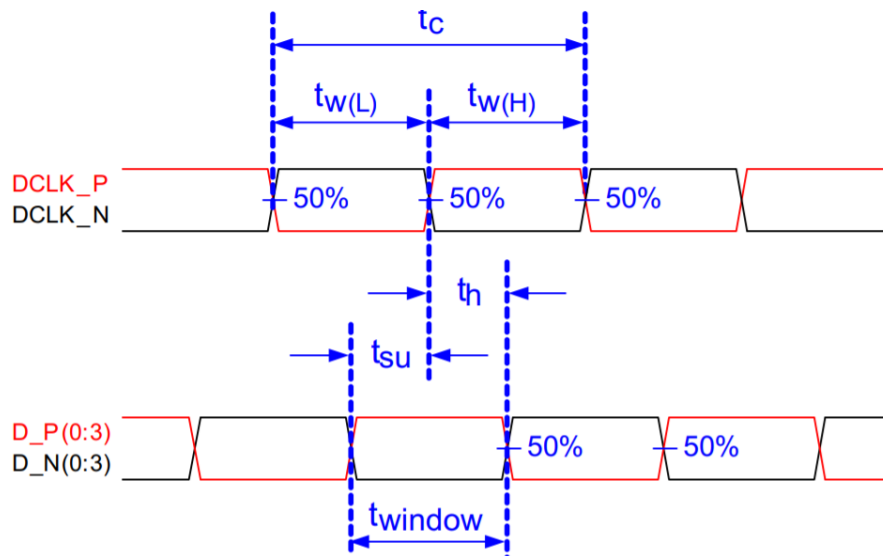
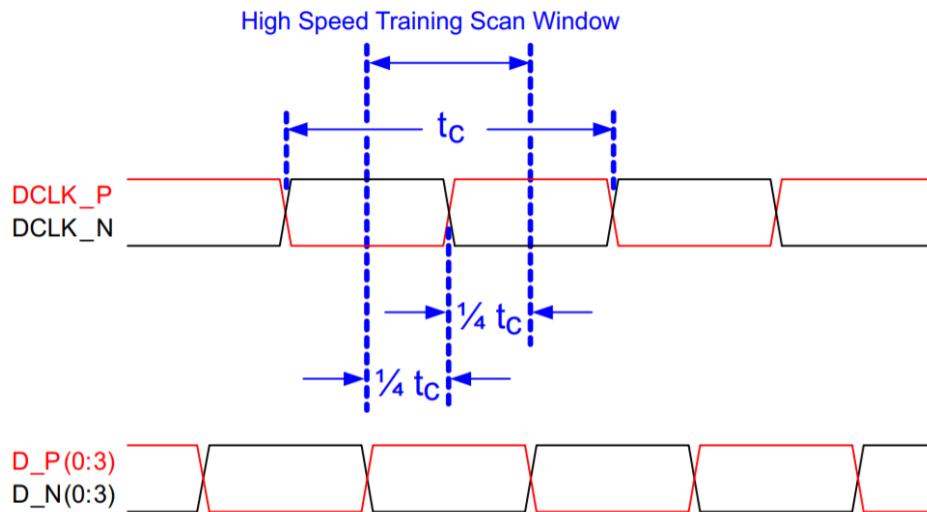


Figure 6. SubLVDS Switching Parameters



Note: Refer to [High-Speed Interface](#) for details.

Figure 7. High-Speed Training Scan Window

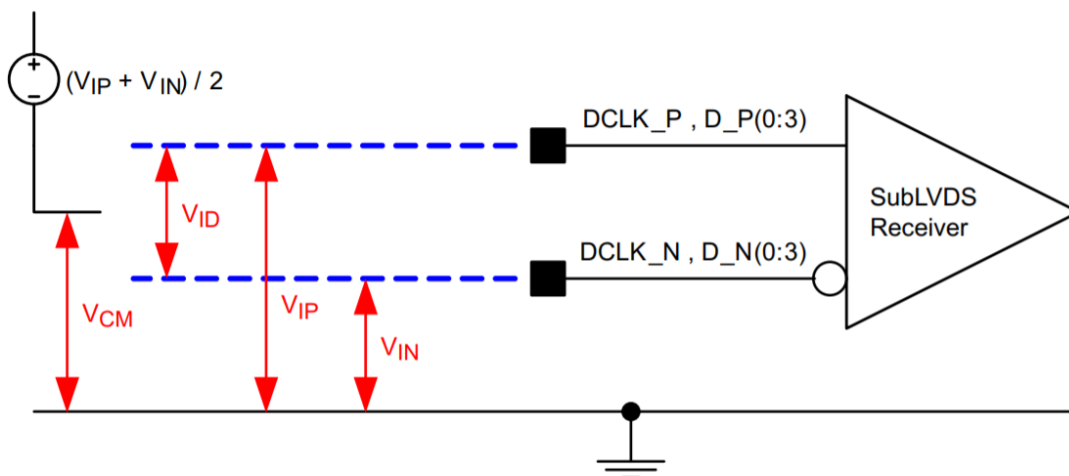


Figure 8. SubLVDS Voltage Parameters

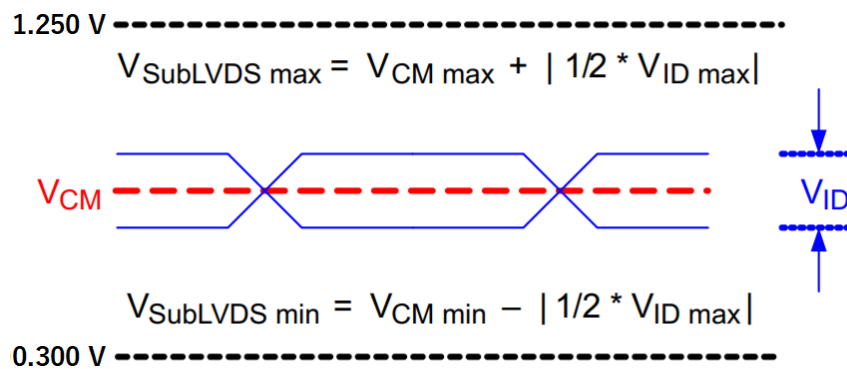


Figure 9. SubLVDS Waveform Parameters