

DLPA2020 Power Management and LED/Lamp Driver IC

1 Features

- High Efficiency RGB LED/Lamp Driver with Buck-Boost DC-to-DC Converter, DMD Supplies, DPP Core Supply, 1.8-V Load Switch, and Measurement System in a Small Chip-Scale Package
 - Three Low-Impedance (30 mΩ Typical at 27°C)
 - MOSFET Switches for Channel Selection
 - Independent, 10-Bit Current Control per Channel
 - 2.4-A Max LED Current for DLPA2020 Embedded Applications
 - DMD Regulators
 - Requires Only a Single Inductor
 - VOFS: 10 V
 - VBIAS: 18 V
 - VRST: -14 V
 - Passive Discharge to GND When Disabled
 - DPP 1.1-V Core Supply
 - Synchronous Step-Down Converter With Integrated Switching FETs
 - Supports up to 900-mA Output Current
 - VLED Buck Boost Converter
 - Power Save Mode at Light Load Current
 - Low-Impedance Load Switch
 - V_{IN} Range from 1.8 to 3.6 V
 - Supports up to 200 mA of Current
 - Passive Discharge to GND When Disabled
 - DMD Reset Signal Generation and Power Supply Sequencing
 - 33-MHz Serial Peripheral Interface (SPI)
 - Multiplexer for Measuring Analog Signals
 - Battery Voltage
 - LED Voltage, LED Current
 - Light Sensor (for White Point Correction)
 - Internal Reference Voltage
 - External (Thermistor) Temperature Sensor
 - Monitoring and Protection Circuits
 - Hot Die Warning and Thermal
 - Low-Battery Warning
 - Programmable Battery Undervoltage Lockout (UVLO)
 - Load Switch UVLO
 - Overcurrent and Undervoltage Protection
 - DLPA2020 QFN Package
 - 48-Pin 0.4-mm Pitch
 - Die Size: 6.0 mm x 6.0 mm ± 0.15 mm
- ## 2 Applications
- DLP® Pico™ Projector
 DLP® Mobile Sensing
- ## 3 Description
- DLPA2020 is a dedicated PMIC/RGB LED/Lamp driver for the DLP2020 Digital Micromirror Device (DMD) when used with a DLPC2020 digital controller.
- | Device Information ⁽¹⁾ | | |
|-----------------------------------|-----------|---------------------------------|
| PART NUMBER | PACKAGE | BODY SIZE (NOMINAL) |
| DLPA2020 | VQFN (48) | 6.00 mm x 6.00 mm
± 0.150 mm |
- (1) For all available packages, see the orderable addendum at the end of the data sheet.

2 Applications

DLP® Pico™ Projector

DLP® Mobile Sensing

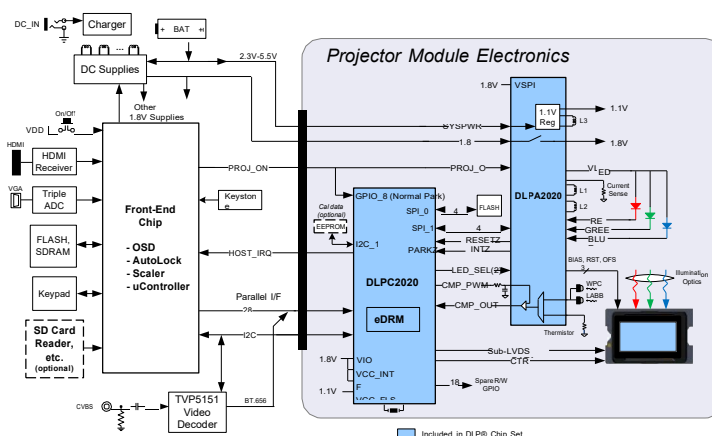
3 Description

DLPA2020 is a dedicated PMIC/RGB LED/Lamp driver for the DLP2020 Digital Micromirror Device (DMD) when used with a DLPC2020 digital controller.

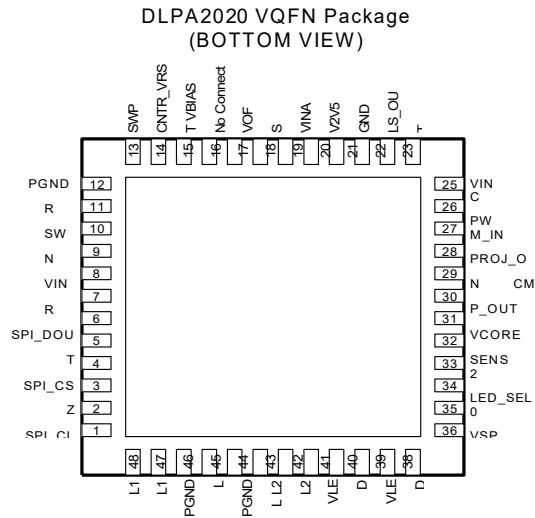
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPA2020	VQFN (48)	6.00 mm x 6.00 mm ± 0.150 mm

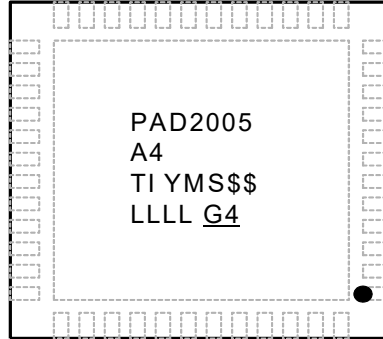
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4 Pin Configuration and Functions



Package Marking DLPA2020
(TOP VIEW)



TI = TI LETTERS
YM = YEAR MONTH DATE CO
DE LLLL = ASSY LOT CODE
S = ASSEMBLY SITE CO
DE PER QSS 005-120
\$\$ = WAFER FAB CODE
(1 or 2
CHARACTERS)

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
VINL	1	I	Power supply input for VLED BUCK-BOOST power stage. Connect to system power.
	2		
SPI_DIN	3	I	SPI data input
RESETZ	4	O	Reset output to the DLP system (active low). Pin is held low to reset DLP system.
AGND1	5	GND	Analog ground. Connect to ground plane.
INTZ	6	O	Interrupt output signal (open drain). Connect to pullup resistor or short to ground.
SPI_CLK	7	I	Clock input for SPI interface
SPI_CSZ	8	I	SPI chip select (active low)
SPI_DOUT	9	O	SPI data output
VINR	10	I	Power supply input for DMD switch mode power supply (SMPS). Connect to system power.
SWN	11	I	Connection for the DMD SMPS-inductor (high-side switch).
PGNDR	12	GND	Power ground for DMD SMPS. Connect to ground plane.
SWP	13	O	Connection for the DMD SMPS-inductor (low-side switch).
CNTR_VRST	14	O	Connection to VRST for fast discharge function
VBIAS	15	O	VBIAS output rail. Connect to ceramic capacitor.
No Connect	16	I	
VOFS	17	O	VOFS output rail. Connect to ceramic capacitor.
VINA	18	POWER	Power supply input for sensitive analog circuitry
V2V5	19	O	Internal supply filter pin for digital logic; typical 2.5 V
GND	20	GND	Ground connection to be connected to ground plane.
LS_OUT	21	O	Load switch
LS_IN	22	I	Load switch
PGNDC	23	GND	Power ground for VCORE BUCK
SWC	24	I/O	Connection for 1.1-V BUCK inductor
VINC	25	I	Power supply input for VCORE BUCK power stage. Connect to system power.
PWM_IN	26	I	Reference voltage input for analog comparator.
PROJ_ON	27	I	Input signal to enable or disable the IC and DLP projector.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Input voltage at VINL, VINA, VINR, VINC	-0.3	7	V
Ground pins to system ground	-0.3	0.3	V
Voltage at SWN	-18	7	V
Voltage at SWP, VBIAS	-0.3	20	V
Voltage at VOFS	-0.3	12	V
Voltage at V6V, VLED, L1, L2, SWC, SW4, SW5, SW6, INTZ, PROJ_ON	-0.3	7	V
Voltage at all pins, unless noted otherwise	-0.3	3.6	V
Source current RESETZ, CMP_OUT		1	mA
Source current SPI_DOUT		5.5	mA
Sink current RESETZ, CMP_OUT		1	mA
Sink current SPI_DOUT, INTZ		5.5	mA
Peak output current	Internally limited		
Continuous total power dissipation	Internally limited by thermal shutdown		
T _J Operating junction temperature	-30	150	°C
T _{stg} Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT	
Input voltage at VINL, VINA, VINR, VINC,	Full functional and parametric performance	2.7	3.6	6	V	
	Extended operating range, limited parametric performance	2.3	3.6	6		
Voltage at VSPI		1.65	1.8	3.6	V	
Operational ambient temperature		-10			85	°C
Operational junction temperature		-10			120	°C

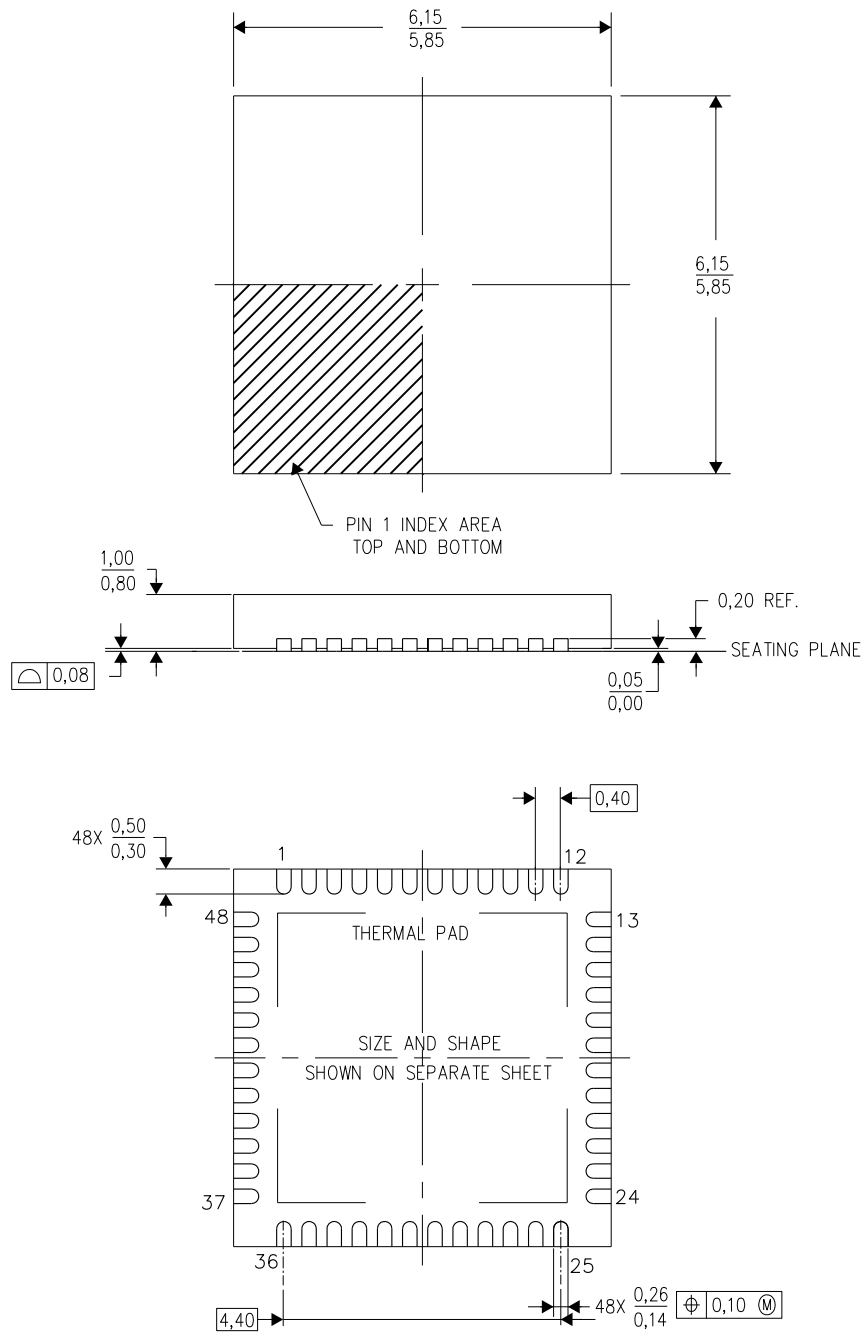
5.4 Thermal Information

THERMAL METRIC		DLPA2020	UNIT
		VQFN (40pins)	
R _{θJB}	Junction-to-board thermal resistance	4.9	°C/W
R _{θJC}	Junction-to-case top thermal resistance	25.6	°C/W

6 Mechanical and Packaging Information

RSL (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



4207548/B 06/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

THERMAL PAD MECHANICAL DATA

RSL (S-PVQFN-N48)

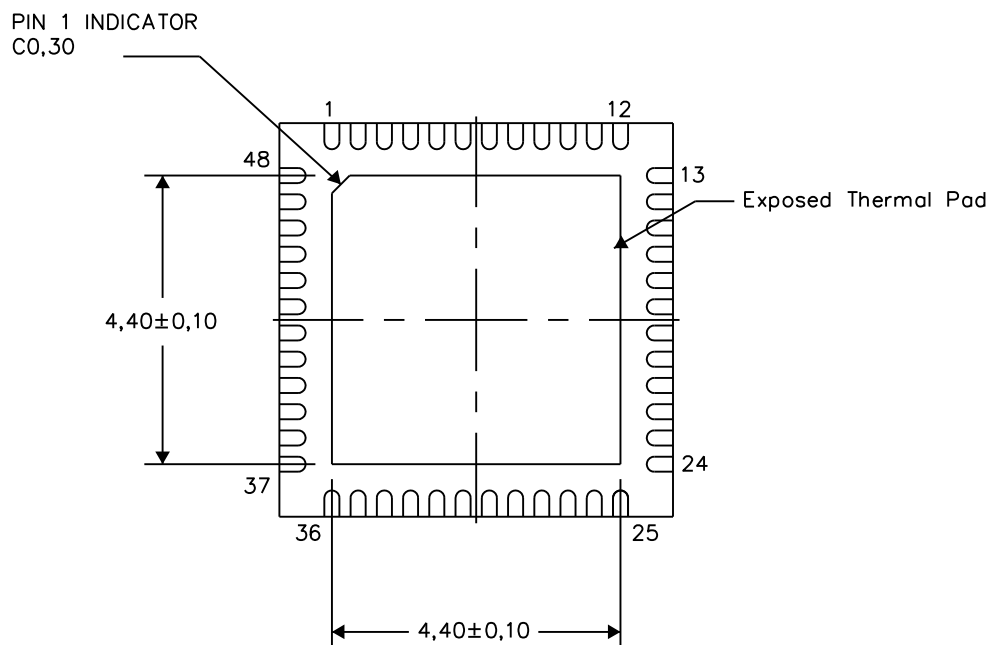
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

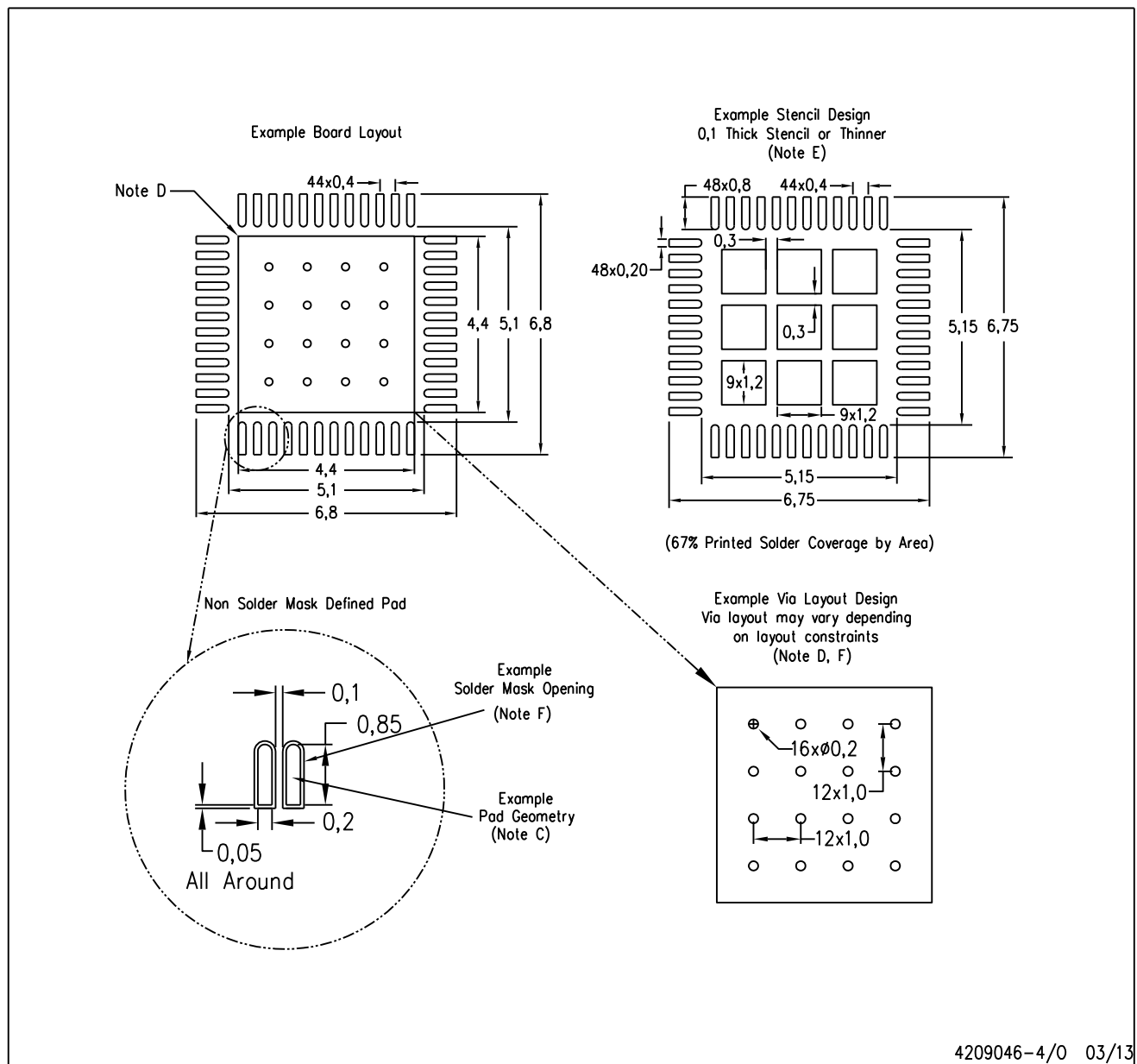
Exposed Thermal Pad Dimensions

4207841-2/P 03/13

NOTE: All linear dimensions are in millimeters

RSL (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.