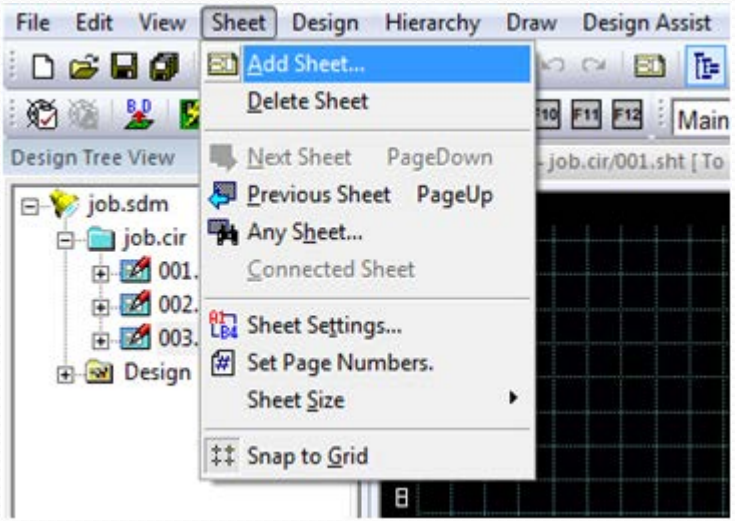
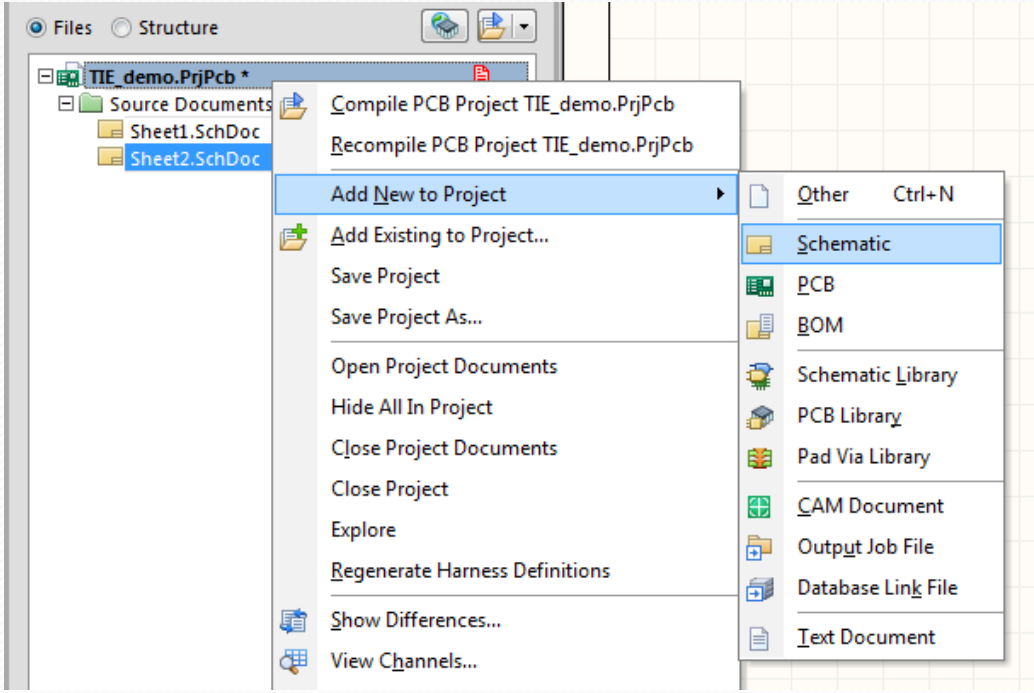
What Design Tool to use for TIE Contest?

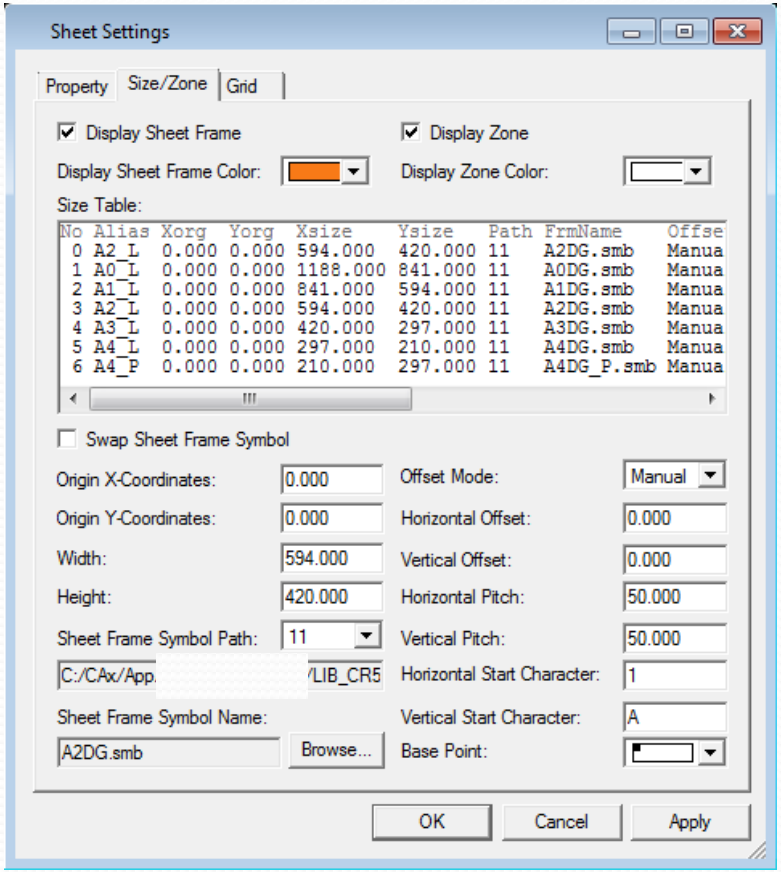
Tool Requirements for Participation to TIE Professional Student Design Contest

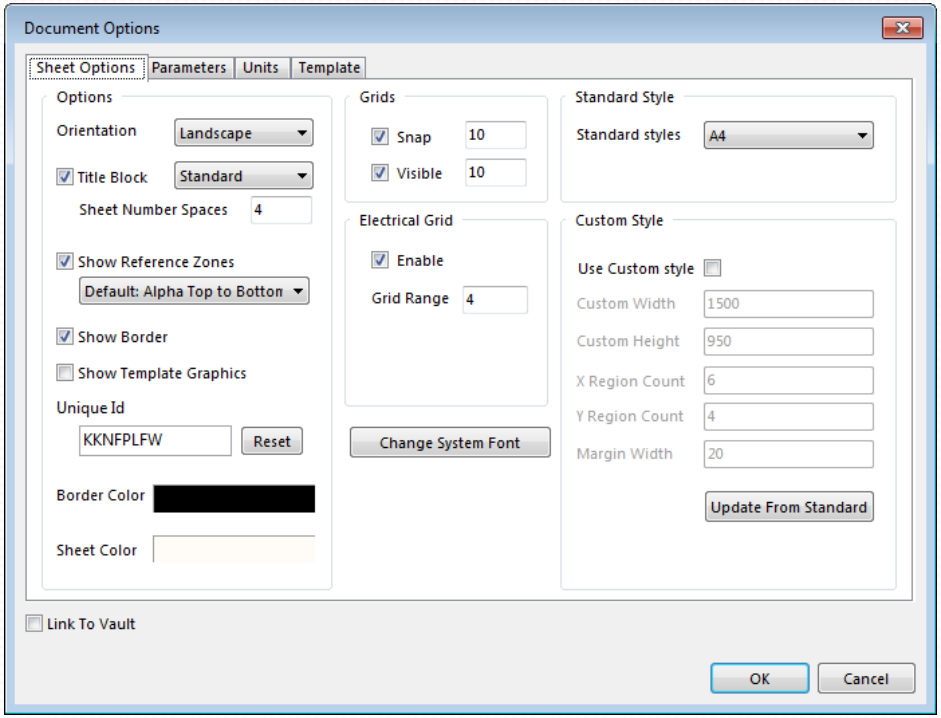
Multiple schematic pages (sheets) in one project



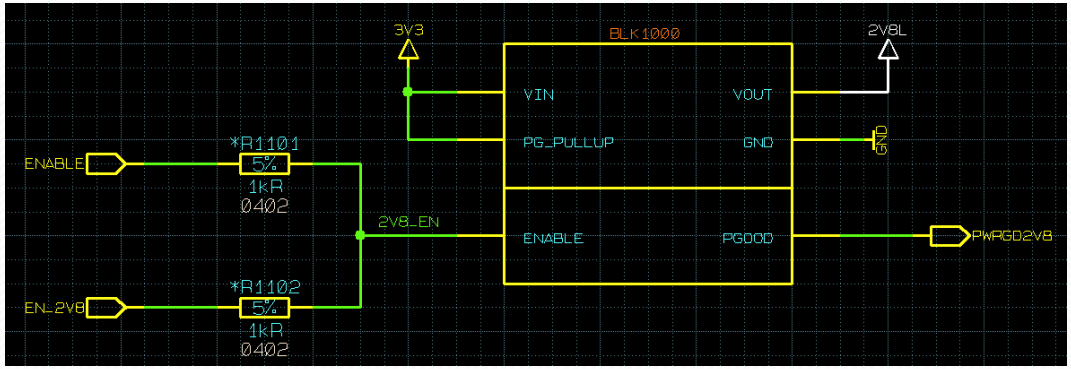


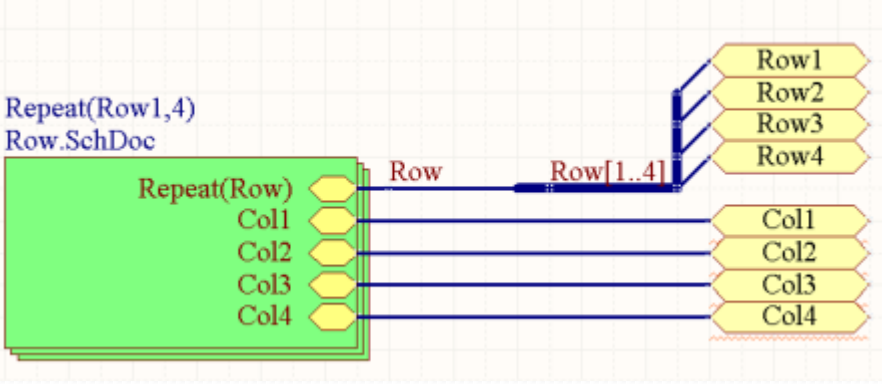
Control of schematic formats (ex: A4, A3, A2,…)



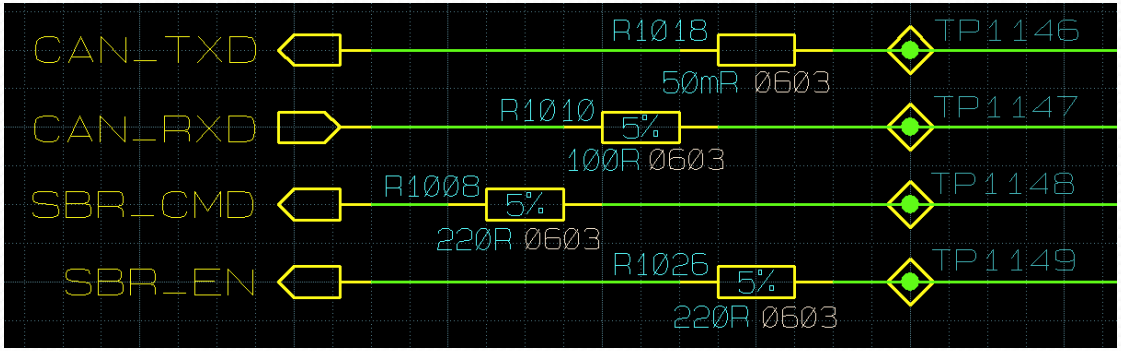


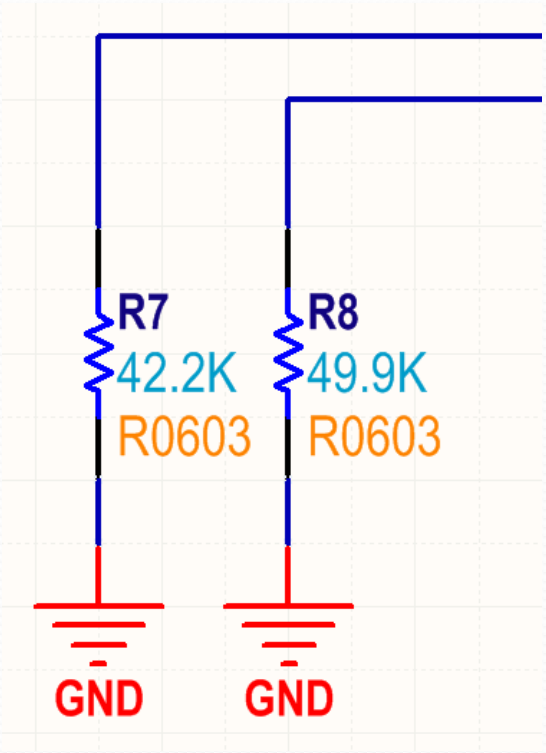
Support for hierarchical projects



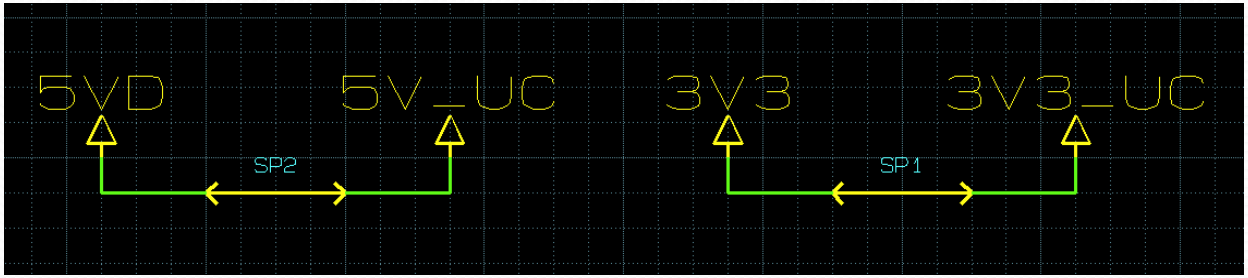


Display/hide component information (ex: value, tolerance, footprint, …)

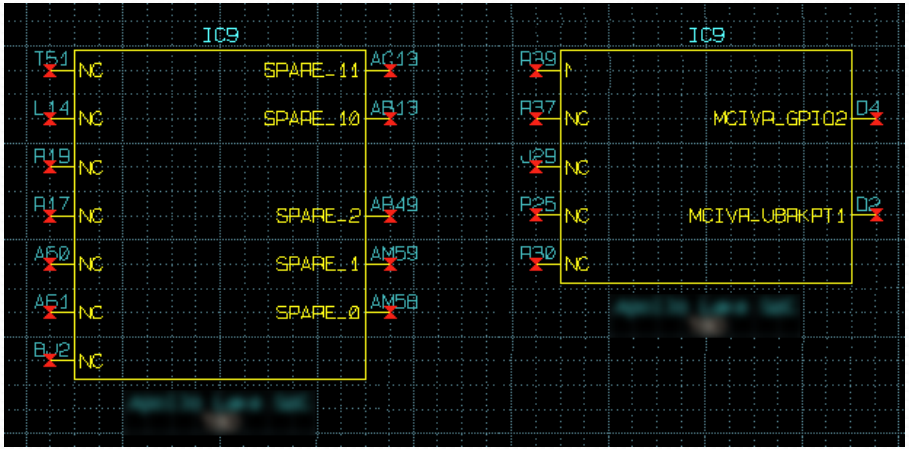


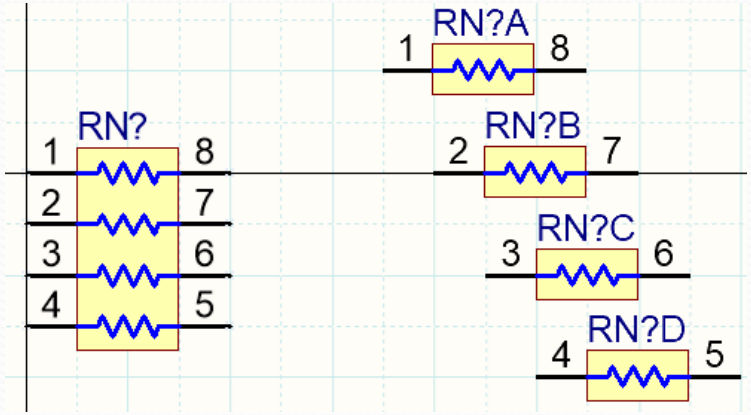


Star-point definition

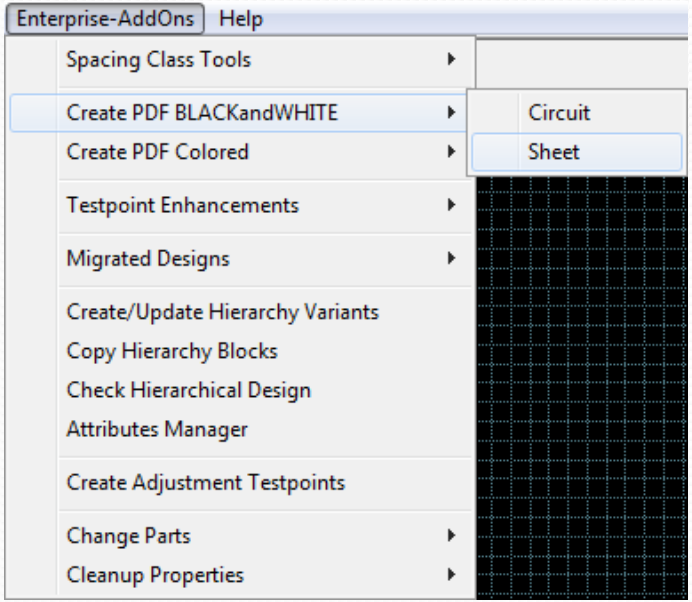


Multi-entity component creation





PDF export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Create/Update Hierarchy Variants
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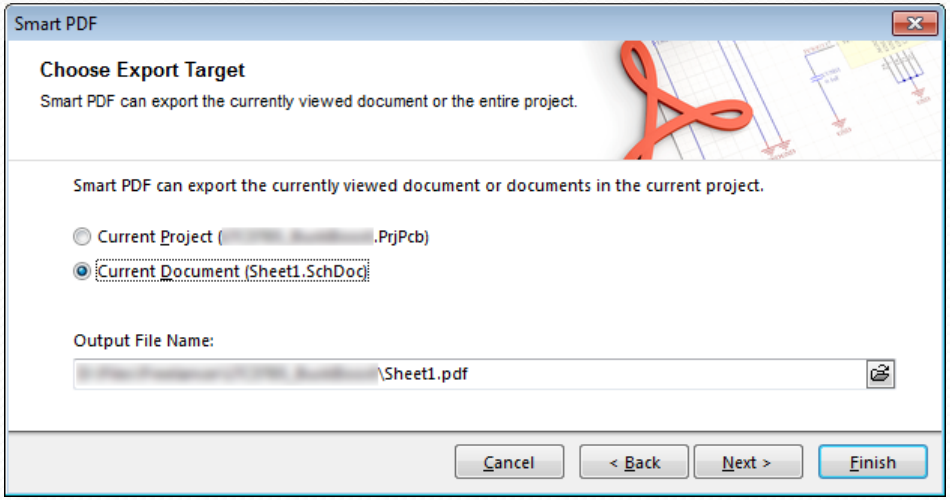
Attributes Manager
Create Adjustment Testpoints
Change Parts
Cleanup Properties
Circuit
Sheet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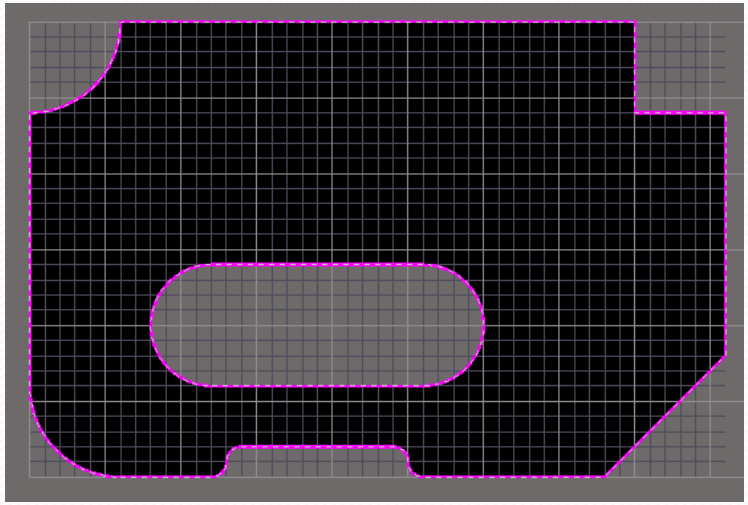
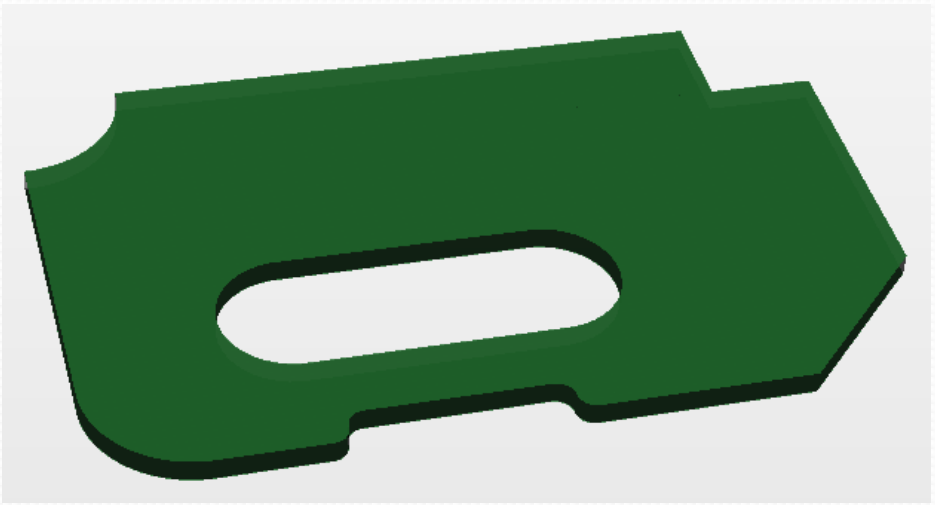
Creation of complex PCB shapes (ex: rounded corners, cutouts)





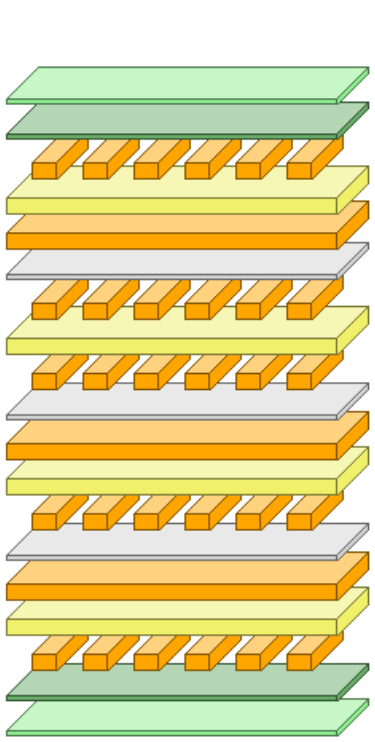
Stack-up definition (number of layers, copper thickness, dielectric type, core / prepreg thickness, etc.)

Material: FR-4

Layer Construction

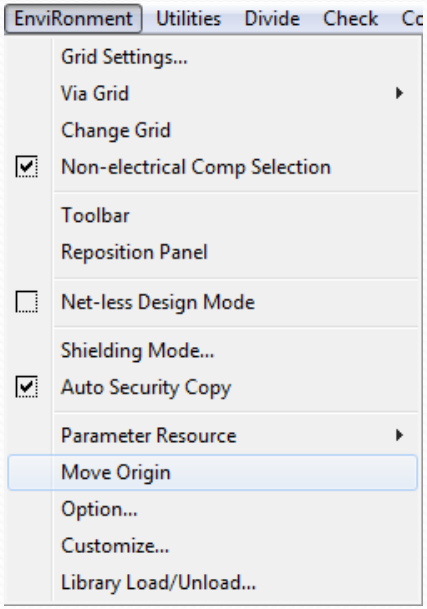
Core Layer: From 4 To 5

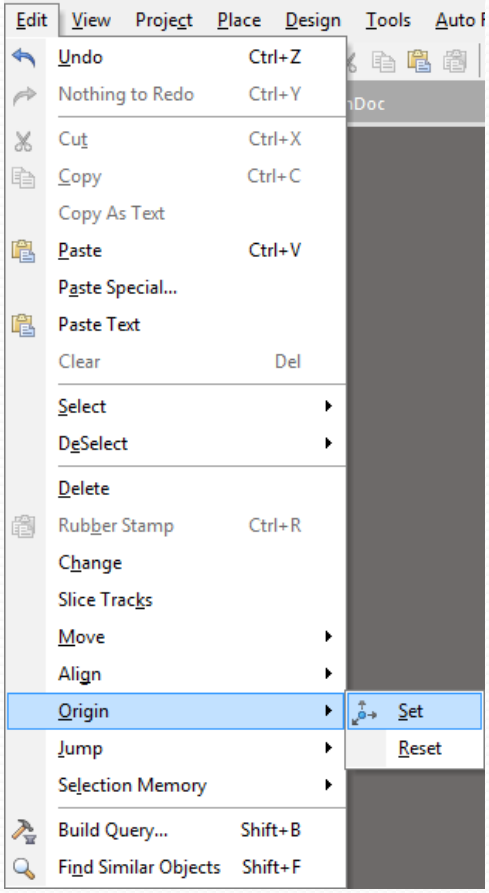
Lay.	Layer thickne…	Material
Resist LayerA	0.025	Probimer 65
Conductor1	0.043	Copper
Insulating1-2	0.073	FR-4
Conductor2	0.043	Copper
Insulating2-3	0.110	FR-4
Conductor3	0.037	Copper
Insulating3-4	0.254	FR-4
Conductor4	0.035	Copper
Insulating4-5	0.350	FR-4
Conductor5	0.035	Copper
Insulating5-6	0.254	FR-4
Conductor6	0.037	Copper
Insulating6-7	0.110	FR-4
Conductor7	0.043	Copper
Insulating7-8	0.073	FR-4
Conductor8	0.043	Copper
Resist LayerB	0.025	Probimer 65



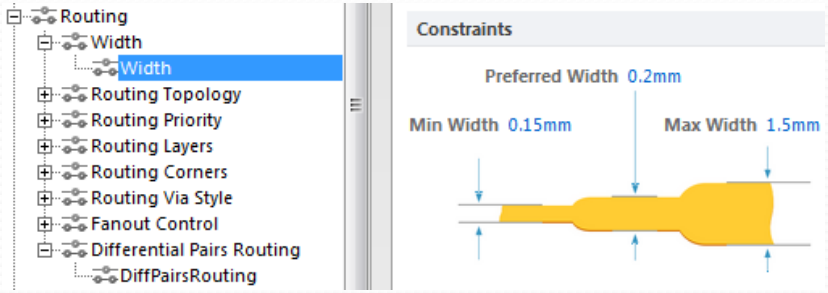
Layer Name	Type	Material	Thickness (mm)
Top Overlay	Overlay		
Top Solder	Solder Mask/Co...	Surface Material	0.01016
Component Side	Signal	Copper	0.03556
Dielectric 1	Dielectric	Core	0.32004
Ground Plane 1 ...	Internal Plane	Copper	0.03599
Dielectric 3	Dielectric	Prepreg	0.127
Inner Layer 1	Signal	Copper	0.03599
Dielectric 6	Dielectric	Core	0.254
Inner Layer 2	Signal	Copper	0.03599
Dielectric 5	Dielectric	Prepreg	0.127
Power Plane (VC...	Internal Plane	Copper	0.03599
Dielectric 4	Dielectric	Core	0.254
Inner Layer 3	Signal	Copper	0.03599
Dielectric 7	Dielectric	Prepreg	0.127
Ground Plane 2 ...	Internal Plane	Copper	0.03599
Dielectric 8	Dielectric	Core	0.254
Solder Side	Signal	Copper	0.03556
Bottom Solder	Solder Mask/Co...	Surface Material	0.01016
Bottom Overlay	Overlay		

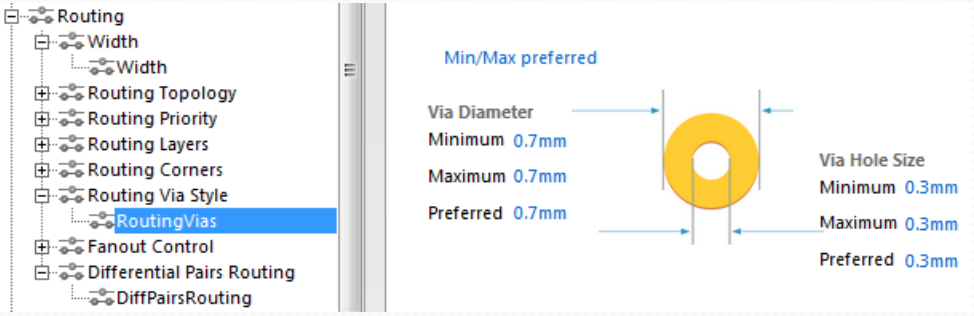
Relocate/move of PCB origin

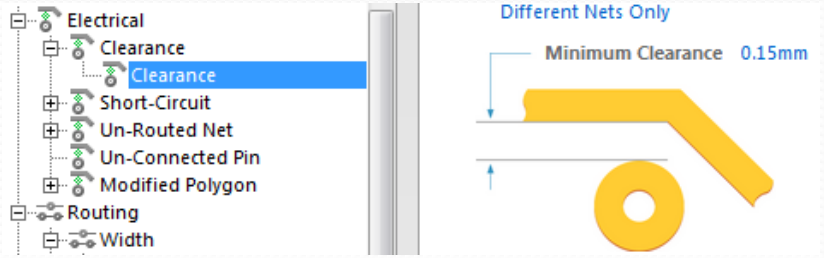




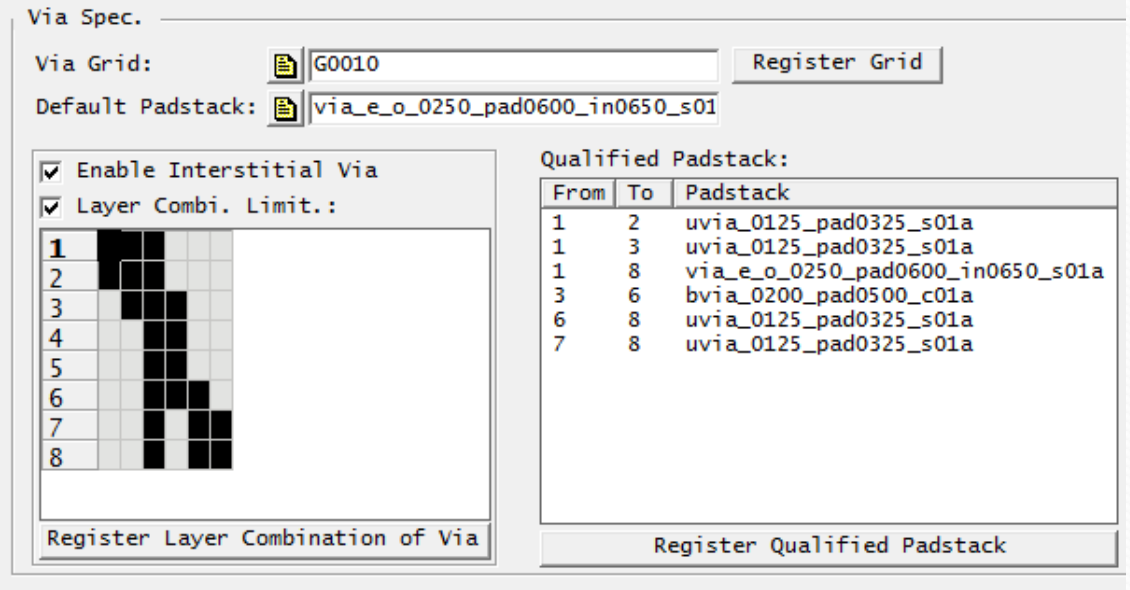
Various rules for trace/clearance dimensions



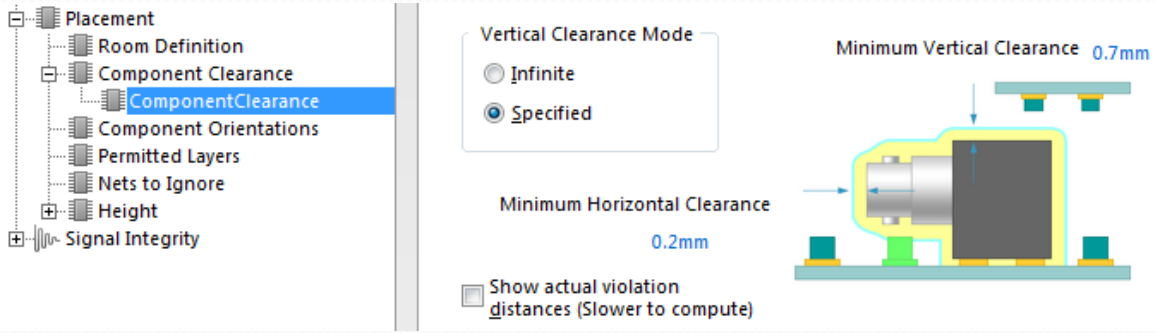


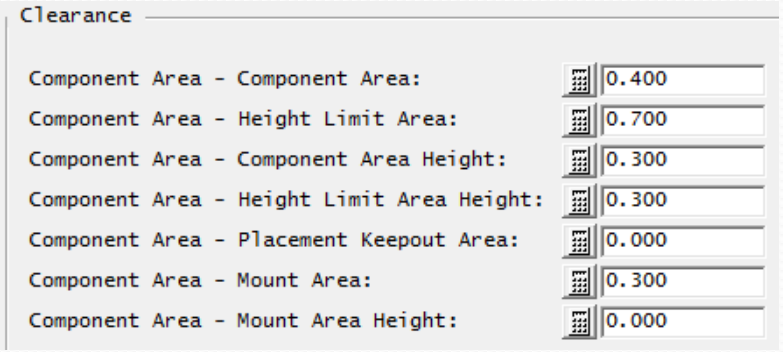


Definition of multiple via types

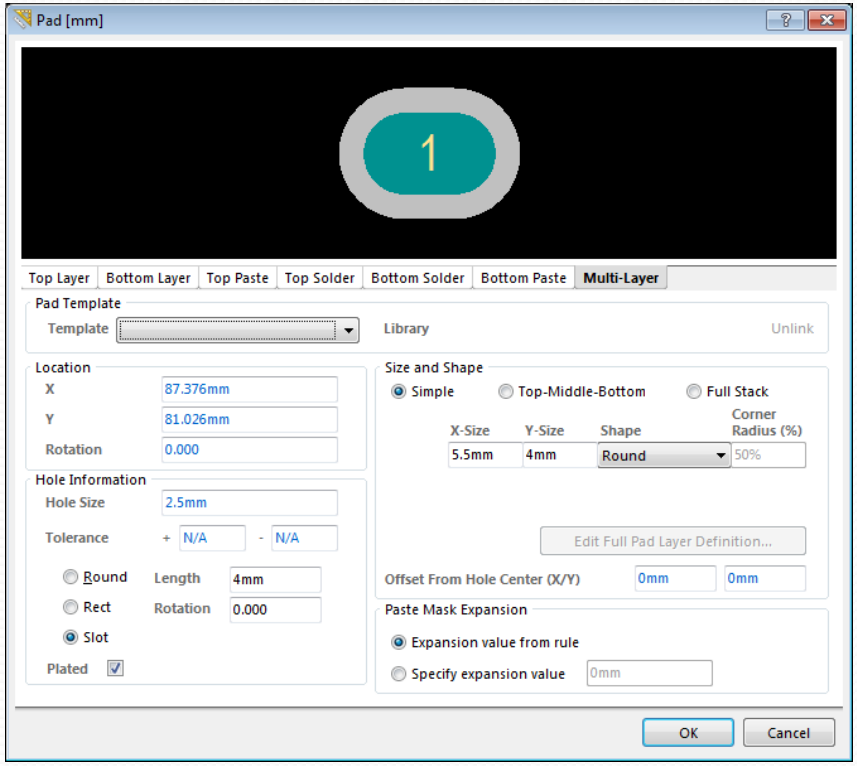


Definition of rules for component clearance

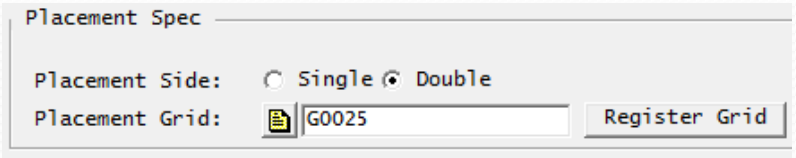


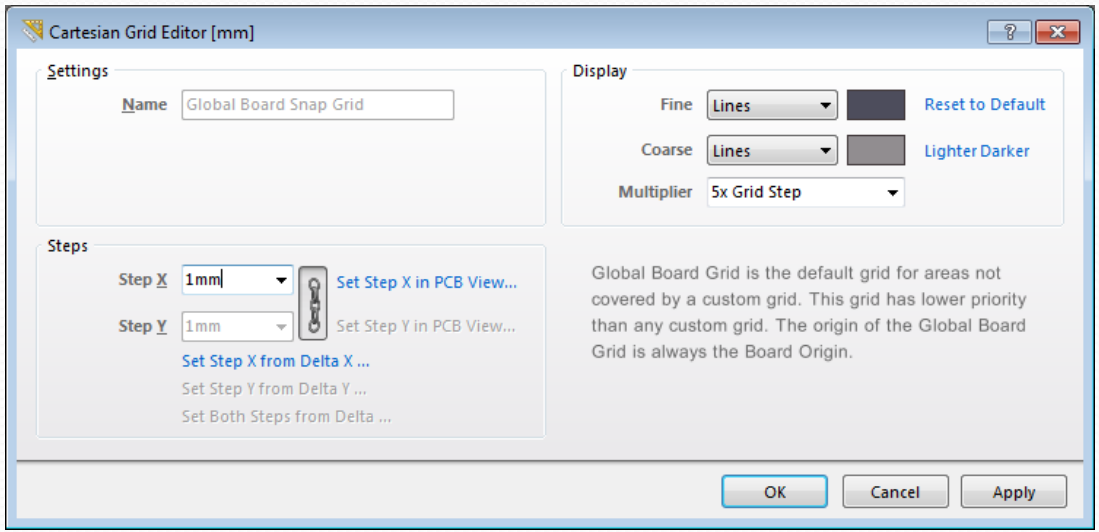


Creation of plated/non-plated slots and non-round holes

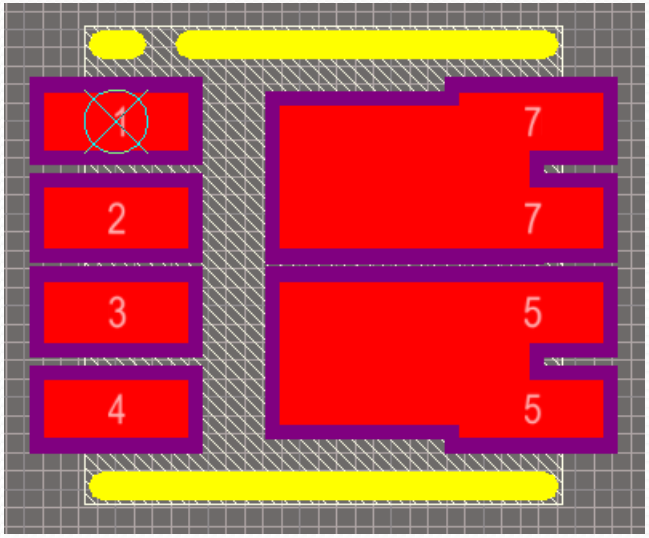


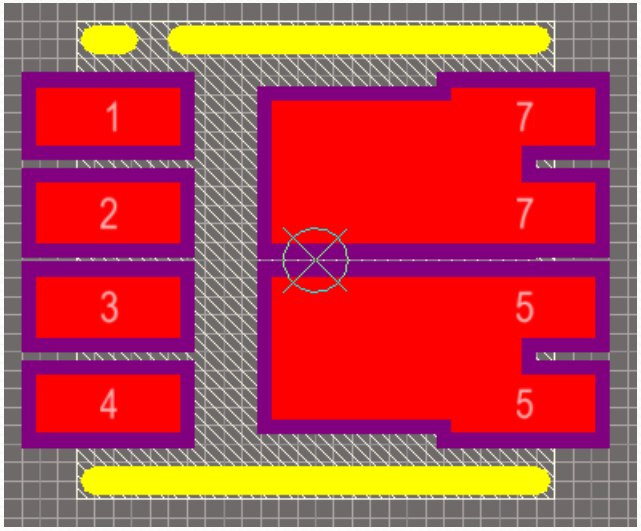
Grid control



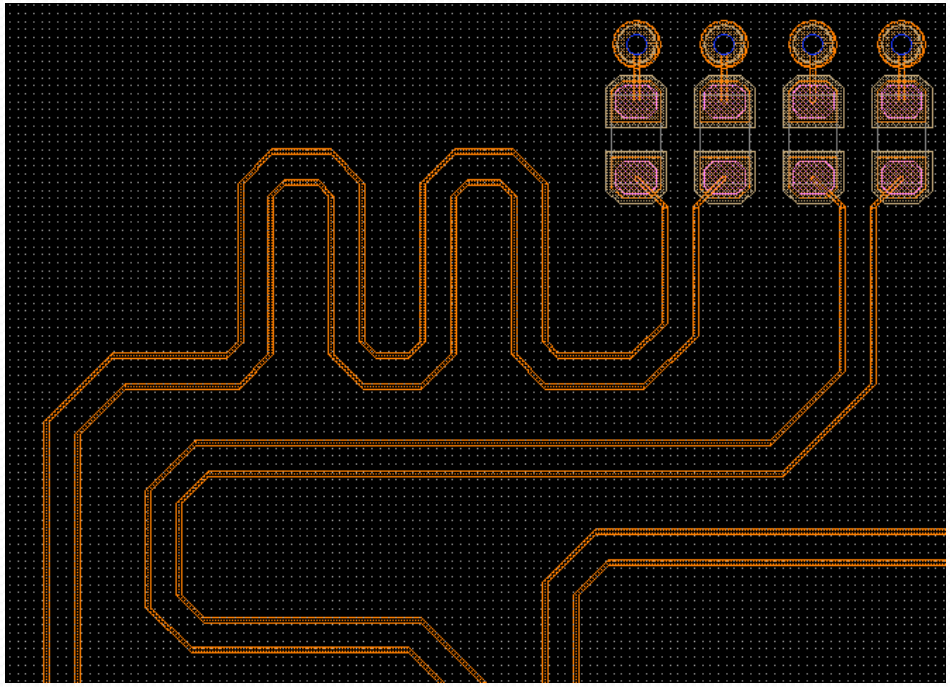


Control on component origin

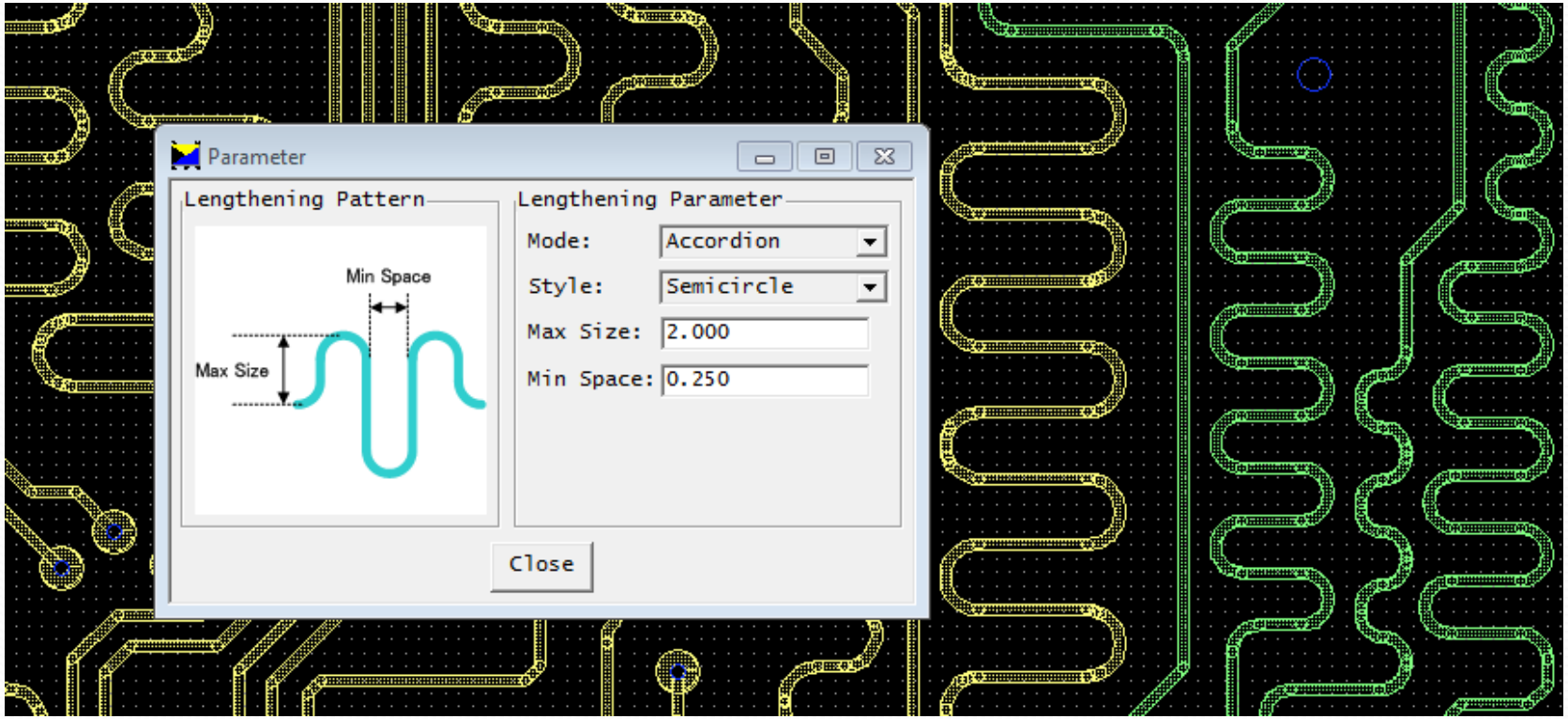




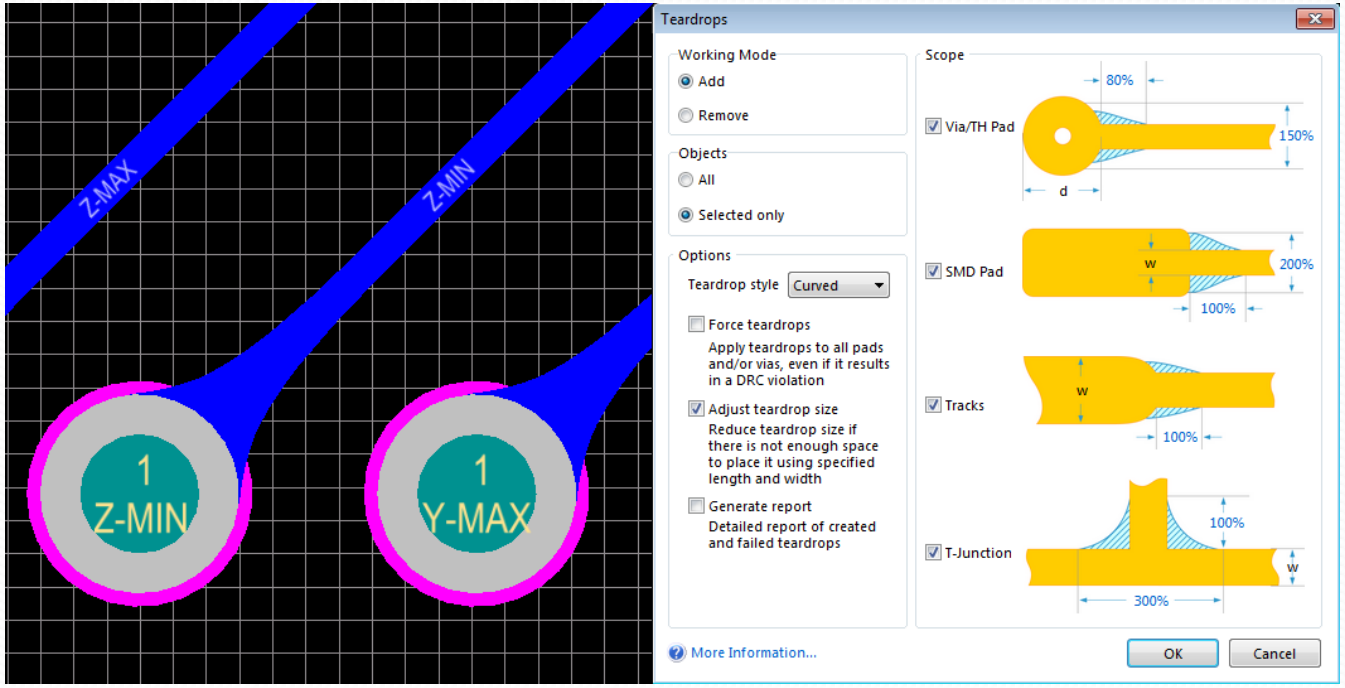
Differential pair routing

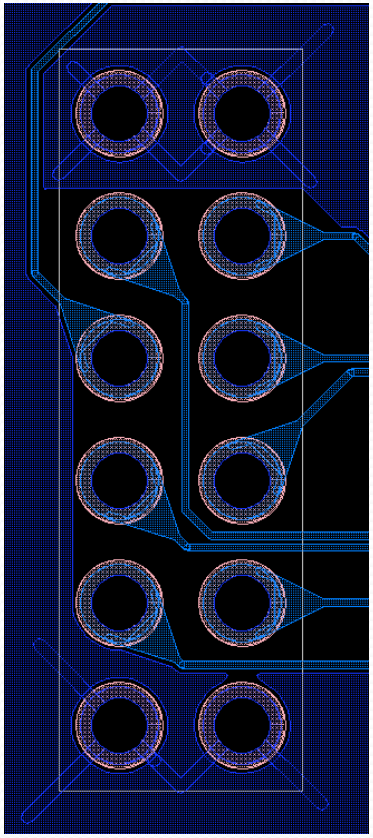


Trace length tuning

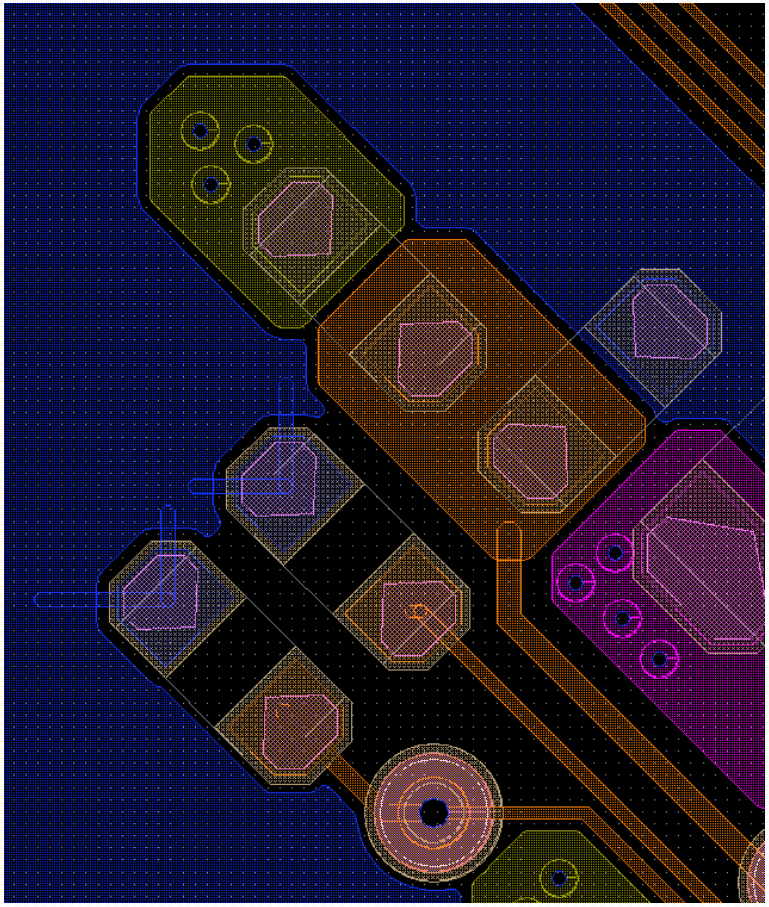


Creation of teardrop (and/or snowman) pads

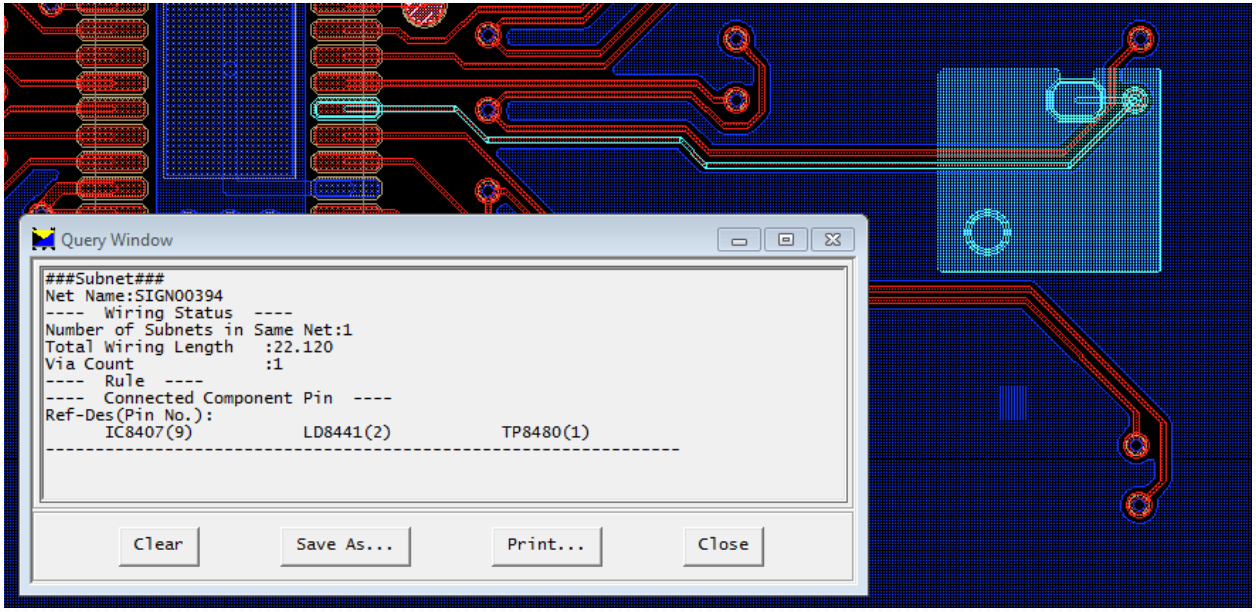




Control of pad – plane connection



Ability to measure the whole length of a trace



Other requirements

- Cross probing (between SCH/SCM and PCB tools);
- Full offline working mode;
- PCB shape support of at least 200x400mm;
- Support for minimum 8 electrical layers (for routing and reference planes);
- Ability to define height restriction areas;
- Import of *DXF* file;
- Ability to create/modify SCH/SCM libraries;
- Ability to create/modify PCB libraries;
- Ability to define differential data lines in SCH/SCM;
- Ability to generate *BOM*, *Gerber* and *ODB* files;
- Ability to generate *Pick & Place* and *Test Point* reports;
- Ability to create Solder Mask openings (text and / or regular shapes);
- Ability to move/place a component to a given position;
- Ability to create keep-out areas (trace keep-out, via keep-out, component keep-out);
- Ability to add a title block (in SCH/SCM & PCB).

Thank you for your attention…

and best of luck to all participants!