What Design Tool to use for TIE Contest?

Tool Requirements for Participation to TIE Professional Student Design Contest

Multiple schematic pages (sheets) in one project



Files Structure			
	<u>Compile PCB Project TIE_demo.PrjPcb</u> <u>Recompile PCB Project TIE_demo.PrjPcb</u> Add <u>N</u> ew to Project	•	Other Ctrl+N
	Add Existing to Project Save Project Save Project As Open Project Documents Hide All In Project Close Project Documents Close Project Explore Regenerate Harness Definitions Show Differences View Channels		Schematic PCB BOM Schematic Library PCB Library Pad Via Library CAM Document Output Job File Database Link File Text Document

Control of schematic formats (ex: A4, A3, A2,...)

Sheet Settings			
Property Size/Zone Grid	1		
Display Sheet Frame		Display Zone	
Display Sheet Frame Color:	•	Display Zone Color:	
Size Table:			
No Alias Xorg Yorg 0 A2 L 0.000 0.00 1 A0 L 0.000 0.00 2 A1 L 0.000 0.00 3 A2 L 0.000 0.00 4 A3 L 0.000 0.00 5 A4 L 0.000 0.00 6 A4 P 0.000 0.00	Xsize 0 594.000 0 1188.000 0 841.000 0 594.000 0 420.000 0 297.000 0 210.000	Ysize Path FrmM 420.000 11 A2DG 841.000 11 A0DG 594.000 11 A1DG 420.000 11 A2DG 297.000 11 A3DG 297.000 11 A4DG	Jame Offse S.smb Manua S.smb Manua S.smb Manua S.smb Manua S.smb Manua S.smb Manua
			P.
🔲 Swap Sheet Frame Symb	ool		
Origin X-Coordinates:	0.000	Offset Mode:	Manual 💌
Origin Y-Coordinates:	0.000	Horizontal Offset:	0.000
Width:	594.000	Vertical Offset:	0.000
Height:	420.000	Horizontal Pitch:	50.000
Sheet Frame Symbol Path:	11 💌	Vertical Pitch:	50.000
C:/CAx/App.	LIB_CR5	Horizontal Start Characte	er: 1
Sheet Frame Symbol Name:		Vertical Start Character:	A
A2DG.smb	Browse	Base Point:	
		OK Cance	I Apply

Options	Grids	Standard Style	
Drientation	Snap 10	Standard styles	A4 🔻
Title Block Standard	Visible 10		
Sheet Number Spaces 4	Electrical Grid	Custom Style	
Show Reference Zones	C Enable	Use Custom style	
Default: Alpha Top to Botton 🔻	Grid Range 4	Custom Width	1500
Show Border		Custom Height	950
Show Template Graphics		X Region Count	6
Jnique Id		Y Region Count	4
KKNFPLFW Reset	Change System Font	Margin Width	20
Border Color			Update From Standard
Sheet Color			
nk To Vault	-		

Support for hierarchical projects





Display/hide component information (ex: value, tolerance, footprint, ...)





Star-point definition



Multi-entity component creation





PDF export

Ente	rprise-AddOns Help		_
	Spacing Class Tools	+	
	Create PDF BLACKandWHITE	•	Circuit
	Create PDF Colored	×	Sheet
	Testpoint Enhancements	+	
	Migrated Designs	+	
	Create/Update Hierarchy Variants		
	Copy Hierarchy Blocks		
	Check Hierarchical Design		
	Attributes Manager		
	Create Adjustment Testpoints		
	Change Parts	+	
	Cleanup Properties	+	····\$····

imart PDF
Choose Export Target Smart PDF can export the currently viewed document or the entire project.
Smart PDF can export the currently viewed document or documents in the current project.
Current Project (
Current Document (Sheet1.SchDoc)
Output File Name: \Sheet1.pdf
<u>C</u> ancel < <u>B</u> ack <u>N</u> ext > <u>F</u> inish

Creation of complex PCB shapes (ex: rounded corners, cutouts)



Stack-up definition (number of layers, copper thickness, dielectric type, core / prepreg thickness, etc.)

Material:	FR-4			
Layer Construction				
Core Layer: From	∰ 4 To ∰ 5			
Lay.	Layer thickne…	Material		
Resist LayerA	0.025	Probimer 65		
Conductor1	0.043	Copper		
Insulating1-2	0.073	FR-4		
Conductor 2	0.043	Copper		
Insulating2-3	0.110	FR-4		
Conductor 3	0.037	Copper		
Insulating3-4	0.254	FR-4		
Conductor4	0.035	Copper		
Insulating4-5	0.350	FR-4		
Conductor 5	0.035	Copper		
Insulating5-6	0.254	FR-4		
Conductor6	0.037	Copper		
Insulating6-7	0.110	FR-4		
Conductor7	0.043	Copper		
Insulating7-8	0.073	FR-4		
Conductor8	0.043	Copper		
Resist LayerB	0.025	Probimer 65		

7
7

	Layer Name	Туре	Material	Thickness (mm)
V	Top Overlay	Overlay		
V	Top Solder	Solder Mask/Co	Surface Material	0.01016
1	Component Side	Signal	Copper	0.03556
1	Dielectric 1	Dielectric	Core	0.32004
1	Ground Plane 1	Internal Plane	Copper	0.03599
V	Dielectric 3	Dielectric	Prepreg	0.127
1	Inner Layer 1	Signal	Copper	0.03599
1	Dielectric 6	Dielectric	Core	0.254
1	Inner Layer 2	Signal	Copper	0.03599
1	Dielectric 5	Dielectric	Prepreg	0.127
1	Power Plane (VC	Internal Plane	Copper	0.03599
1	Dielectric 4	Dielectric	Core	0.254
1	Inner Layer 3	Signal	Copper	0.03599
V	Dielectric 7	Dielectric	Prepreg	0.127
V	Ground Plane 2	Internal Plane	Copper	0.03599
1	Dielectric 8	Dielectric	Core	0.254
1	Solder Side	Signal	Copper	0.03556
V	Bottom Solder	Solder Mask/Co	Surface Material	0.01016
V	Bottom Overlay	Overlay		

Relocate/move of PCB origin

Envi	Ronment	Utilities	Divide	Check	Cc
	Grid Setti	ngs			
	Via Grid				•
	Change G	irid			
✓	Non-elect	trical Com	p Selecti	on	
	Toolbar				
	Repositio	n Panel			
	Net-less [Design Mo	de		
	Shielding	Mode			
•	Auto Secu	urity Copy			
	Paramete	r Resource	:		۲
	Move Ori	gin			
	Option				
	Customiz	e			
	Library Lo	ad/Unloa	d		

<u>E</u> dit	<u>V</u> iew Proje <u>c</u> t	<u>P</u> lace <u>D</u> es	ign	<u>T</u> o	ols	<u>A</u> uto F
4	<u>U</u> ndo	Ctrl+Z		6 1	1	8
P	Nothing to Redo	Ctrl+Y		Doc		i
*	Cu <u>t</u>	Ctrl+X				
Þ	<u>C</u> opy	Ctrl+C				
	Copy As Text					
2	<u>P</u> aste	Ctrl+V				
	P <u>a</u> ste Special					
2	Paste Text					
	Clear	Del				
	<u>S</u> elect		•			
	D <u>e</u> Select		•			
	<u>D</u> elete					
ð	Rub <u>b</u> er Stamp	Ctrl+R				
	C <u>h</u> ange					
	Slice Trac <u>k</u> s					
	Move		•			
	Align		×			
	<u>O</u> rigin		•	¢.	<u>S</u> et	
	Jump		۲		<u>R</u> es	et
	Selection Memory					
₹.	Build Query	Shift+B				
Q	Fi <u>n</u> d Similar Object	s Shift+F				

Various rules for trace/clearance dimensions



Definition of multiple via types

Via Spec.	
Via Grid: GO010 Default Padstack: Via_e_o_0250_pad	Register Grid
<pre>✓ Enable Interstitial Via ✓ Layer Combi. Limit.: 1 2 3 4 5 6 7 8 8</pre>	Qualified Padstack: From To Padstack 1 2 uvia_0125_pad0325_s01a 1 3 uvia_0125_pad0325_s01a 1 8 via_e_o_0250_pad0600_in0650_s01a 3 6 bvia_0200_pad0500_c01a 6 8 uvia_0125_pad0325_s01a 7 8 uvia_0125_pad0325_s01a
Register Layer Combination of Via	Register Qualified Padstack

Definition of rules for component clearance



Clearance	
Component Area - Component Area:	0.400
Component Area - Height Limit Area:	0.700
Component Area - Component Area Height:	0.300
Component Area - Height Limit Area Height:	0.300
Component Area - Placement Keepout Area:	0.000
Component Area - Mount Area:	0.300
Component Area - Mount Area Height:	0.000

Creation of plated/non-plated slots and non-round holes

				1				
Top Layer Botton	Layer Top	Paste Top S	older	Bottom Sol	der Botto	om Paste	Multi-Layer	
Pad Template			•	Library				Unlink
Location				Size and	Shape			
х	87.376mm			Simple				Full Stack
Y	81.026mm				Y-Size	V-Size	Shane	Corner Padius (%)
Rotation	0.000				5.5mm	4mm	Round	▼ 50%
Hole Information								
Hole Size	2.5mm							
Tolerance	+ N/A	- N/A				E	dit Full Pad Laye	r Definition
© <u>R</u> ound	Length	4mm		Offset Fro	om Hole Ce	enter (X/Y)	0mm	Omm
Rect	Rotation	0.000		Paste Ma	sk Expansio	on		
Slot			Evnar	osion value	from rule			
Plated V								
Plated V								

Grid control

Placeme	ent Spec —		
Placem Placem	ent Side: ent Grid:	C Single ⊙ Double ■ G0025	e Register Grid
iring Width Stack	: 🗈 w	5_0100	Register Wiring Width Stack
iring Grid:	🛅 G0	025	Register Grid

<u>S</u> ettings		Display		
<u>N</u> ame	Global Board Snap Grid	Fine	Lines 🔹	Reset to Default
		Coarse	Lines 🔻	Lighter Darker
		Multiplier	5x Grid Step	•
Steps Step <u>X</u> Step <u>Y</u>	Imm Set Step X in PCB View Imm Set Step Y in PCB View Set Step X from Delta X Set Step Y from Delta Y Set Both Steps from Delta Set Step X from Delta	Global Board Grid is the default grid for areas not covered by a custom grid. This grid has lower priority than any custom grid. The origin of the Global Board Grid is always the Board Origin.		

Control on component origin





Differential pair routing



Trace length tuning

Parameter			
Lengthening Pattern Min Space	Lengthening Parameter Mode: Accordion Style: Semicircle Max Size: 2.000		
Max Size	Min Space: 0.250		
	Close		

Creation of teardrop (and/or snowman) pads





Control of pad – plane connection



Ability to measure the whole length of a trace

Query Window ###Subnet### Net Name:SIGN00394 Wiring Status Rule cont Rule Rule Rule Rule Rule Connected Component Pin Ref-Des (Pin No.): IC8407(9) LD8441(2) TP8480(1)	
Clear Save As Print Close	

Other requirements

- Cross probing (between SCH/SCM and PCB tools);
- Full offline working mode;
- PCB shape support of at least 200x400mm;
- Support for minimum 8 electrical layers (for routing and reference planes);
- Ability to define height restriction areas;
- Import of *DXF* file;
- Ability to create/modify SCH/SCM libraries;
- Ability to create/modify PCB libraries;
- Ability to define differential data lines in SCH/SCM;
- Ability to generate BOM, Gerber and ODB files;
- Ability to generate Pick & Place and Test Point reports;
- Ability to create Solder Mask openings (text and / or regular shapes);
- Ability to move/place a component to a given position;
- Ability to create keep-out areas (trace keep-out, via keep-out, component keep-out);
- Ability to add a title block (in SCH/SCM & PCB).

Thank you for your attention...

and best of luck to all participants!