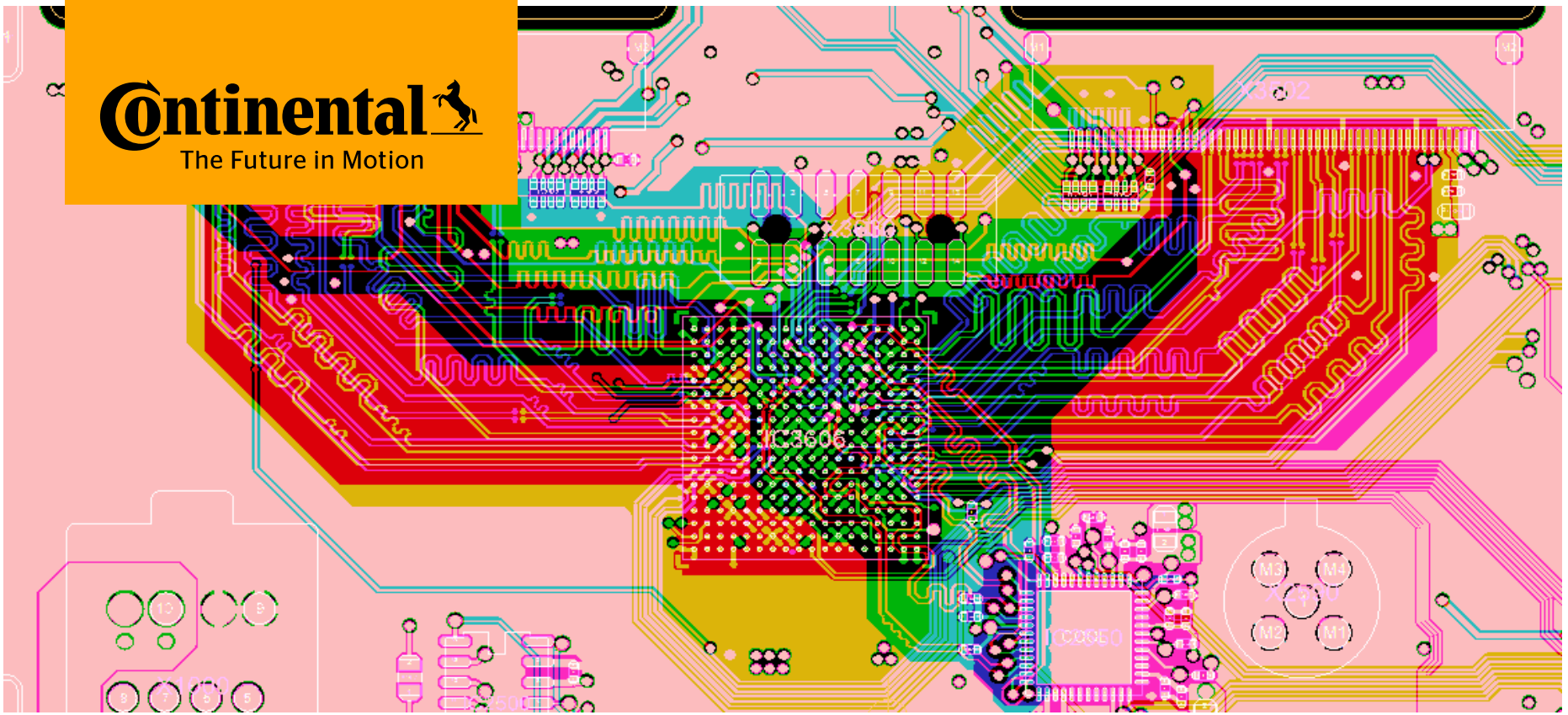


TIE Plus.

The step towards interconnect simulation technology

Catalin Negrea, Ph. D.
SI/PI &Thermal Management Lead Engineer
Continental Automotive, Interior Division

Agenda

1. The need for virtual prototyping
2. TIE Plus definition and objectives
3. Why signal integrity ?
4. SI Design & Simulation Flow
5. Field solvers and SI simulation software
6. TIEplus 2015 review
7. TIEplus 2017 fresh review + some words on power integrity
8. Contest topics and recommended bibliography
9. Contest workflow

Electronic market trends

- The trends are set by the smartphone/tablet product segment
- This means that sooner or latter all other devices with a “commercial” destination will follow. This all especially true for automotive.
- These trends imply usage of
  - ⇉ high resolution displays
  - ⇉ high speed connectivity + IoT (always connected, Internet of Things integration)
  - ⇉ miniaturization

VW - Concept Car “Budd-e” ← Presented at CES2016 → **Corning - Cockpit Study**

Electronic market trends

› Eventually even devices with very simple functions become…..

… A Tablet

In 2011 Samsung launched the
Refrigerator with Twitter on an 8” LCD

In 2016 Samsung launched the
Refrigerator with “fridge commerce” on an 21.5” LCD

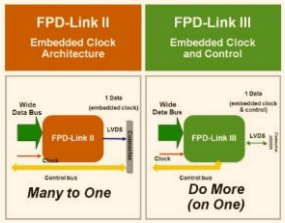
Today’s electronic market drivers

Technologies

ddr3 A JEDEC STANDARD

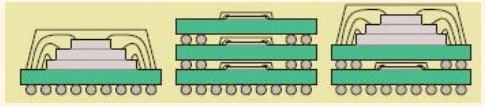
DDR4

3D Graphical Processors



High-Speed Serial Links

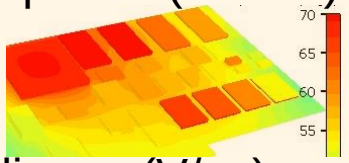
Wireless Data transfer



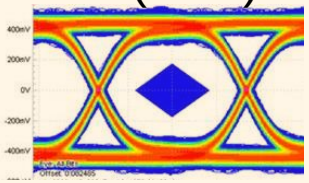
Packaging Technologies (SiP, SoC)

Challenges

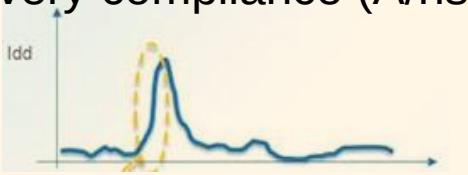
- thermal dissipation (W/cm^2)



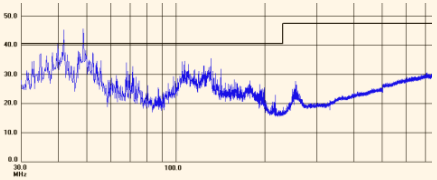
- signal compliance (V/ns)



- power delivery compliance (A/ns)

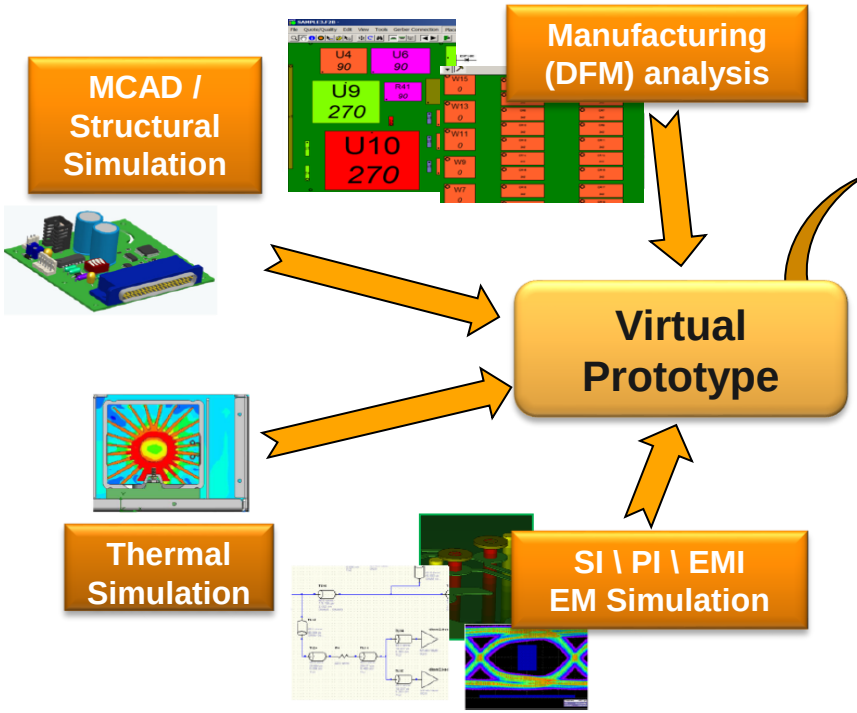


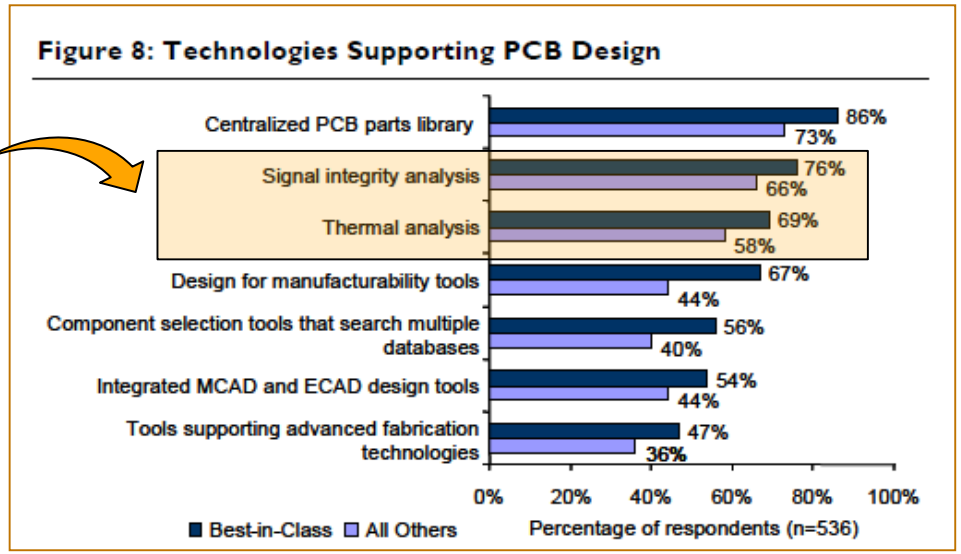
- EM compatibility (dBuV/m)



Virtual Prototyping

› Virtual prototyping = the usage of computer based modeling and simulation techniques for the definition of a multidisciplinary model of the device under development (with the goal of predicting physical behavior in different use cases)





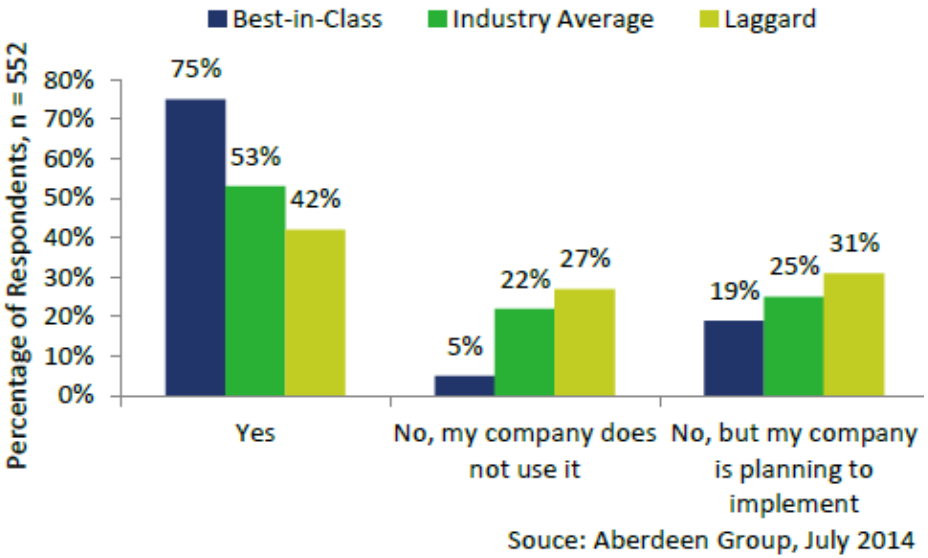
Source: Aberdeen Group Market Study "Why PCB Design Matters to the Executive", Feb. 2010

› "Ideal world" goal → Get it right the first time !

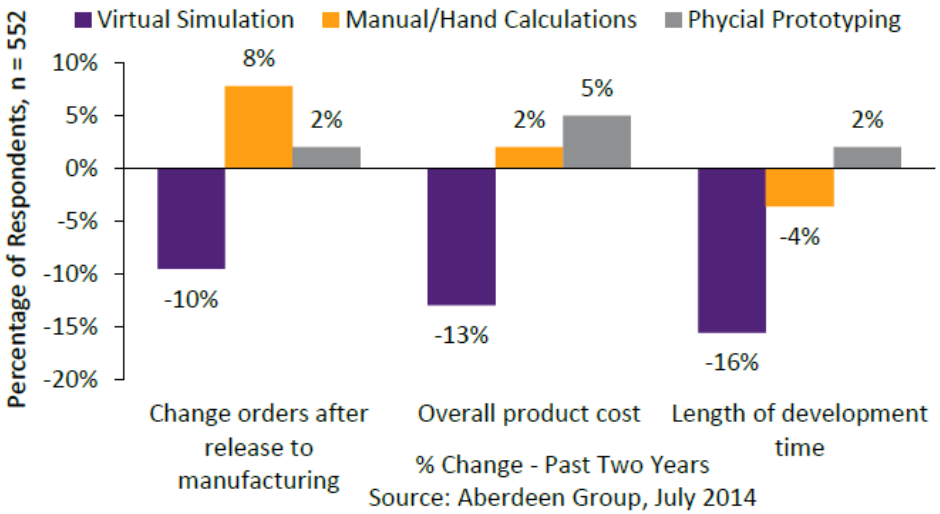
› "Real R&D world" goal → Reduce number of design loops, prototype costs, development time

Virtual prototyping impact

Are companies turning to virtual prototyping ?



Impact of virtual prototyping on design metrics



- 75% best-in-class companies report using virtual prototyping consistently and only 5% do not consider implementing this in the future
- A 16% percent decrease total development was observed as a consequence of a simulation driven design flow
- a total cost decrease of 13% was observed
- 48% of respondents reported a decrease in the number of physical prototypes
- 31% of respondents identified that problem root cause identification time would be significantly without the use of simulation tools

** Aberdeen Group: The Value of virtual simulation versus traditional methods, December, 2014*

TIE Plus Objectives

- TIE Plus = a new contest challenge under the TIE brand, dedicated to virtual prototyping disciplines that support high-complexity PCB design
- Objectives:
  - Promoting simulation based PCB design disciplines in universities and R&D centers
  - Stimulating the development of future specialist in the field of interconnect simulation in a accordance to best-in-class companies demands
  - Create a collaborative-competitive environment where the contestants presents their technical solutions, but also exchange ideas on simulation approaches and get in touch other PCB design professionals
- Subject topics for upcoming editions of TIE plus:
  - Signal Integrity (SI) -> simulations for signal integrity associated with wired data transmissions at PCB and system level
  - Power Integrity (PI) -> simulation power supply distribution networks in high frequency digital applications

Why SI & PI as primary topics for TIE Plus?

Job add from Mentor Graphics

Senior Hardware Engineer - 4231

Mentor® A Siemens Business

Req ID: 4231

Work Location: RO - Bucharest

Description

Company: Mentor Graphics
Job Title: Senior Hardware Engineer - 4231 Job Location: Romania - Bucharest Job Category: R&D/Hardware Engineering

Job Qualifications

The successful candidate will possess the following combination of education and experience:

- Bachelor or Master degree in electrical / electronic engineering or related discipline
- Experience in concept definition and circuitry design of digital and analog electronics ideally for automotive applications
- Experience with CAD tools for schematic design and for support of layout design
- Experience in simulation technology for electronic circuitry design
- Experience in optimization of electronic circuits with regards to EMC/EMI, signal integrity and performance
- Experience in testing and qualification as well as in industrialization of electronic modules and complete devices
- Strong team player with good spoken and written communication skills in English

Job add from Tesla

Description

Signal Integrity Engineer

Job Summary

TESLA MOTORS

We are hiring a Signal Integrity/Power Integrity Engineer at Tesla. You will be responsible for high-speed serial interface signal integrity, and/or DDR SI/PI co-design, and/or core power integrity for automotive electronic systems, e.g., auto pilot, infotainment, camera system etc. You will develop and execute test plans to validate signal and power integrity. You will work with design engineers and vendors to debug and optimize the system designs including PCB, package, cable harness, circuit design etc.

Key Qualifications

- MSEE/Ph.D with 5+ years of relevant actual product design analysis experience
- Prior design and modeling experience with high speed interfaces, and/or DDR, and/or high power core power integrity analysis is a must.
- Familiar with lab equipment, such as scope, TDR, VNA, spectrum analyzer etc, and lab correlation/validation of the simulation results
- Strong hands-on skills in debug and simulation lad validation
- Solid understanding of transmission line theory, electromagnetic theory and/or power delivery network knowledge.
- Good communication skills

Job add from Micron

PCB Layout Designer

Date: Apr 10, 2017
Location: Boise, ID, US

Req Id: 67881
Printed Circuit Board Layout Designer

Micron MICRON TECHNOLOGY, INC.
INCORPORATED UNDER THE LAWS OF THE STATE OF DELAWARE

Qualifications

Strong skills in manual and interactive component placement & routing
Thorough knowledge of layout techniques related to signal integrity.
Advanced knowledge of PCB manufacturing processes.
Familiar with electronic schematic graphic symbols and reference designation standards
Knowledgeable in PCB layout guidelines and standards
Ability to read and interpret component datasheets, schematics, and design-related documents to extract pertinent information to follow specified layout guidelines.

What is high speed ?

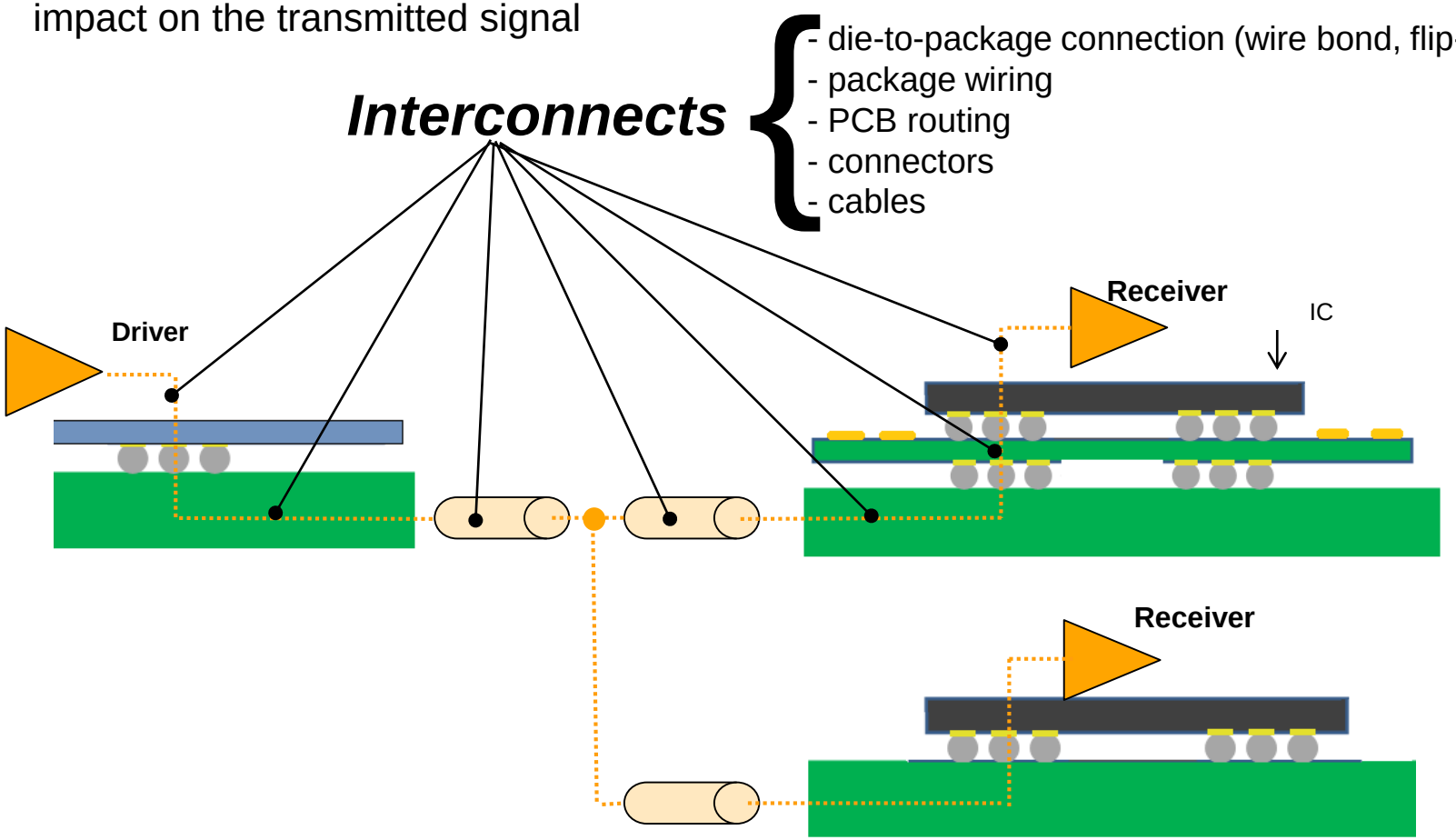
- As the variation speed of electric signals increases, physical properties of the interconnect structures can induce unwanted signal distortion
- Due to the need of high data rates (implying high frequency), the signal's rise&fall times become smaller and smaller (for DDR interfaces tr~0.2-1 ns)
- The interconnect path can be no longer modeled as an RLC structure, but as a transmission line with a electrical behavior described by the telegraphers equations

- The following items fall in to the high speed domain and must be considered in the analysis:
  - interconnect reflections
  - losses due to skin effect
  - crosstalk (near end and far end)
  - interconnect timing delays
  - IC package parasitics
  - IC driver\receiver circuit characteristics

Rise time evolution	
TTL:	100ns-0.5ns
CMOS logic:	30ns-0.3ns
ECL gates:	3ns-0.2ns
Gbit SerDes:	0.8ns-10ps

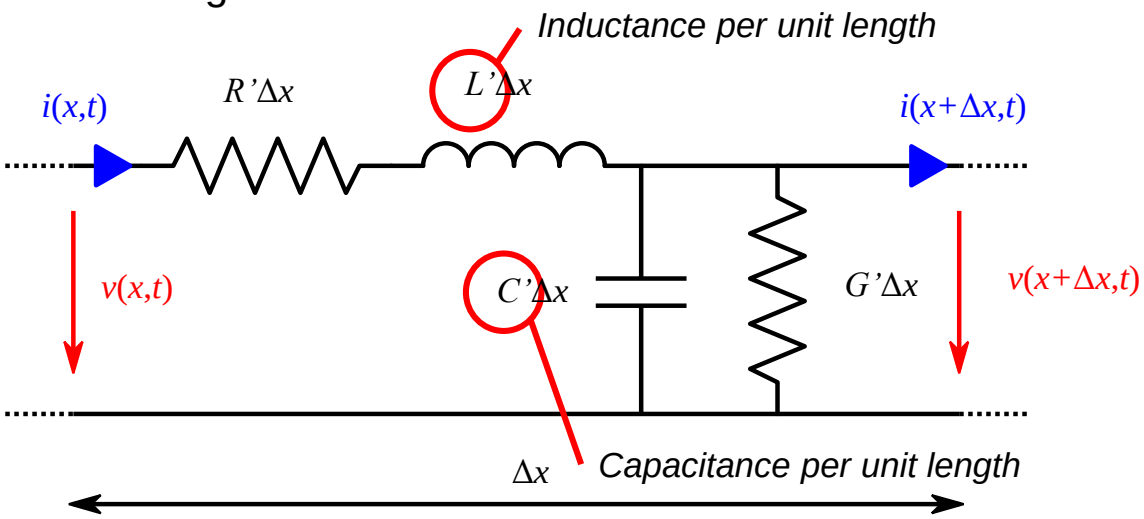
What can be considered an interconnect ?

› Every electrical connection element placed in the signal path is a potential source for signal degradation and its electrical behavior must be characterized in order evaluate the impact on the transmitted signal

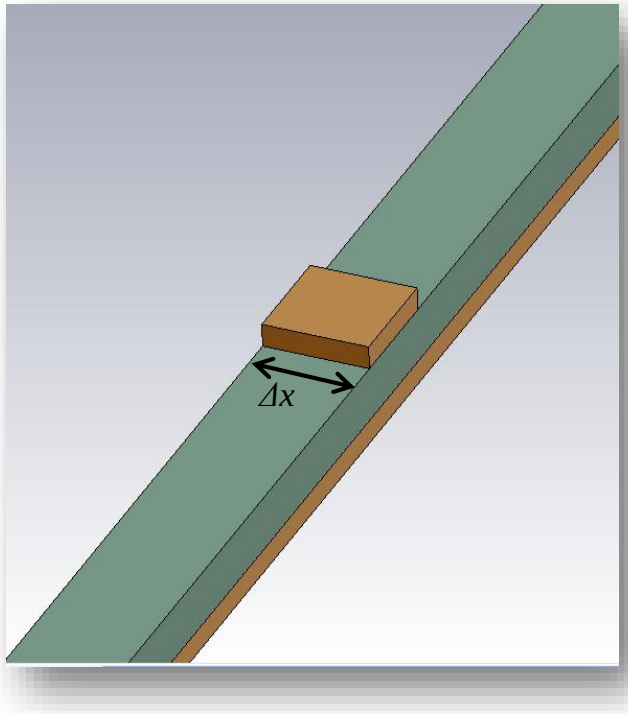


What is a transmission line?

- (At least) two parameters determine a transmission line
  - Propagation speed
  - Characteristic impedance Z_L
- A transmission line can be cut in short pieces having the length Δx:



Transmission Line RLCG segment



What is high speed ?

When do these effects become critical? Rule of thumb (for FR4):

$$l_{max} / \text{inch} < t_r / \text{ns}$$

$$l_{max}(mm) <\sim 25 \times t_r(\text{ns})$$

**Source: Eric Bogatin, Signal and Power Integrity – Simplified, Prentice Hall, 2004*

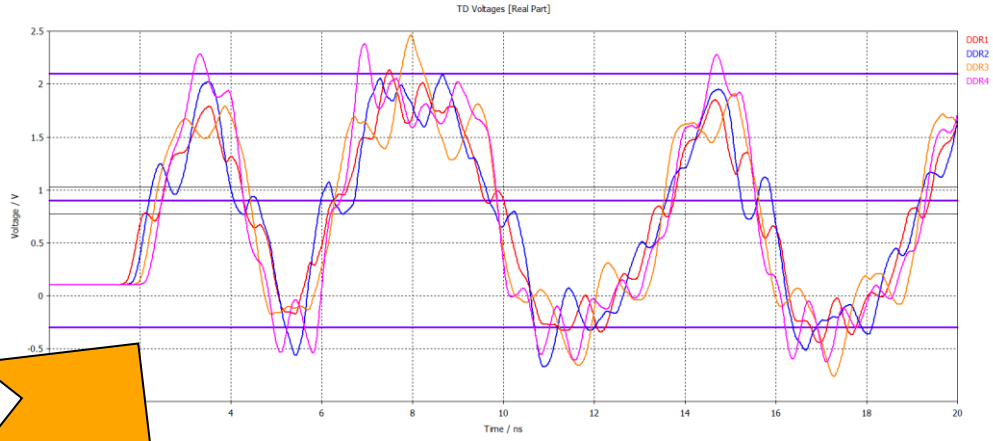
…so for a 25mm trace length, a signal with a rise time < 1ns (for 3.3V logic this would mean ~2V/ns) creates already a SI risk if the interconnect is not properly designed

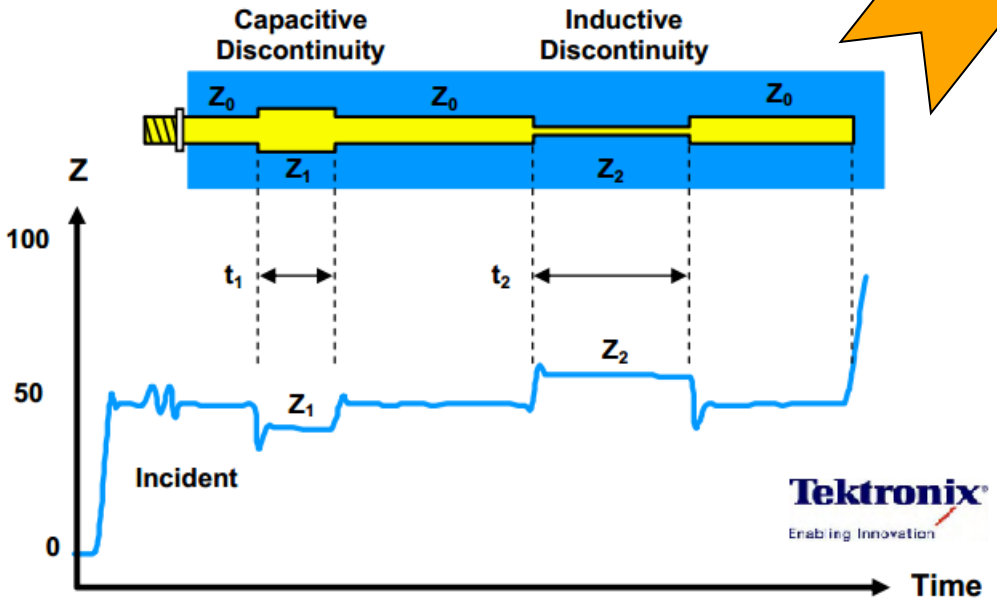
› and properly designed for SI means <u>impedance matching at circuit level</u>

The term "high speed" indicates an unhappy combination of interconnect length and variation speed

Impedance Discontinuities

Changes in interconnect impedance over the signal transmission path will cause distortion depending on driver characteristics (every IC I/O has a non-linear impedance curve) and interconnect discontinuity characteristics.



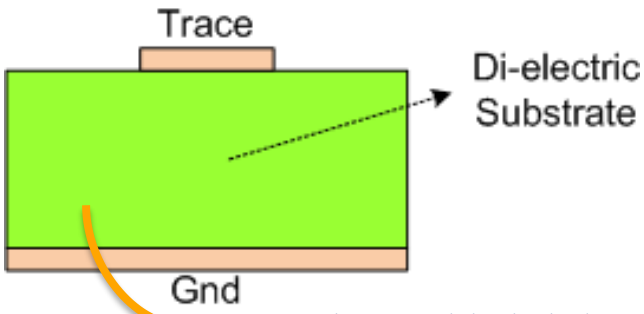


Impedance discontinuities have consequences:

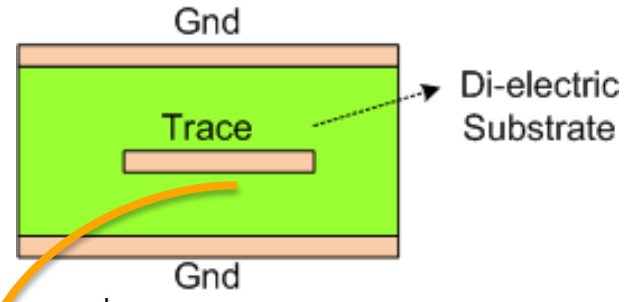
- overshoot \ undershoot
- reflections in the triggering region
- false logic triggering
- interconnect added jitter
- timing deviations

Controlled Impedance Routing

Microstrip



Stripline



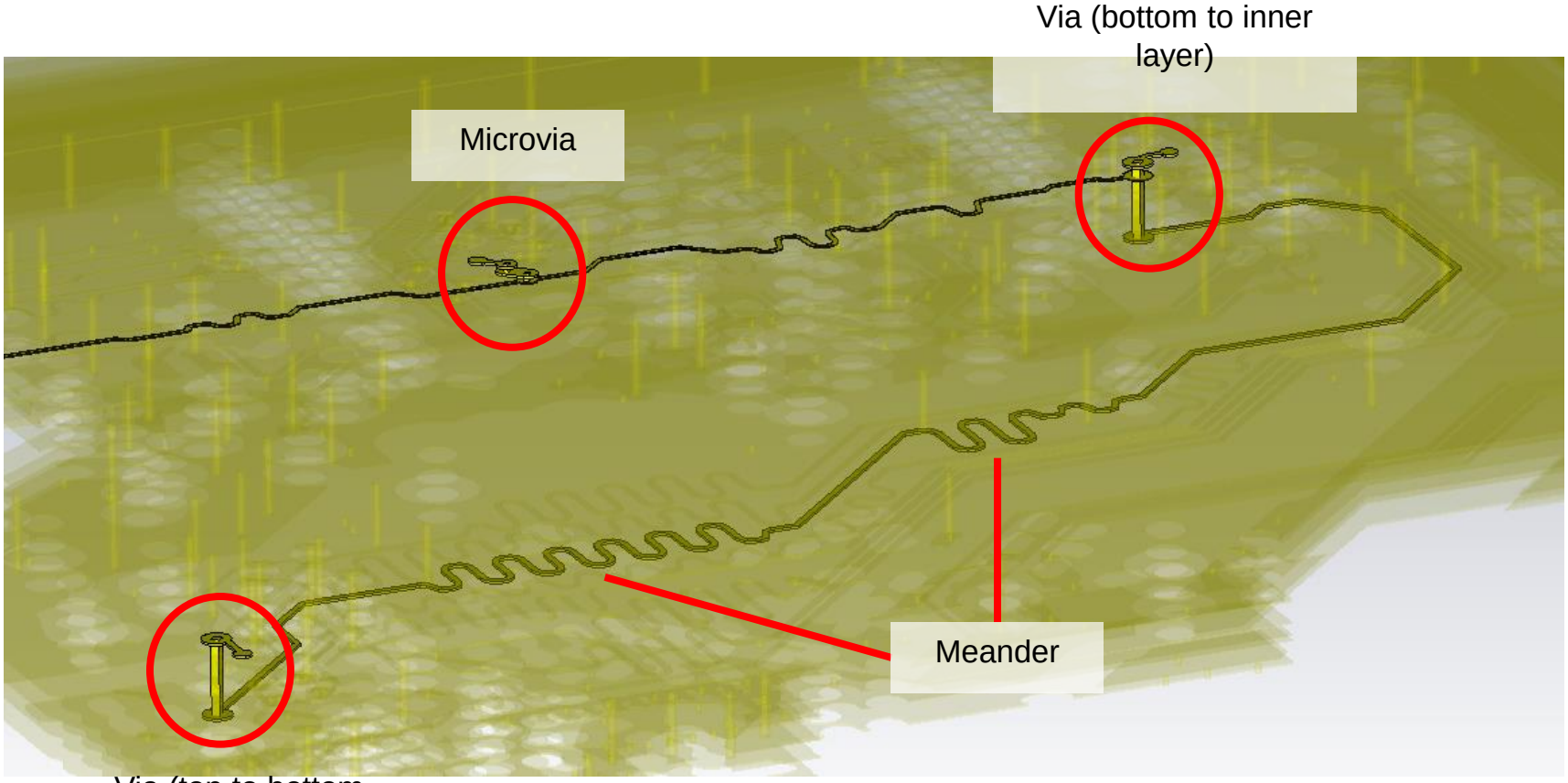
GENERIC PCB Spec

		Thickness [um]	Type
		25	Solder Mask
Signal	1	18+25 min	Base Copper + plating
		65	Prepreg 1080 or 1067
GND	2	18	Base Copper
		100	CORE
Signal	3	18	Base Copper
		100	Prepreg 2116
GND	4	18	Base Copper
		890	CORE
1V5	5	18	Base Copper
		100	Prepreg 2116
Signal	6	18	Base Copper
		100	CORE
GND	7	18	Base Copper
		65	Prepreg 1080 or 1067
Signal	8	18+25 min	Base Copper + plating
		25	Solder Mask
		1553	

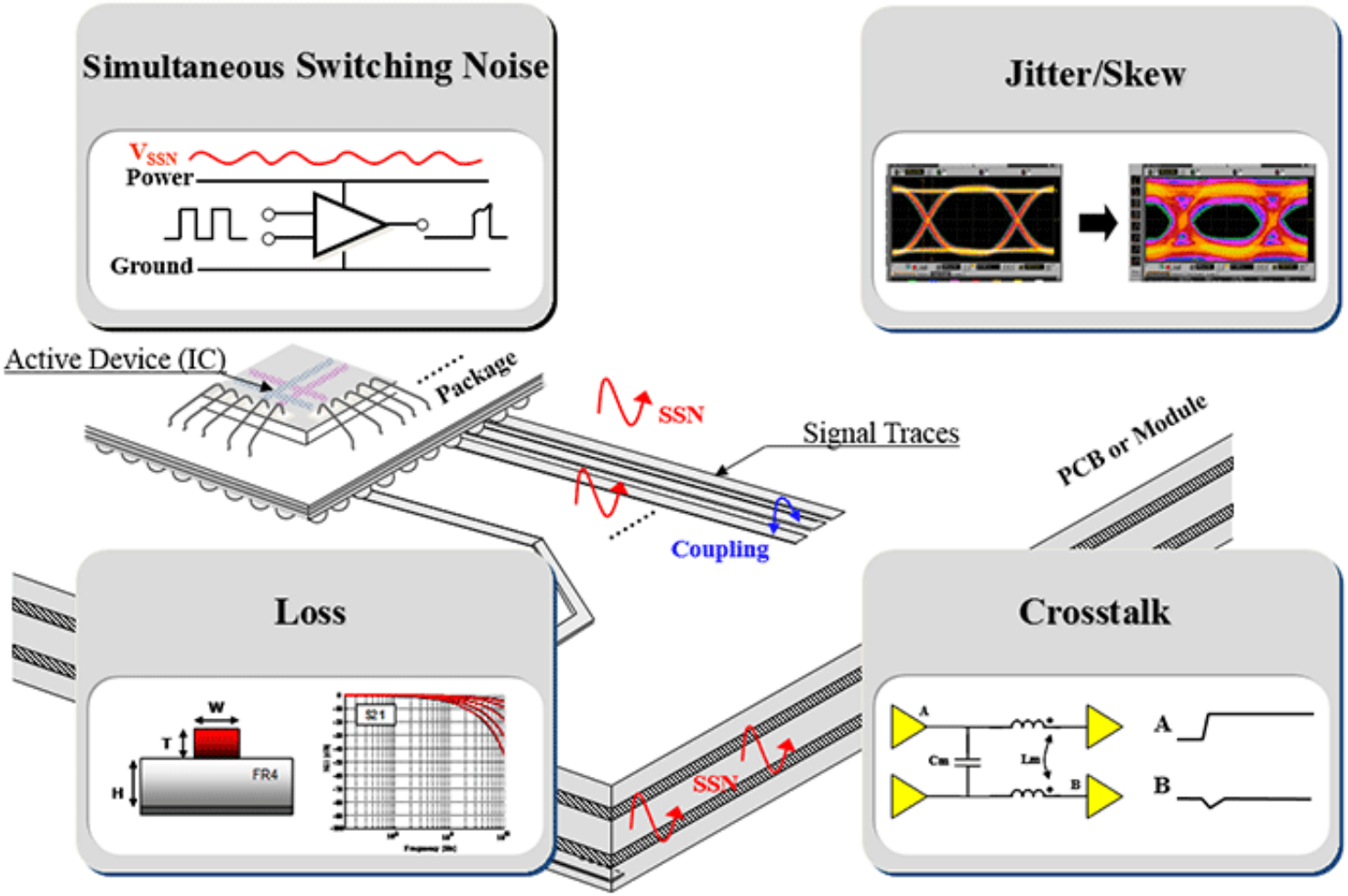
… does not solve everything

But some things can not be avoided …….

› Reality may look something like this



….and there are some additional EM effects



SI \ PI Workflow

Problem Formulation

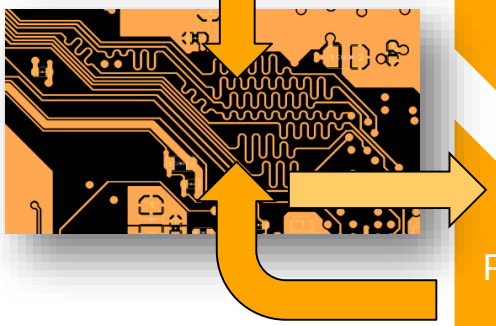
- evaluate of system\ interface requirements
- define design targets
- define modeling approach

Pre-layout Analysis

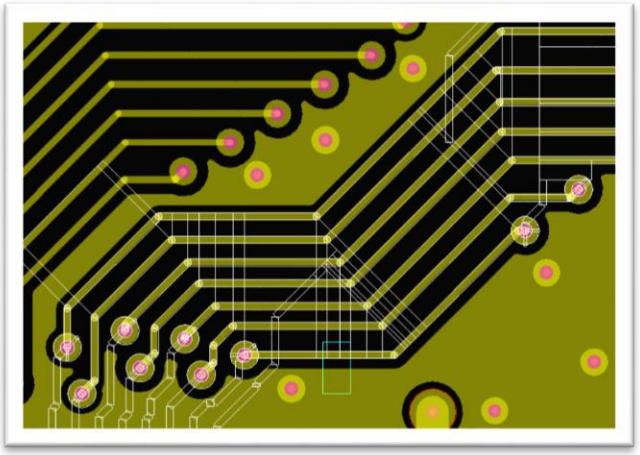
- define PCB stack-up (layers, materials)
- “what-if” simulations – explore design possibilities in order to meet interface requirements, obtain best performance/cost ratio

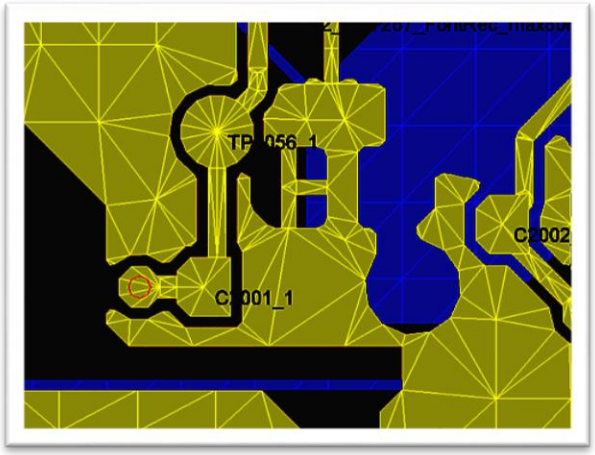
Post-layout Analysis

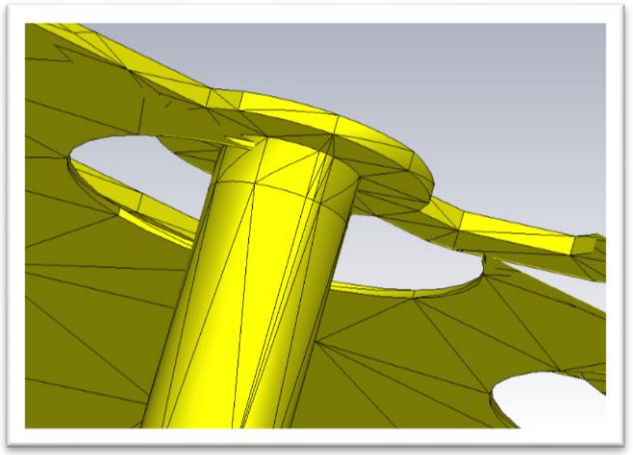
- PCB stack-up and CAD represent the inputs for the simulation
- Identify potential problems that were not considered in pre-layout
- debugging of a physical prototype problem; identify root cause and define possible remedies



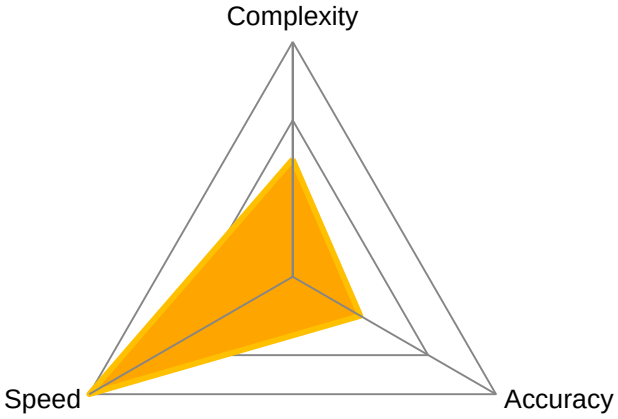
Interconnect extraction techniques



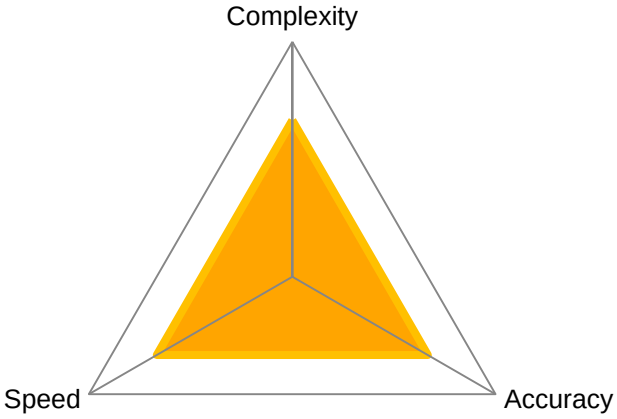




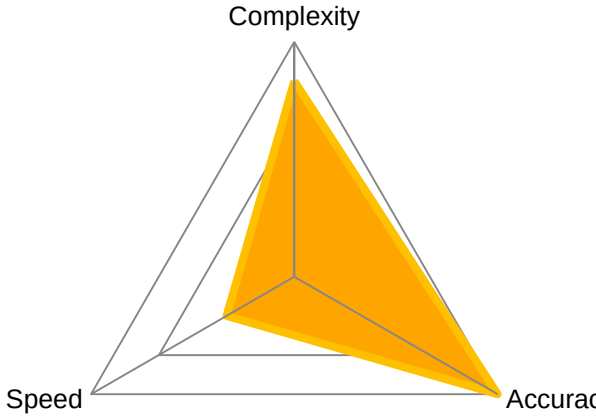
Transmission lines (sectional)



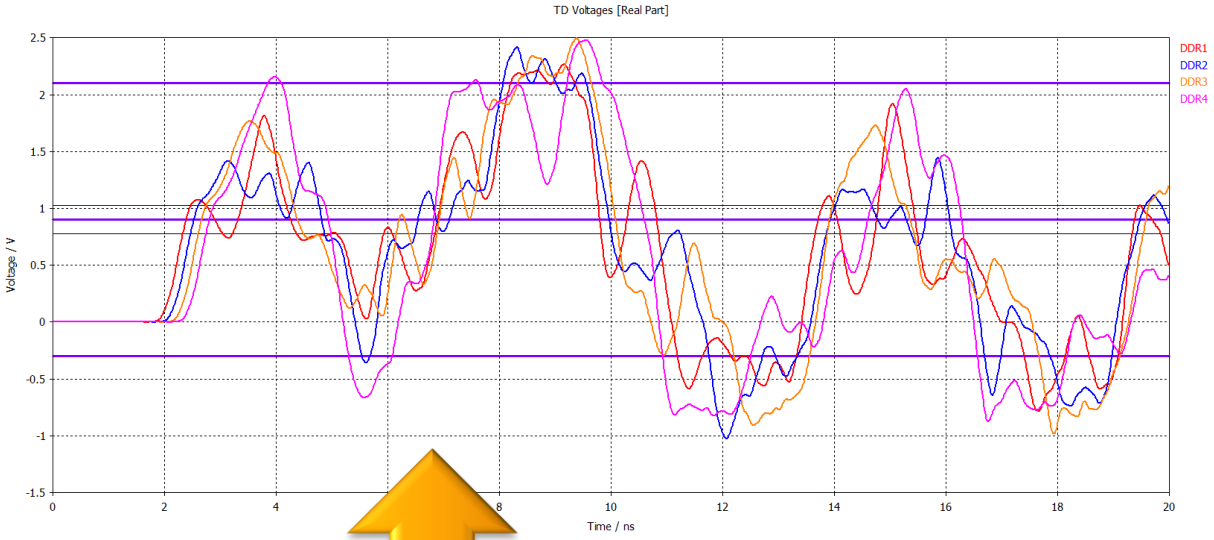
2D/2.5D



3D

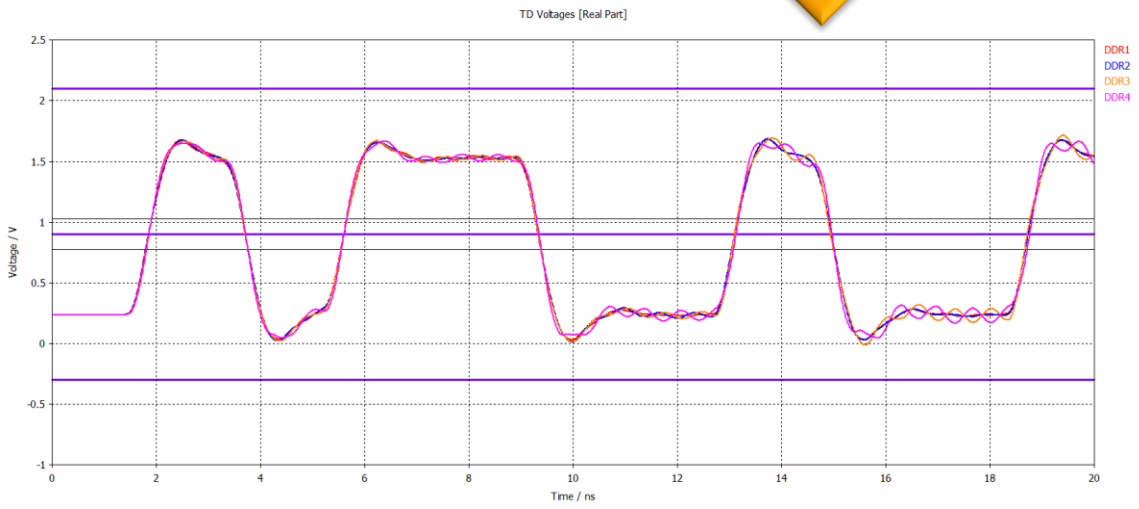


High Speed Design makes the difference

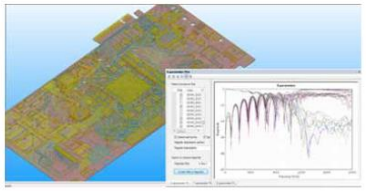


Address line waveforms for a DDR3 multi-drop system before optimization

….and after optimization

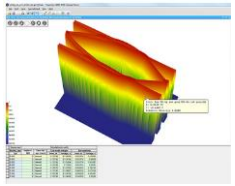


SI & PI Simulation Tools



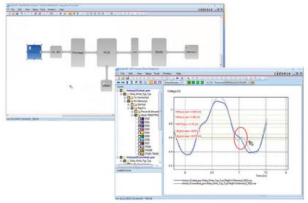
ANSYS

Designer SI, HFSS, SIWave



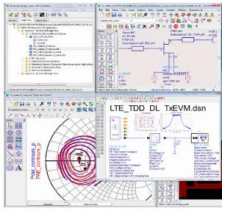
Mentor Graphics

HyperLynx



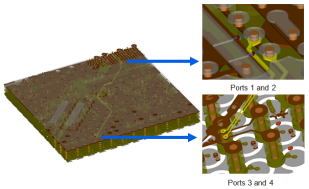
cadence

Allegro Sigrity



KEYSIGHT TECHNOLOGIES

Advanced Design System (ADS)



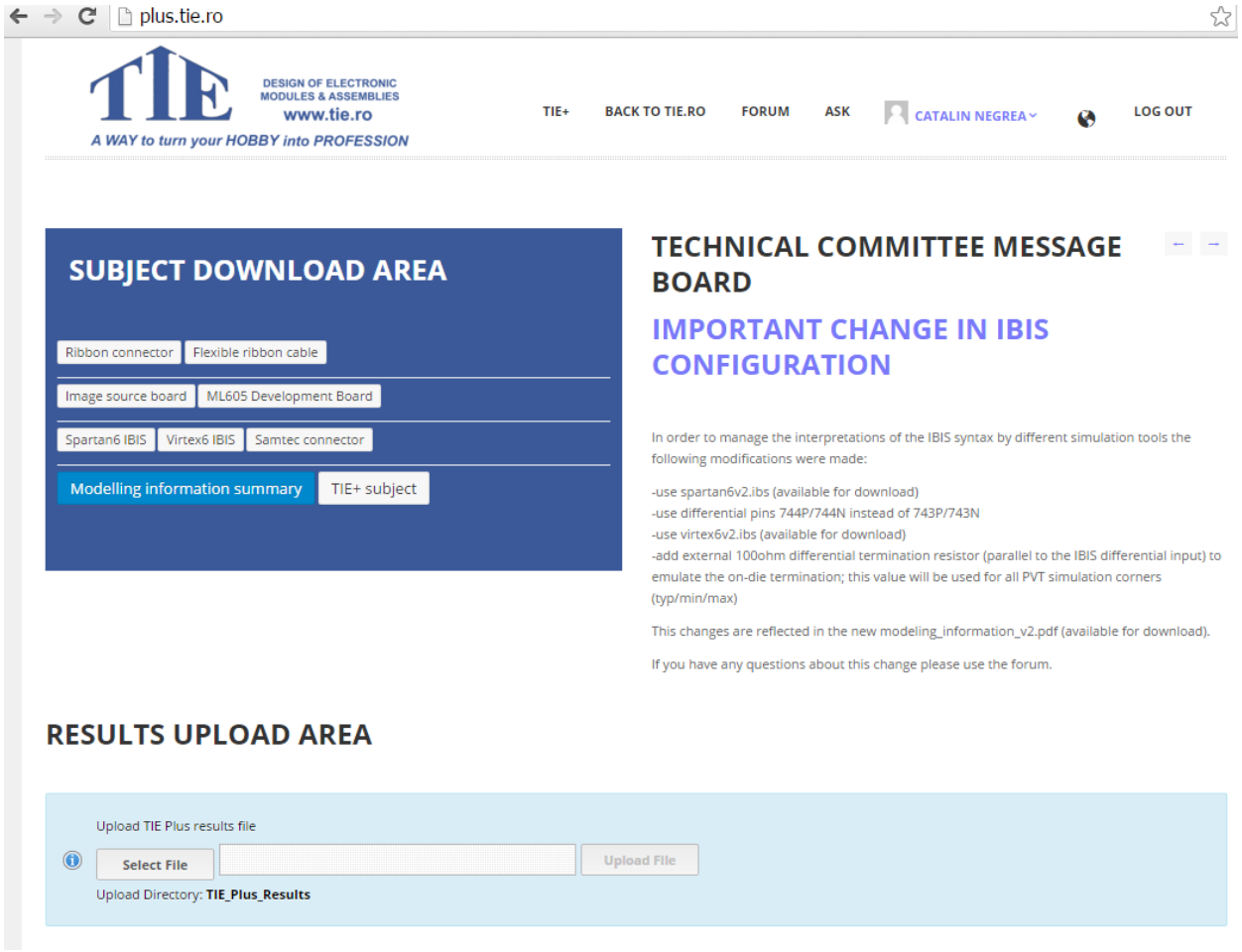
CST

COMPUTER SIMULATION TECHNOLOGY

TIEplus 2015 Review

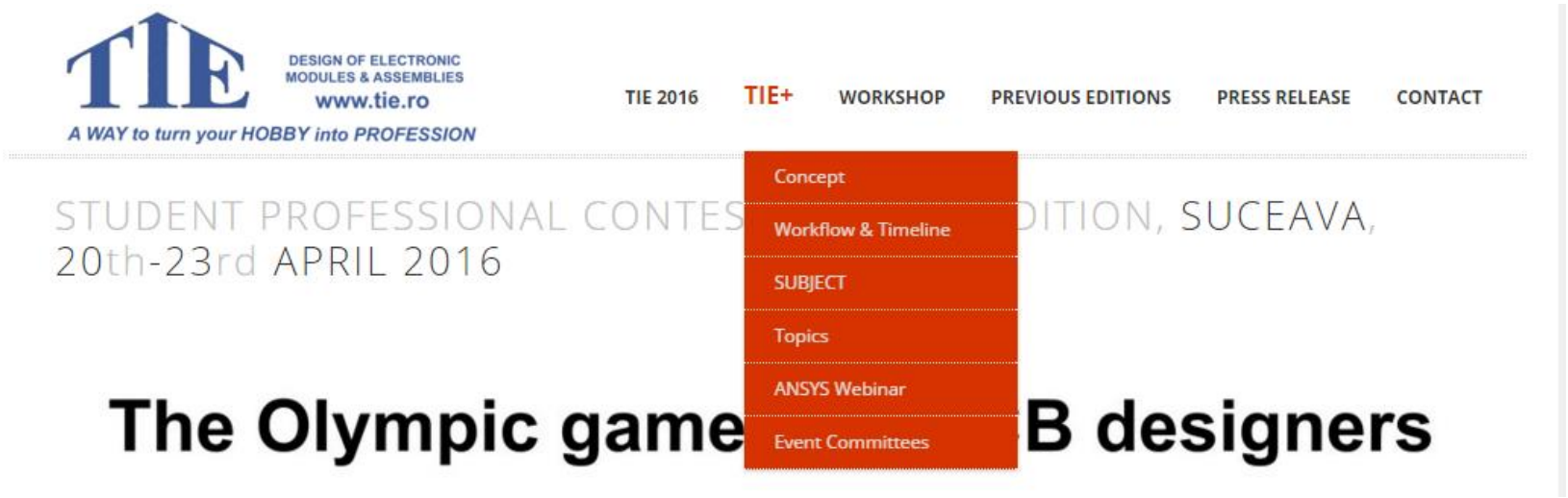
TIE+ 2015 review

› The contest started based on an online platform; the contestants received login credentials after their registration profile has been validated



TIE+ 2015 review

The TIE+ info for the 2015 edition is still available online



- After a 2 week period dedicated to solving the subject the contestants finally got the chance to present their simulation results
- ***The final stage of TIE+ took place at the Stefan cel Mare University of Suceava the next day after the standard TIE seminar***

…. But let's see how TIE+ really looked like…..

Summary of the first edition

- 11 registered participants from 6 universities
- 4 bachelor students, 5 master students, 2PhD students
- 5 participants made it to Suceava and presented their solutions
- Used software for the solving of the subject: ANSYS, Hyperlynx, CST
- 3 of the participants reached a good level in providing a feasible technical solutions
- The top 3 contestants received a “Certificate of competence in Signal Integrity Simulation”

TIEplus 2015 SUBJECT

TIE+ Subject
General circuit description

The multi-board system overview presented in figure 1 is given, describing an high resolution image acquisition system for quality compliance testing. Figure 2 presents the PCB board connectivity and signal flow.

System description:

- Board 1
  - represents the image source device containing the image source driver IC100 (IBIS model: Spartan6.ibs); the high speed interface consists out of 13 (1*CLK + 12*Data) differential pairs following RSDS specifications (Reduced Swing Differential Signaling)
  - the RSDS signals exit Board1 PCB trough connector B1.X100 and are propagated by a flexible ribbon cable to Board 2
  - the Board1 PCB interconnect model is provided as touchstone file
- Board 2
  - represents the an intermediate connectivity board that is used to connect and organize the RSDS lines to match Board 3 requirements
  - this PCB is under development and requires pre-layout routing directives that will result from the signal integrity analysis
  - the PCB stack-up is provided
- Board 3
  - represents a ML605 development board containing a Virtex6 FPGA
  - the receiver for the RSDS signals of interest and is represented by U1, a Virtex6 FPGA (IBIS Model: Virtex6.ibs)
  - PCB CAD data in ODB++ format and stack-up information are provided

TIE+ Subject
System Overview

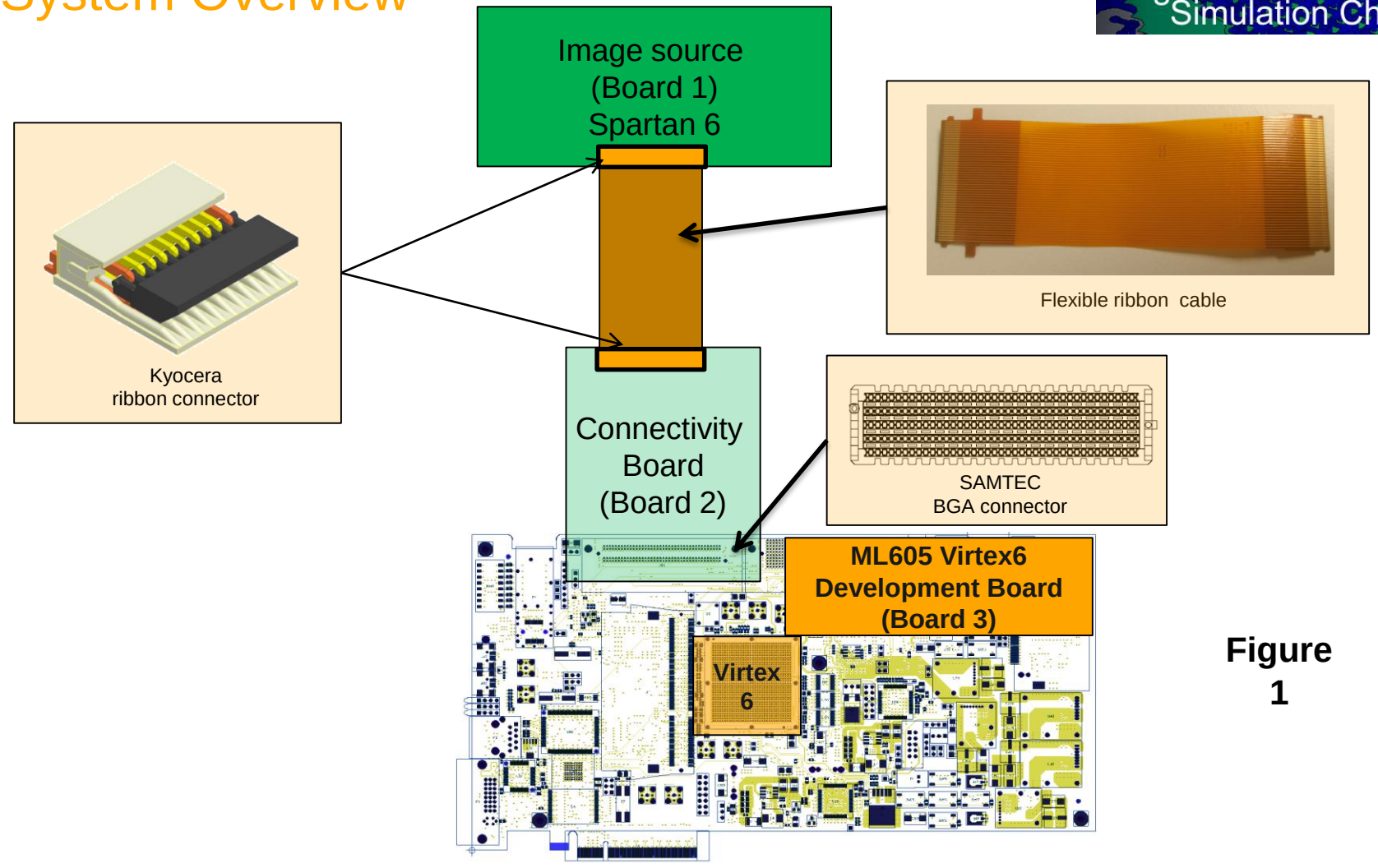


Figure 1

TIE+ Subject

Multi-board system diagram. Signal flow diagram.

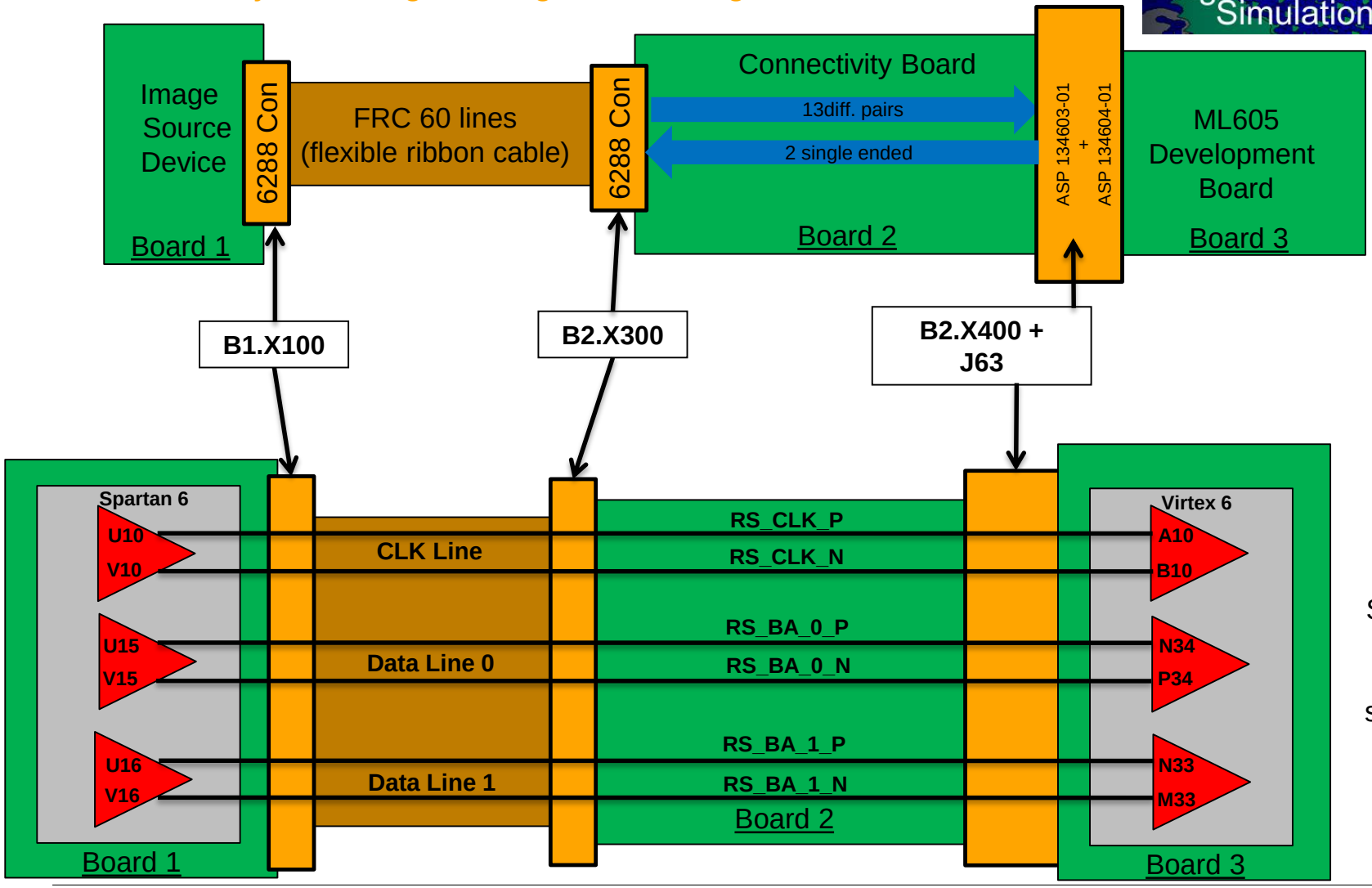


Figure 2

Signals of interest for the simulation

TIE+ Subject
Requirements

Based on the previous system description it is required to analyze signal integrity aspects for the signals RS_CLK_P, RS_CLK_N, RS_BA_P_0, RS_BA_N_0 , RS_BA_P_1, RS_BA_N_0 based on the signal flow diagram from figure 2.

Requirements

A) Define the routing directives for Board 2 PCB specifying: routing layers, routing topology options (microstrip/stripline), differential and common-mode impedance, inter-pair spacing (spacing between the traces of the same pair), trace width.

B) Evaluate the need of series resistors placement on Board 2 for signal integrity improvements (e.g. reflections, crosstalk) .

C) Evaluate VIA propagation delays on Board 2 and establish if there is a need for inter-pair and pair-to-pair VIA number matching.

D) Evaluate pair-to-pair far-end crosstalk at system level. Define a Vp-p crosstalk vs. pair-to-pair spacing chart. Define the minimum acceptable pair-to-pair spacing for Board 2 based on the obtained data.

E) Evaluate the following signal parameters at receiver end (Virtex6 input pins): rise\fall slew rate SE, overshoot & undershoot values SE, high\low time differential.

F) Evaluate the following timing parameters at receiver end (Virtex6 input pins): setup time to CLK (differential); hold time to CLK (differential)

* All simulation data must be provided for MIN (slow), TYP(typical), MAX(fast) IBIS model PVT IBIS corners (assume the logical worst case for the target analysis)

Simulation conditions:

CLK frequency: 125MHz, duty cycle: 50%
Single Data Rate transfer (positive edge)
Unit Interval =1 *CLK period = 8ns

Receiver signal requirements:

Data-to-CLK max. pair-to-pair skew = +/- 50 ps
Max. inter-pair skew = +/- 10 ps
Max. differential signal crosstalk =10 mVpp
High Input Voltage = +100mV
Low Input Voltage = -100mV

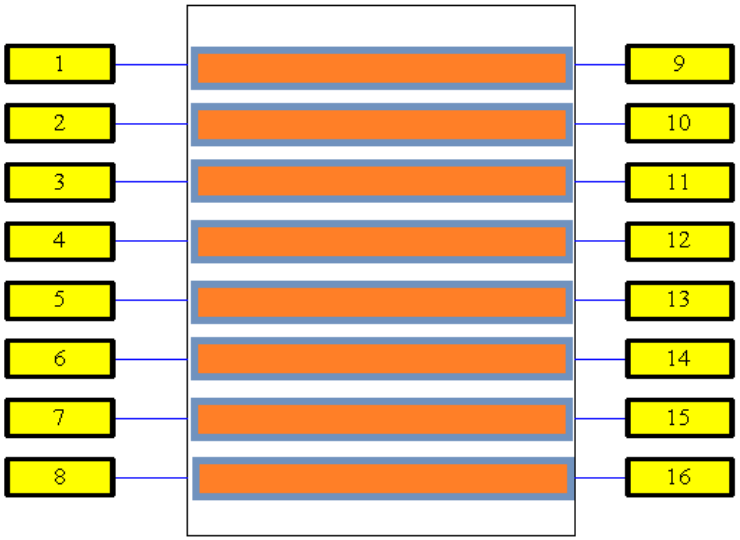
Part information\modeling summary

Part Name \ Reference	Description	Modeling information
Board1 ref: IC100 IC: Spartan 6 FPGA IC code: XC6SLX453CSG324	Driver IC	IBIS model: *spartan6.ibs* - use CSG324 package parasitics - use differential pins 743P\743N corresponding to driver model RSDS_25_TB_25
Board 1 PCB	DUT board	The 3 diff pairs are extracted (2D field solver) in Touchstone model : *Board1_sparam_1000pts.s12p*
B1.X100, B2X300	Ribbon connector	Touchstone model for 8 pins: SERIES_6288_8Pin.s16p S-parameter port definition: 6288_sim_model.pdf
Flexible ribbon cable	Length: 60mm	Touchstone model for 8 lines*: FRC_model_log.s16p,* Mechanical drawing: *FRC_data.pdf*
Board 2	PCB under development	4 layer stack-up presented on slide 6 board mechanical drawing is presented *adapter_drawing.pdf*
B2.X400 + J63	Adapter board – ML605 connector pair	HSpice simulation model: *HM_seam035_seaf065.mlm* Mechanical drawing: *ASP-134604-01-mkt.pdf*
Board_3 PCB	ML605 Virtex 6 development board	16 layer stack-up on slide 9 board ODB++: ML605_odb.zip
Board3 ref: U1 IC: Virtex 6 FPGA IC code: XC6SLX453CSG324	Receiver IC	IBIS model: *virtex6.ibs* - use FF1156 package parasitics - use differential pins 132P\132N corresponding to driver model LVDS_25

Ribbon cable model

S-parameter model port assignment for files
FRC_model_log.s16p (1000 frequency points, 1GHz, log distribution)
FRC_model_lin.s16p (1000 frequency points, 1GHz, linear distribution)

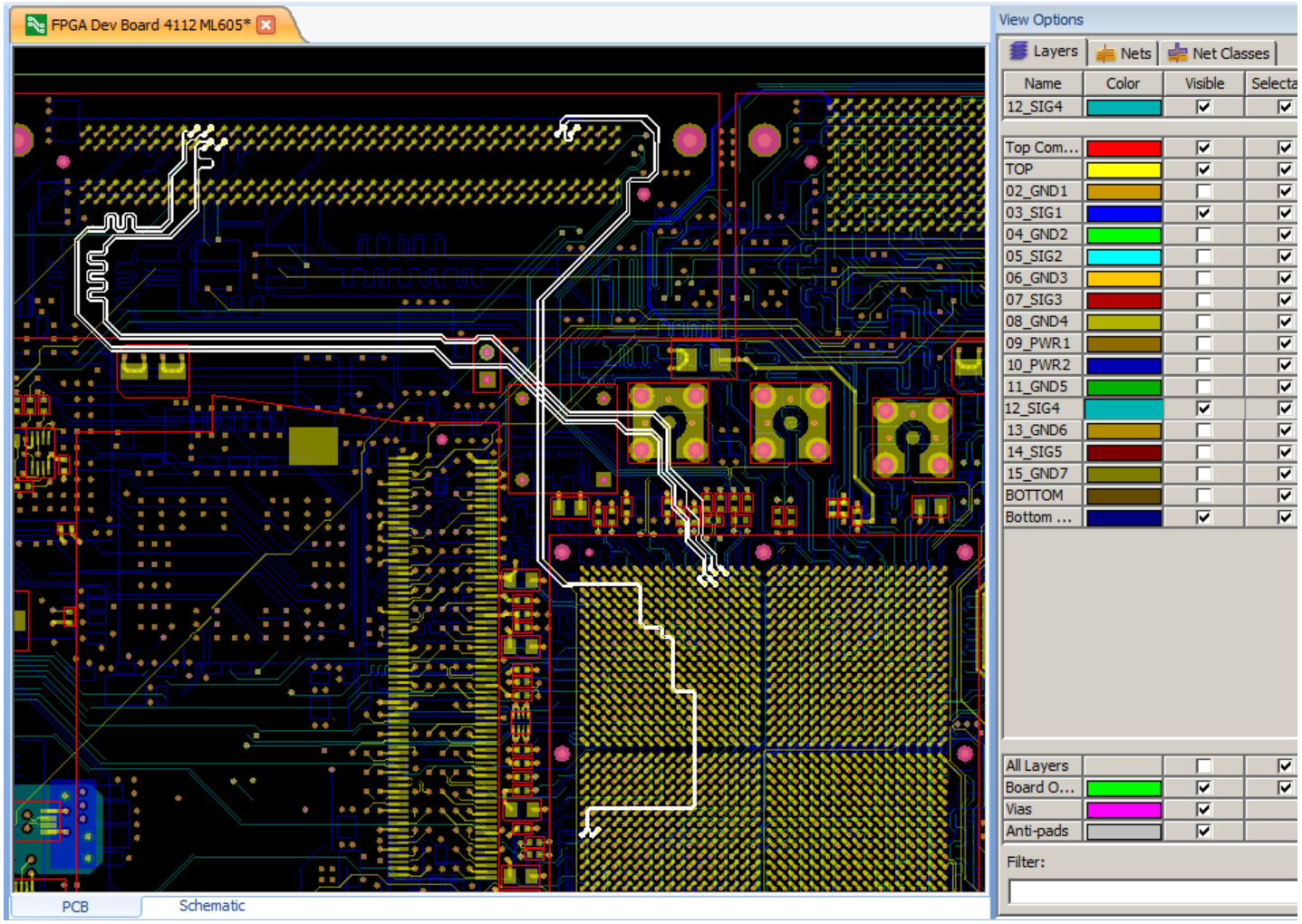
Mechanical dimensions can be found in FRC_data.pdf



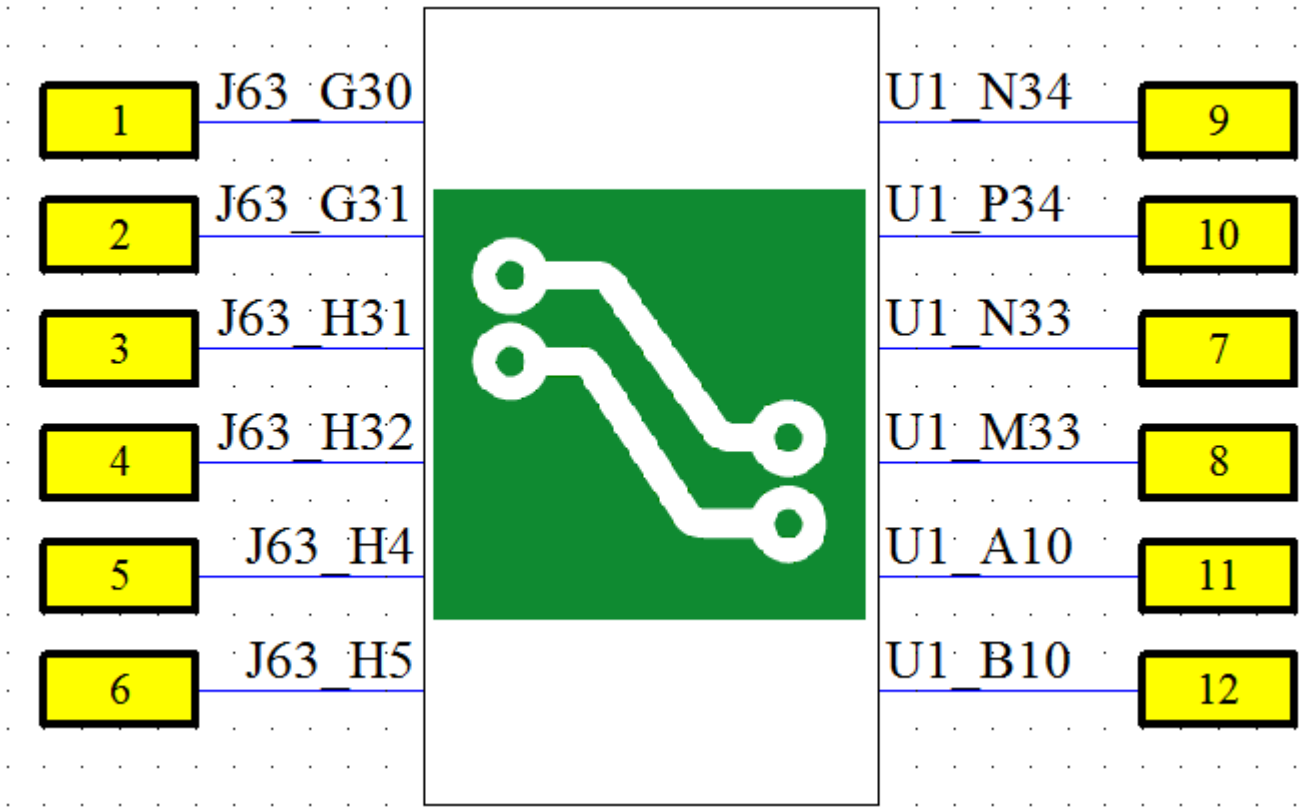
Recommendations:
- connect the 2 unused lines to ground

Passivity and causality checked using Hyperlynx Touchstone viewer V2.1; no errors found

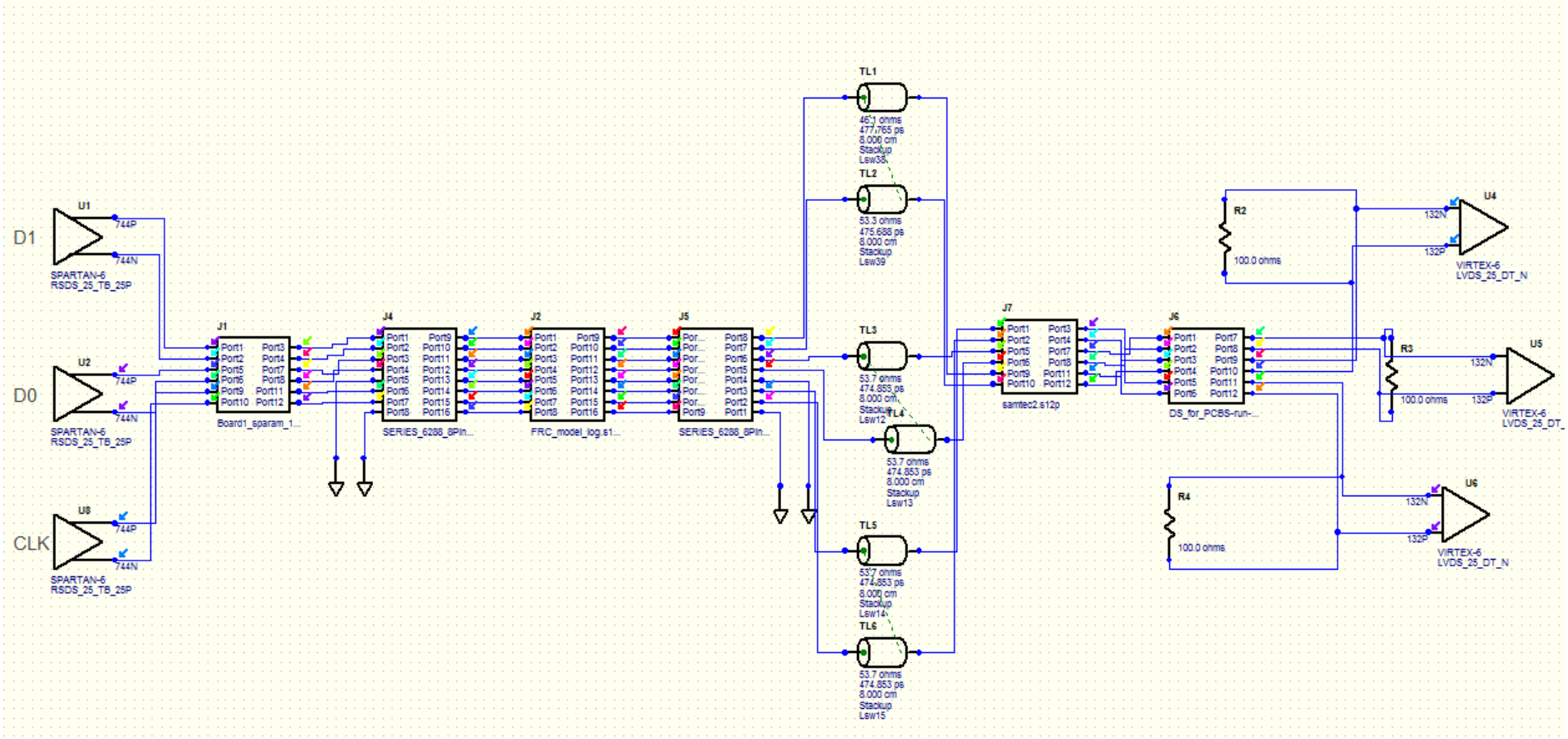
CST Modeling



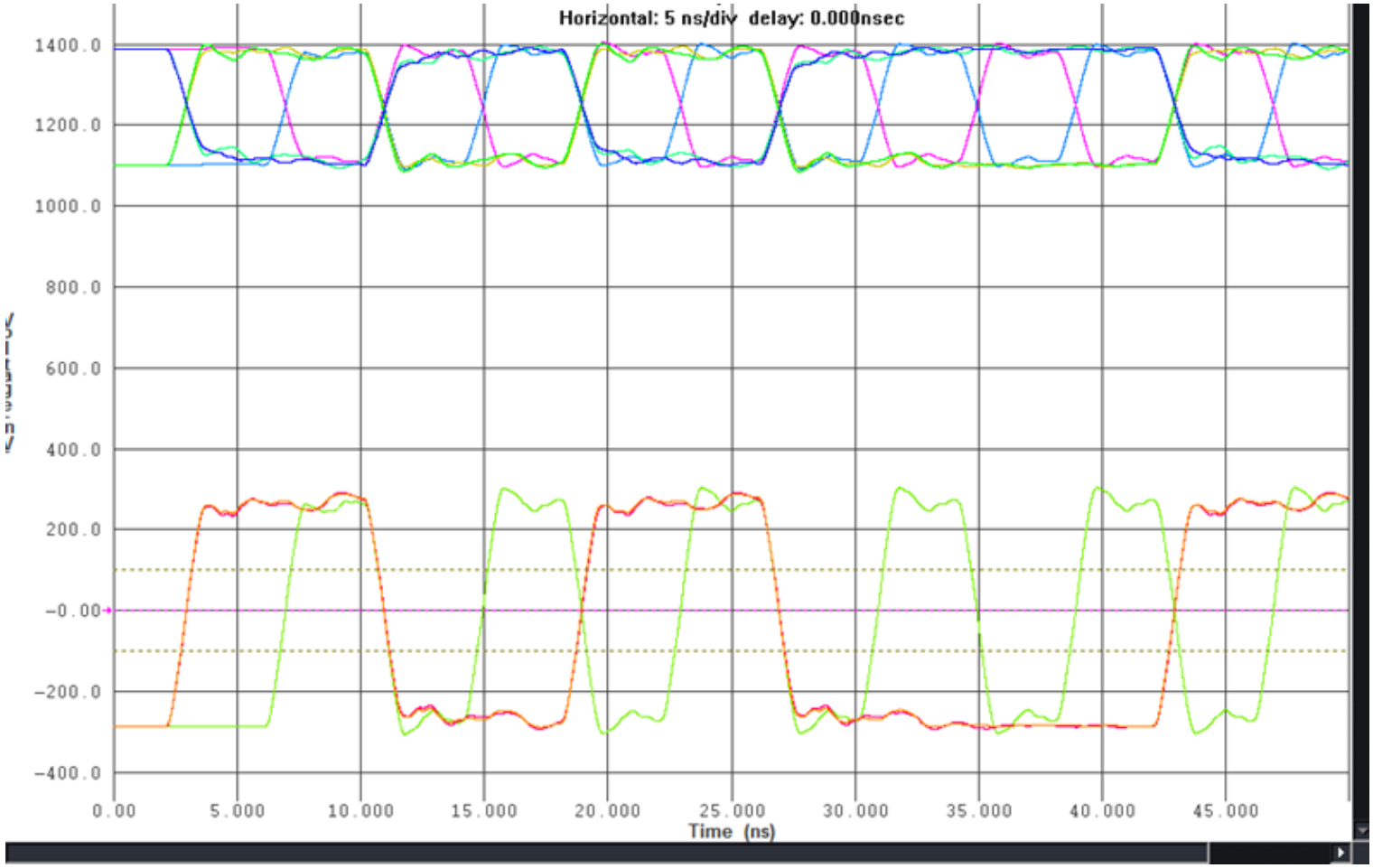
….. some hours later



System schematic for the nets of interest

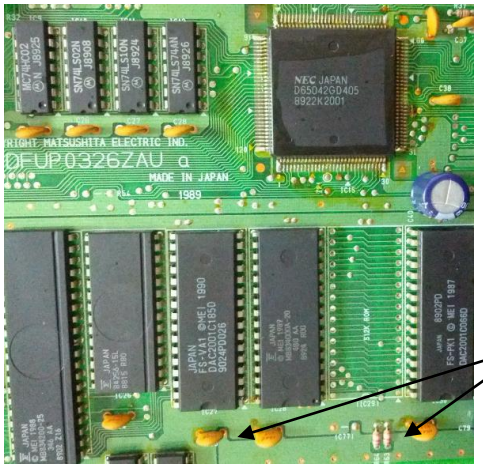


A first look at the signals in TYP



TIEplus 2017 Review

PDN Design
Then and Now

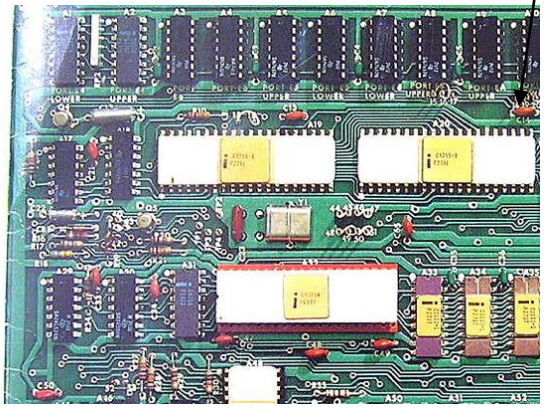


PDN design from the 90’

THD
ceramic disk
capacitors

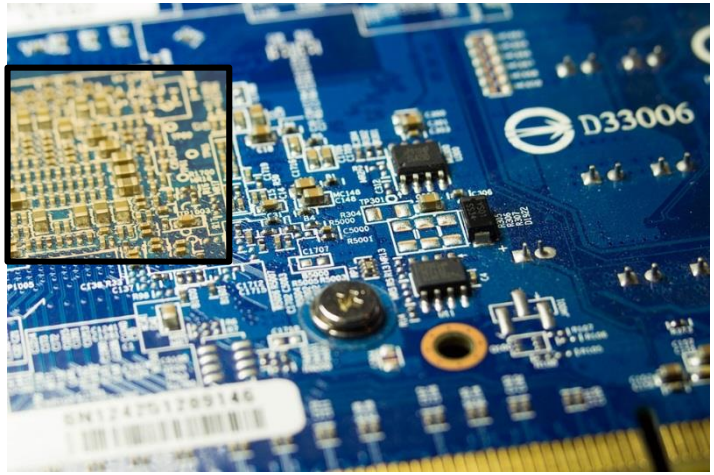
on-package
MLCC
capacitors

PDN design from the 2011 (Apple)



PDN design from the ’76
Intel single board computer

PCB
decoupling
capacitor
array under
GPU



This edition's topic was POWER INTEGRITY

- Importance of PDN design is rapidly increasing:
  - Semiconductor technology fabrication node progress

    - latest commercial chip uses 14nm
    - 32nm and 22nm are considered "standard" technology
    - ITRS (International Tech. Roadmap for Semiconductors) forecast -> 5nm in 2020

  - For digital cores this always means

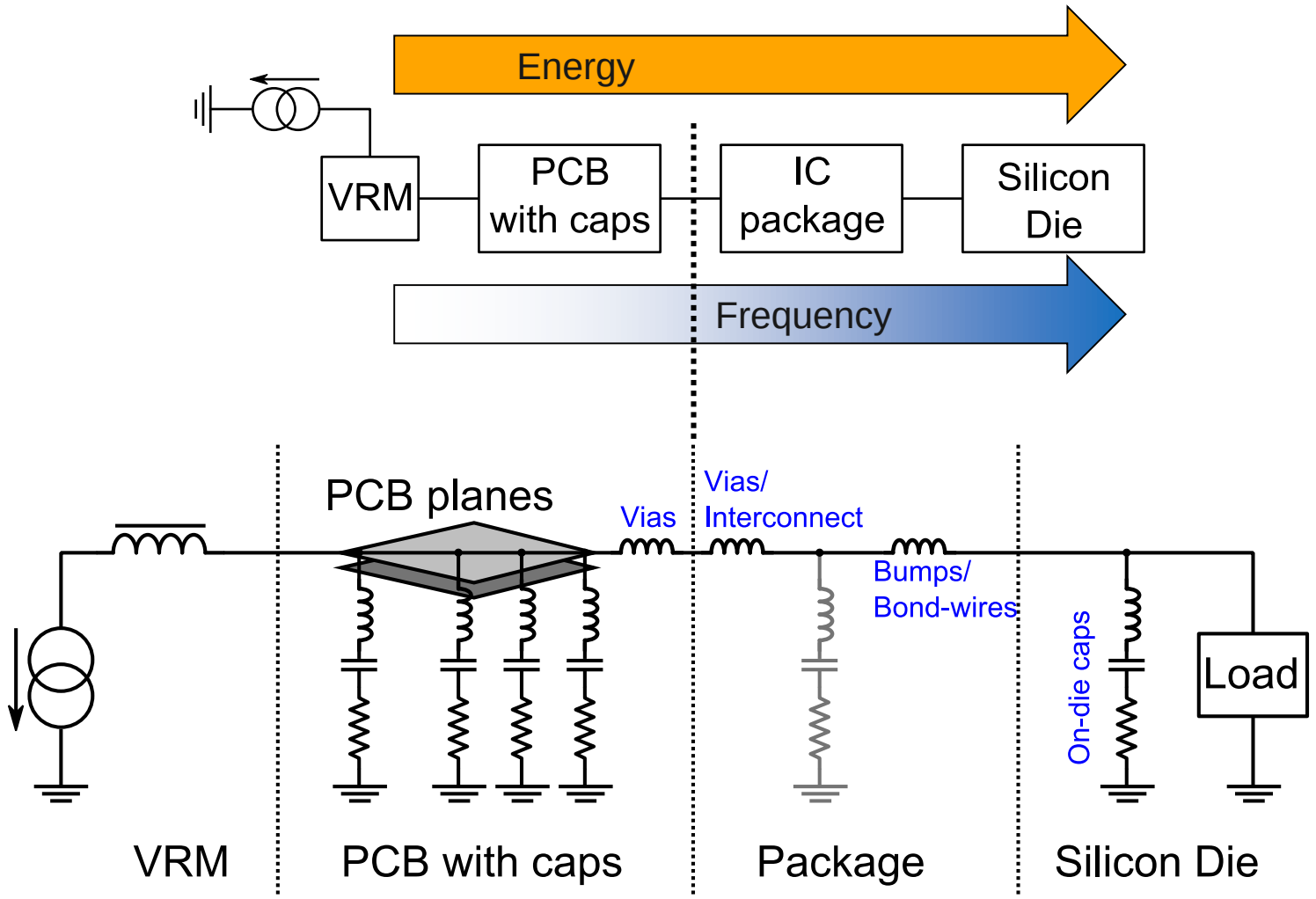
	current technology
supply voltage ↘ ↘	*0.7..1.1 V*
noise tolerance ↘ ↘	*2.5..5 %*
supply current ↗	*10-30 A*
clock rates ↗↗	*1-2GHz*

- For power distribution networks this means

Lower Target Impedance up to higher frequencies

$$|Z| < V_{noise} / I_{transient}$$

Parts of a power distribution network



Summary of the 2017 edition

- 10 registered participants from 5 universities
- 6 bachelor students, 2 master students, 2PhD students
- 4 participants made it to Iasi and presented their solutions
- Used software for the solving of the subject: ANSYS, CST + a PCB CAD tool

TIEplus 2017 Evaluation

TIEplus 2017 Awarding

TIEplus 2017 SUBJECT

TIE+ Subject
General circuit description

Figure 1 presents the block diagram for a SoC based graphical processing system. Figure 2 presents the connectivity diagram for the embedded x32 DDR3 point-to-point interface.

System description:

- IC1000 represents the GPU processing unit IC in a BGA625 package
- IC2000 and IC3000 are the two 1Gb DDR3 memory ICs in a FBGA96 package
- The data transfer rate is 1066MT/s; DDR3 clock frequency is 533MHz
- The DDR3 module is supplied by a 1.5V rail generated by the SMPS module based on IC5000
- VREF supply line design is not required

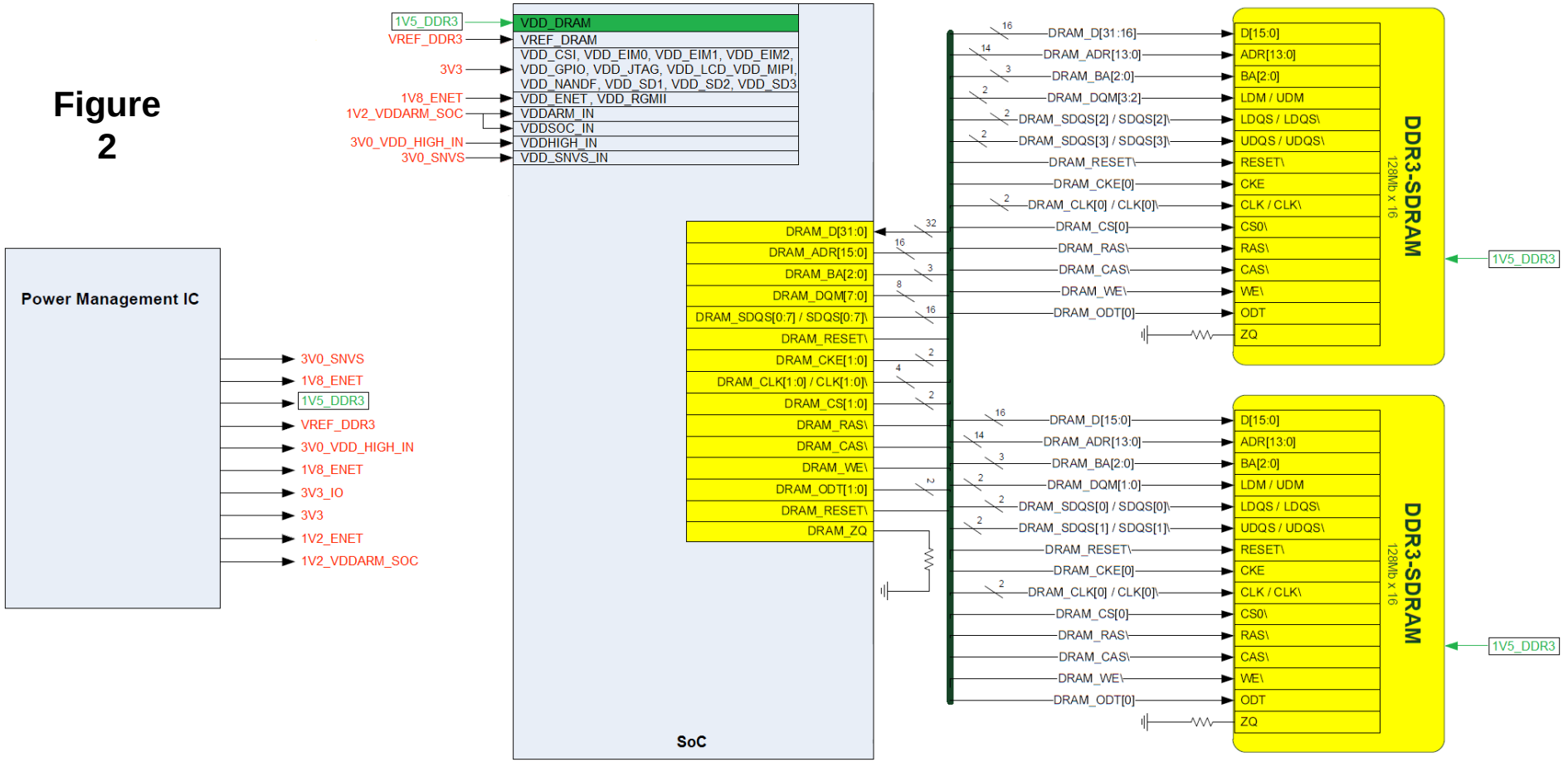
The following documents are provided:

1. Stack-up.pdf – PCB stack-up definition with material properties and routing constraints
2. DDR3_Datasheet – technical data for DDR3 memory IC
3. SoC_Datasheet - technical data for GPU SoC
4. Schematic.pdf – the DDR3 interface schematic

The board definition and component placement are defined in on page 5.
The VRM (SMPS) modeling information is provided on page 6.

TIE+ Subject
DDR3 Interface Diagram

Figure 2



TIE+ Subject
Requirements

Based on the previous system description it is required to design and verify the power integrity solution for 1.5V DDR3 supply rail in order to meet the ripple noise requirements under maximum transient load conditions.

PRE-LAYOUT

(A) Evaluate noise budget and define DC drop and AC design targets

(B) Define plane geometry constraints based on the DC drop target

(C) Evaluate capacitor mounting inductance and plane spread inductance

(D) Establish the guidelines for power plane routing (minimum width, length)

(E) Define the decoupling capacitor network based on the AC design target

*Use capacitor models from Murata MLCC lineup (www.murata.com)
*Only capacitors with 0402, 0603 and 0805 case type must be used for decoupling

LAYOUT

(F) Based on the defined results from (D) and (E), route the power rails for 1V5 and GND (including capacitor network) in a CAD environment

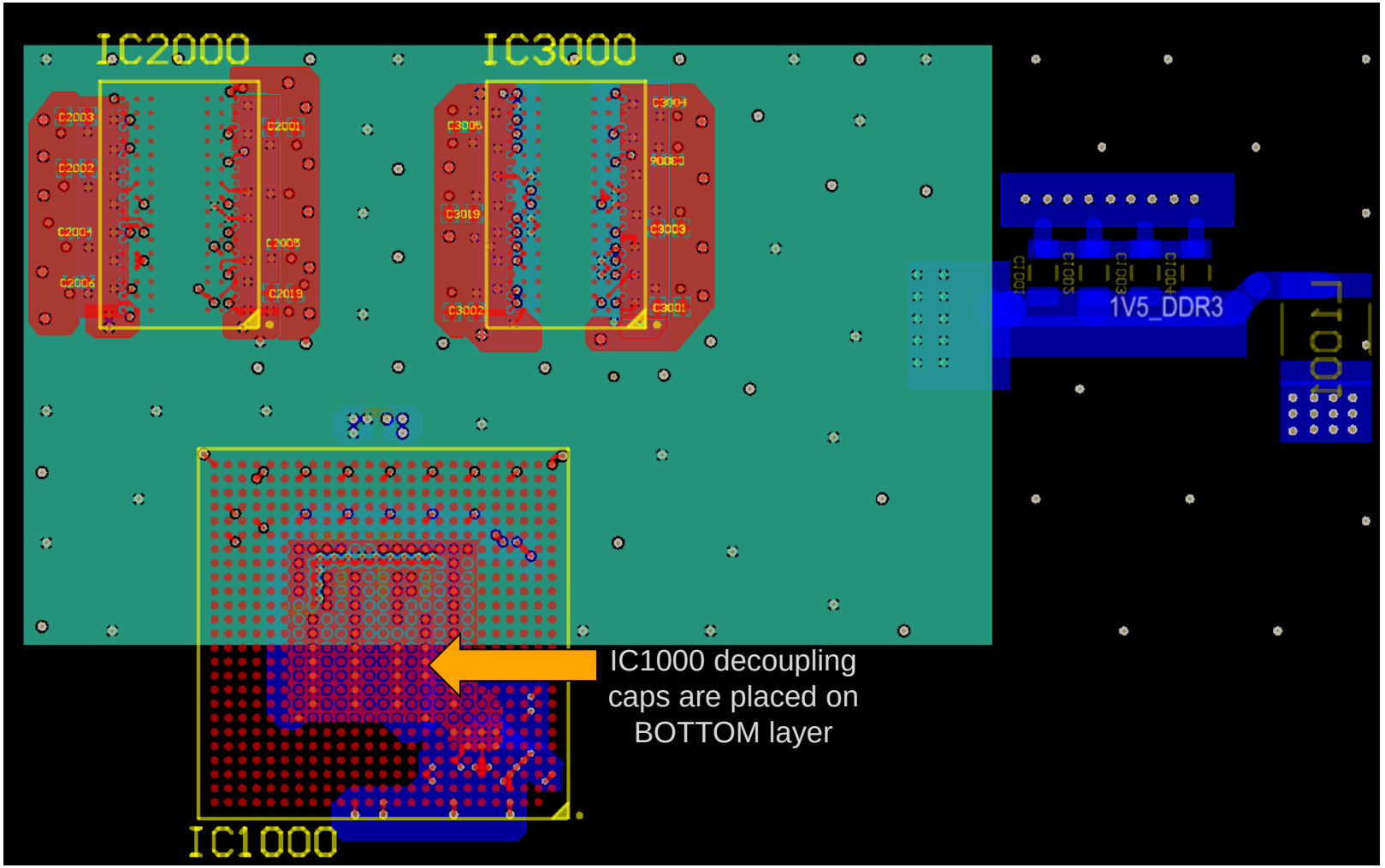
POST-LAYOUT

(G) Make an IR Drop Analysis on the 1V5 supply rail and verify compliance to the DC Drop target (point A)

(H) Make a post-layout analysis in the frequency domain for the 1V5 supply rail (and corresponding return path) and analyze impedance vs. frequency plot compliance to the target impedance (point A)

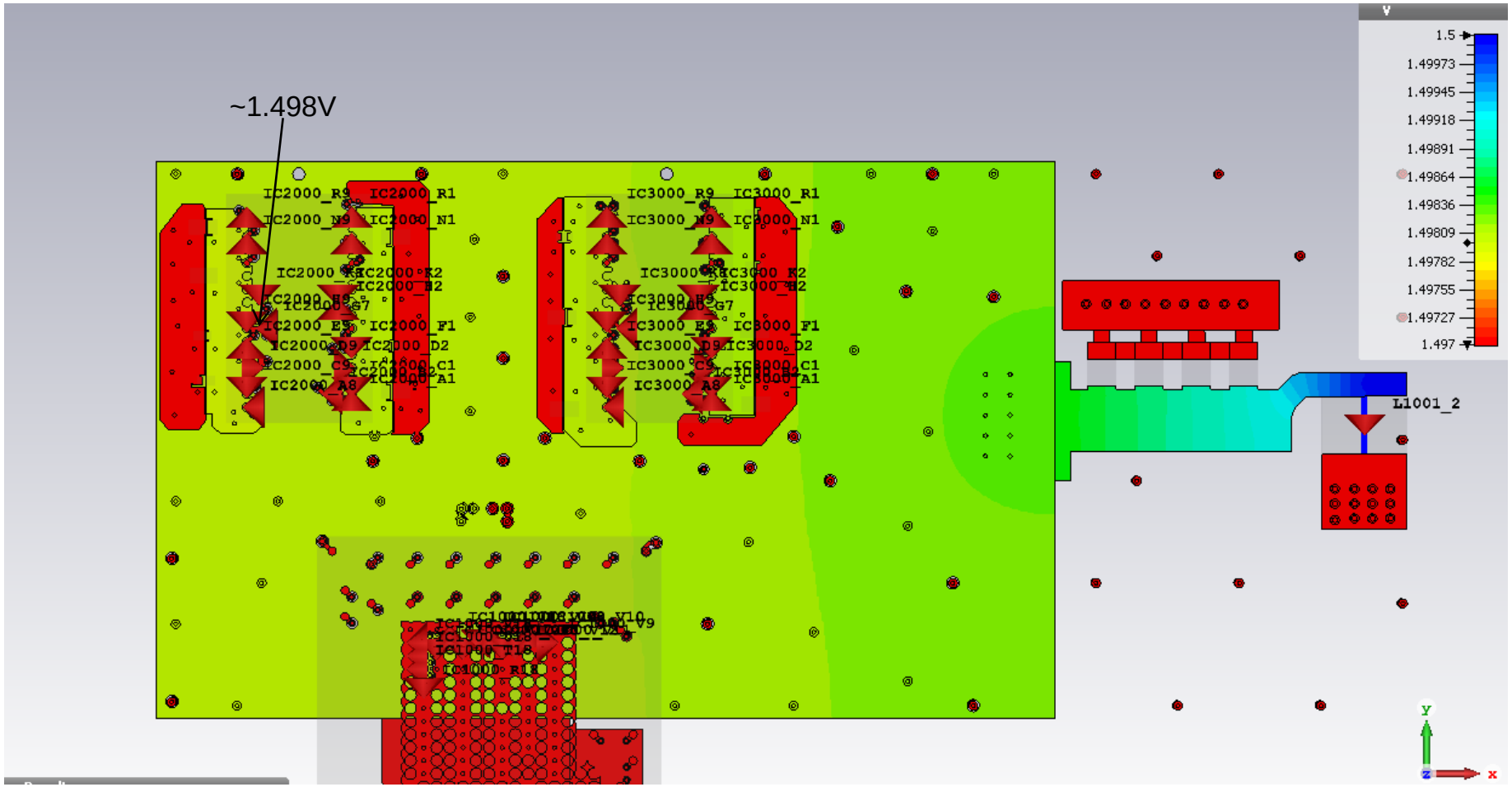
H) Optimize the PDN design using a minimum number of decoupling capacitors

First layout loop
PCB Layout 1

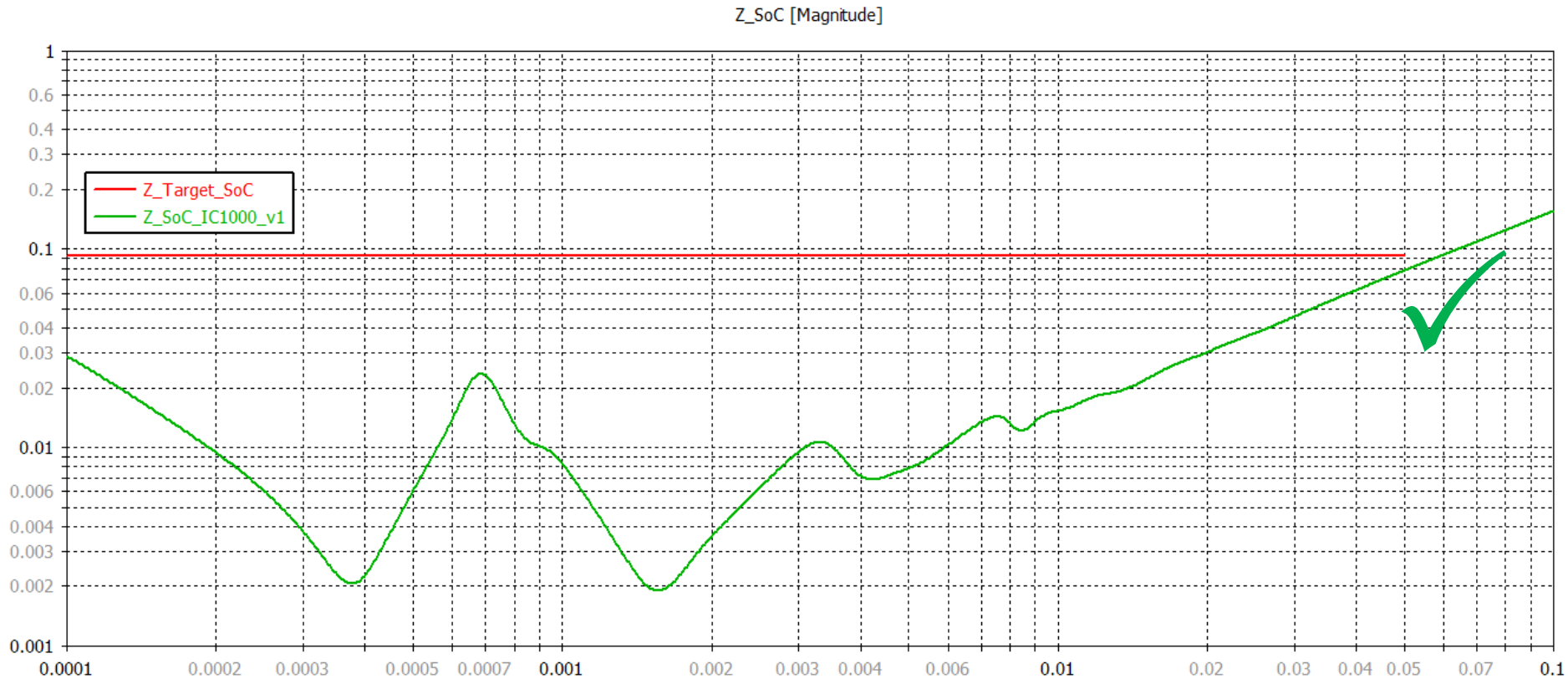


First layout loop
IR Drop Results / VDD

TIEplus
Signal & Power Integrity
Simulation Challenge



Second layout loop
AC results / mean impedance SoC



Next TIEplus editions

TIE Plus workflow

- **Publication of subject**
  - The subject content will published on the TIE website in a separate form “TIE Plus”. Also contest topics, recommended bibliography and contest regulations will be available.
  - At this stage only the subject text and block diagrams will be public. The simulation models, datasheets and other details will be available for download only after the contestant is registered.
- **Contestant registration**
  - The registration will be done using an application form. The provided information will be analyzed by the technical committee and a notification email will be sent to the applicant (accepted \ rejected as a contestant for TIE Plus). After acceptance the contestant will receive user login information on the TIE plus platform. Based on this he/she will be able to download all necessary files associated with the subject.
- **Solving the subject**
  - Solving the subjects will be done by own\university\supported\sponsored technical means (hardware and software).
  - The technical solution will be posed as R&D report document that shall be uploaded on the web platform.
- **Assessment of the solutions**
  - The contestants are required to prepare a short presentation (15-20 min.) that will be exposed to the technical committee during an evaluation meeting. The presentation content must be in full agreement with the uploaded R&D report.

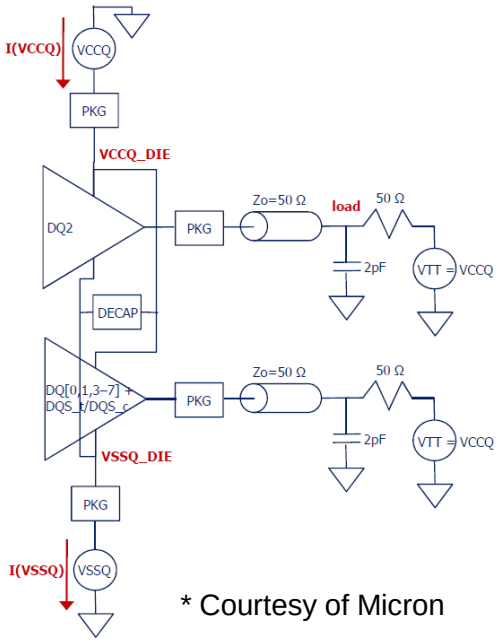
The TIEplus live evaluation session will take place in Pitesti in the same week as the TIE contest.
Keep an eye on the www.tie.ro for upcoming news on TIE PLUS.

Next edition's subject topic ?

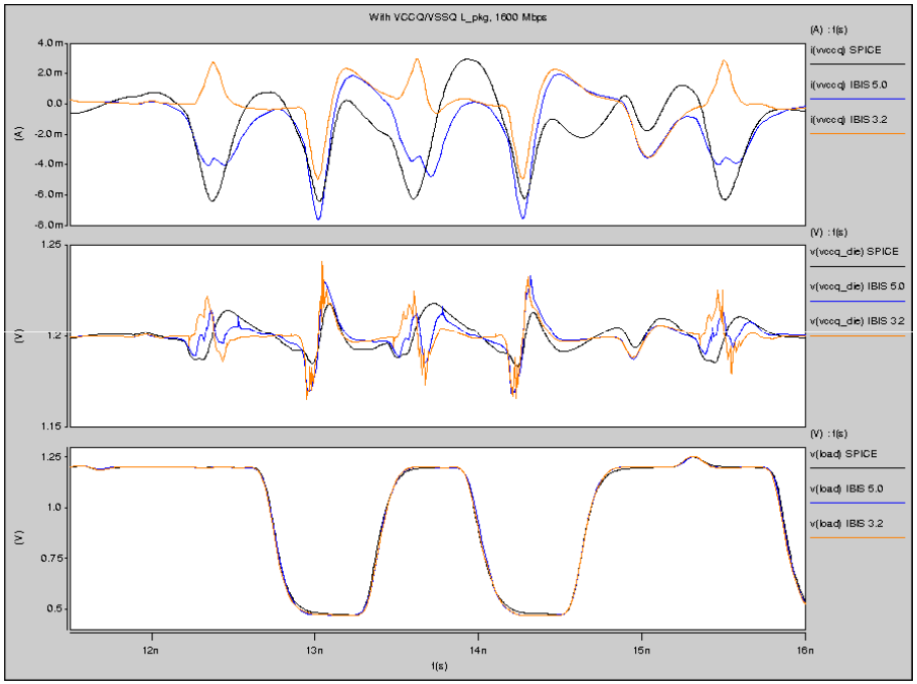
- First edition : signal integrity for RSDS differential transmission
- Second edition: power integrity for a DDR3 embedded memory system

NEXT STEP ?

- Maybe mixed Signal and Power Integrity Co-simulation.....
  - IBIS rev 5.0 models support power aware I/O modelling
  - Effects like supply noise and SSN induced jitter can be analyzed in detail



* Courtesy of Micron



I/O current

VDDQ noise

DQ output

TIE Plus recommended bibliography

- *Signal Integrity Issues and Printed Circuit Board Design*, Douglas Brooks, Prentice Hall PTR
- *High-Speed Digital Design "A handbook of Black Magic"*, H. W. Johnson, Prentice Hall PTR
- *High-Speed Circuit Board Signal Integrity*, Stephen C. Thierauf, Artech House
- *Advanced Signal Integrity for High-Speed Digital Designs*, Stephen Hall, Howard Heck, IEEE-Wiley, 2009.
- *Frequency Domain Characterization of Power Distribution Networks*, Istvan Novak, Jason R. Miller, Artech House, Boston, 2007.
- *Signal Integrity – Simplified*, Eric Bogatin, Prentice Hall, New Jersey, 2009.
- *Signal Integrity Characterization Techniques*, Mike Resso, Eric Bogatin, IEC, 2009.
- *Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages*, Brian Young, Prentice Hall, 2000.
- *Timing Analysis and Simulation for Signal Integrity Engineers*, Greg Edlund, Prentice Hall, 2007.
- Power Distribution Network Design Methodologies, Istvan Novak
- Frequency-domain Characterization of Power Distribution Networks, , Istvan Novak

START HERE !

How to approach the subject

› At first sight the requirements and level of complexity can be a little intimidating

› Use the registration period (from the moment the draft subject is released until to full subject description) to define understand the theory behind the subject topic and to establish a design flow

› As with the traditional TIE, preparing upfront makes the difference; you have an entire year to get familiar with theory an practical examples; the web is full of useful information

› Don’t jump directly in to simulations; try to make an action plan and start with some rough hand calculated approximations to the get a “feeling” for the magnitude of involved parameters

› Start with selecting what is relevant from the recommended bibliography for the subject topic

› Simplify the subject and see how far you can get with just the basic requirements

› Don’t waste time searching for design examples that would magically fit the subject requirements

› Don’t waste time searching for “pre-cooked” solutions; if something like that existed there would be no point in making a contest

Continental
The Future in Motion

Thank you for your attention.

catalin.negrea@continental-corporation.com