"POLITEHNICA" UNIVERSITY OF TIMIȘOARA
&
"POLITEHNICA" UNIVERSITY OF BUCHAREST
CENTER FOR TECHNOLOGICAL ELECTRONICS AND INTERCONNECTION TECHNIQUES

INTERCONNECTION TECHNIQUES IN ELECTRONICS

International Student Professional Contest

The 23rd Edition, Timișoara, 9-12 April 2014

TIE

DESIGN OF ELECTRONIC
MODULES & ASSEMBLIES

www.tie.ro

A WAY to turn your HOBBY into a PROFESSION

The 23rd Edition

Final Program

Promoted by IEEE CPMT HU&RO Joint Chapter

TIE Event Programm

Editors:
Prof. eng. Dan Pitică, Ph.D.
Assist. eng. Rajmond Jánó, Ph.D.

DESIGN OF ELECTRONIC MODULES & ASSEMBLIES

www.tie.ro

Student professional contest
The 23rd Edition, Timişoara, April 9 - 12, 2014

Organized by:

"POLITEHNICA" UNIVERSITY OF TIMIŞOARA
http://www.upt.ro

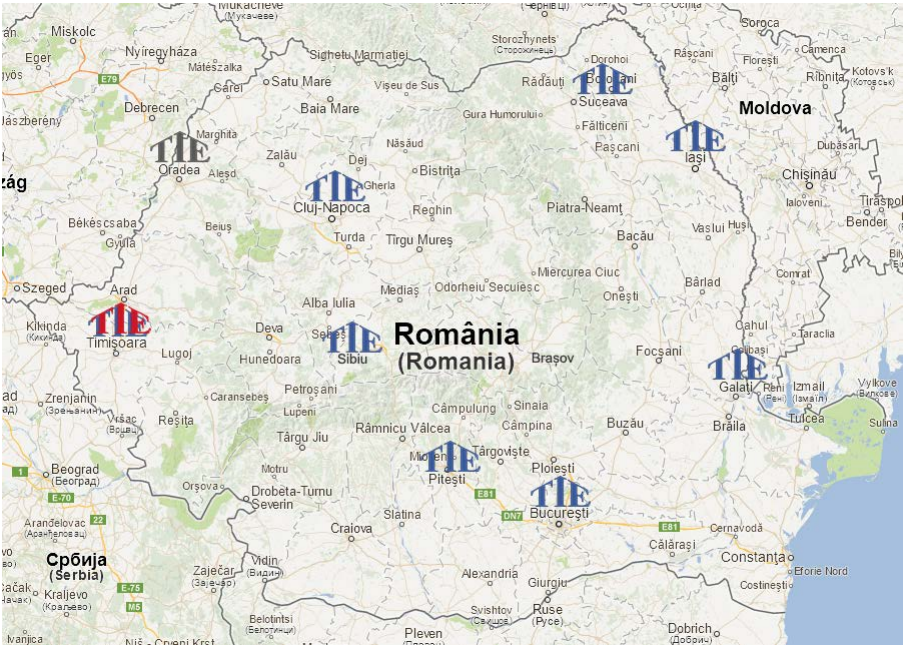
"POLITEHNICA" UNIVERSITY OF BUCHAREST

Center for Technological Electronics and Interconnection Techniques
http://www.cetti.ro

and supported by:

EPETRUN (Electronic Packaging Education Training and research Network)

TIE Past, Present and Future Editions



1992-2002	“Politehnica” University of Bucharest
2003	“Politehnica” University of Timişoara
2004	Technical University of Cluj-Napoca
2005	“Gh. Asachi” Technical University of Iaşi
2006	“Politehnica” University of Bucharest
2007	“Ştefan cel Mare” University of Suceava
2008	University of Piteşti
2009	“Dunărea de Jos” University of Galaţi
2010	Technical University of Cluj-Napoca
2011	“Politehnica” University of Bucharest
2012	“Lucian Blaga” University of Sibiu
2013	“Transilvania” University of Braşov
2014	“Politehnica” University of Timişoara
2015	University of Oradea

Dear participants and guests,

On behalf of the local event organizers from "Politehnica" University Timişoara, it is my pleasure and honor to welcome you to the 23rd Edition of the TIE contest.

Timişoara is located in the Banat region of Western Romania and as, one of country's largest cities, is home to an estimated 312,000 people. Lying on the picturesque northern bank of the Bega River, Timişoara's long and dramatic history and stunning architecture attracts thousands of visitors each year. Widely regarded as a "Little Vienna", the city's vibrant cultural life has transformed Timişoara into one of Romania's most developed and cosmopolitan cities.

We are confident that you will have a pleasant stay in Timişoara and we look forward welcoming you here.

Prof. Aurel GONTEAN, Ph.D.
TIE 2014 Event Director
"Politehnica" University Timişoara, Romania

TIE Academic Platform, a Concrete Answer to the Innovative Electronics Industry Requirements

During these spring days we meet in Timişoara, a powerful centre of the electronics industry, in order to participate to the 23rd edition of TIE. For the last 23 springs, representatives of the Romanian academic environment as well as, for the last several years, their colleagues from Hungary participate at the TIE event, the “Interconnection Techniques in Electronics” international student contest. During these more than two decades, since the start of the TIE event, the main purpose has been the education and training of the future engineers involved in development of electronic modules, to be focused on the real problems they will face in their future professional activity as specialists in the design and manufacturing of electronic products in various fields. At one point during the evolution of TIE, it was felt the need to involve those whom, as students, competed in the contest and now are true professionals in electronics, working in well-known companies. This “industrial spirit infusion" in TIE has been a natural step since TIE promotes the idea of training students for the industry. This explains the presence of the IAC (Industrial Advisor Committee) in the committees list of the organizational structure of the TIE academic platform. This committee consists of engineers who are part of the electronics industry, many of whom are former TIE participants, persons who obtained leading positions in the finals or even won the competition. The presence of this committee in the organizational structure of TIE has led, through the very good collaboration with the Technical Committee (TC) – representing the academic environment, to a synergistic effect of great value. As a natural result of this collaboration, TIE has become an event that gives students the opportunity to have their level of professional competence certified directly by the industry. IAC and TC manage, through a perfect collaboration, the development of the technical subject (topic, drafting of the subject), the evaluation form, and the entire evaluation process. Finally, after ranking the results obtained by the participating students, IAC establishes the number of points that a student should obtain in order to receive the "PCB Designer" Certificate of Competence.

In my opinion, this level of cooperation between academia and industry could not have been achieved if the participating actors, the academic teaching staff and professionals from the industry, had not collaborated (and they are still fully collaborating), even at an affecting level at this platform created in universities; a platform that provides valuable skilled professionals for the

industry. TIE is a significant and a concrete response to the constant demands coming from companies in the electronics industry, from Romania or from abroad, regarding the adequate education and training of future engineers. At the same time, considering how many years have passed since the first TIE edition took place, we can notice the development, in this geographical area, of a “reservoir” of skilled and certified engineers in PCB design, representing the human resource of companies and being able to increase the competitiveness of them.

Although I have already mentioned this on several other occasions, this high level of the TIE event could not have been reached without the existence of a fruitful collaboration between the teams representing the universities that form the EPETRUN network (Electronic Packaging Education Training and Research University Network). These teams, coming from all over our geographical region, have made and continue to make a significant contribution to the education and training of future specialists in accordance with the requirements of the technical and technological progress we are witnessing now. The TIE Steering Committee includes persons who have an important role in determining the development of the electronic packaging topics in the curricula of the universities where the students are coming from. The decisions of the TIE Steering Committee have been correct milestones that have led to the current high level reached by TIE today. I would like to thank all those who were and are actively involved in the decision making process because this process represents the evolution base for future TIE progress.

This year, the final stage of TIE takes place in Timişoara and is organized by one of the most prestigious technical universities in the country, "Politehnica" University of Timişoara. I would like to thank the Local Organizing Committee of TIE for their support in organizing TIE and for their outstanding effort in providing high class conditions for this event.

I wish all TIE 2014 participants a successful and fruitful edition.

Bucharest 07 April 2014

Prof. Dr .h. c. Paul Svasta, Ph.D.
TIE Initiator
Head of Center
Center for Technological Electronics and
Interconnection Techniques
“Politehnica” University of Bucharest, Romania

The TIE Contest - Bridging academia and industry through students

The Interconnection Techniques in Electronics (TIE) is at its 23rd edition. Started by an enthusiastic group of teachers, its size increased from year to year - currently gathering over 40 competitors from all technical universities in Romania, and, in the last 4 seasons, even competitors from Budapest. This makes TIE an example of excellence, perseverance and passion for innovative thinking. Being the host of the event in 2014, "Politehnica" University of Timişoara (UPT) is proud to be associated with the values TIE has come to represent and promote.

"Politehnica" University of Timişoara is one of the biggest public universities in the Western part of Romania. It is among the institutions with great potential, which are responsible for the development of higher education and science in Romania "Politehnica" University of Timişoara takes into account the enhancement of its relationship with the economic and the socio-cultural environment of Western Romania, in particular, and, additionally, the exploitation of a wider national or international area, by strengthening its ties with the industry and with the companies whose profile matches the university's domains of specialization.

UPT encourages competition and performance and it is therefore honored to host the TIE contest, an event where many outstanding students of our university have been noticed and appreciated. Moreover, due to the massive involvement of industry representatives, TIE is much more than a simple academic competition; it is a bridge between academia and industry, the binder being students.

Hosting the Interconnection Techniques in Electronics Contest highlighters' "Politehnica" University's interest in continuing its cooperation with the local, county, regional and national authorities, therefore acting as a complex catalyst for development and as a binder for the various social actors.

Prof. Marius Oteşteanu, Ph.D.
Vice-rector for Scientific Research and External Relations
"Politehnica" University of Timişoara

Importance of the Layout for Quality and Reliability

The main goal of the production of SMT-Boards is the fulfillment of the expectations of the customer. There are three important parts of this expectations for a whole electronic equipment, the full function based on the description in the data sheet, an outstanding reliability under defined conditions and last but not least an adequate price.
These goals will be influenced by a lot of factors. This will be start by an analysis of the customer wishes. A specification sheet is one result of this analysis. One of the next steps is the design of the electronic circuit of the electronic equipment. This will be completed by careful selection of the used components and the definition of the ancillary conditions. These data are the starting point for the layout designer.
The responsibility of the layout designer for the final product is very high. The designer influences directly the costs of the board (e.g. how many layers are necessary). There are also a lot effects to the behavior of the produced board, e.g. an unsymmetrical construction of the layers in z-direction will possible lead a not acceptable warpage of the board during the soldering. A very small pad size will save area on the board, but such a layout will decrease the reliability of the solder joint. All these things are considered in design rules with a defined background. The knowledge of these rules and especially the background will help the designer, to create layouts not only with a working electric function, but also with a good reproducibility including quality and reliability.
The TIE-Contest will help you, to fulfill more and more the complete challenges of a professional layout designer!

Dresden 31st March 2014

Dr.-Ing. habil. Heinz Wohlrabe
Centre of Microtechnical Production
Dresden University of Technology

Student Contest with High Impact on Industry

The student contest in Design of Electronic Modules and Assemblies (TIE) provides a unique opportunity for the best PCB CAD designer students in Romania to demonstrate their expertise in this rapidly developing field of electronics. I have been privileged to participate in this excellent events in the last couple of years and to experience the exciting atmosphere of this generous rivalry.

The knowledge that is required to the successful performance at the contest perfectly conforms to what industry expects from young electronic engineers. The skills that the students learnt during the education at their universities as well as gained in the course of the preparation for and participating in the contest make them real CAD design professionals, who are able to develop innovative electronics products. The high-tech manufacturing of perfectly designed circuits and systems is essentially important for the sustainable development of the Romanian and the entire European industry and economy.

As I have visited lots of industrial companies in different Romanian cities, it has been my pleasure to see how many previous TIE participants have been working at these companies, advancing the research and development activities, which have been more and more moving to this region of Europe. The universities, professors, TIE organizers and participants rightly be very proud of the professional level of TIE and its high impact on the Romanian electronic industry.

Budapest, 16 March 2014

Dr.h.c. Zsolt Illyefalvi-Vitéz, Ph.D.

Professor

Budapest University of Technology and Economics

TIE as model for engineering education

In the last 10 years, especially due to increased design density, new manufacturing technologies and increased performance needs, the PCB design and technology went through revolutionary changes.

In the automotive industry the focus increased on the design for signal and power integrity, manufacturability and also reliability. High speed design and thermal simulation became mandatory design step. More complex products, the need to integrate 3rd party systems (e.g. display modules) push the responsibility of the layout engineer beyond the well know frontiers. With the introduction of new technologies (HDI, microvias, embedded passives …) the need for fast know how ramp up became visible and also the need to develop better and new development tools, which are adapted to this new world. In fulfilling this market requirement for qualified engineers TIE has played a very important role.

TIE has an excellent reputation, it became a brand.

For the industry TIE acts as warranty for the quality of the engineers. Beside the strong theoretical know how, they acquire also the needed practical skills and, even more important, the right professional attitude and behavior. This was possible just by the strong involvement of the members which are in the TIE organization board. They understood the need of our industry, in the same time they act as an excellent professional and behavioral model for the students.

Having the 23rd edition organized in Timişoara is a new chance to strengthen the collaboration between TIE and Continental and to prepare the layout engineers for the future needs and challenges.

Timişoara, 02 April 2014

Kubik Andrei
Head of department
Continental Automotive Romania

Tribute to science

"Our science is the sum of thoughts and experiences of countless minds." When I think of the TIE contest, this quote of Ralph Waldo Emerson comes to my mind. I consider the participation of so many great minds in this important event in order to listen, think, design and exchange experiences in the field of advanced electronics is an honorable duty we pay to science.

In other words, I am very happy that such a contest exists and I would like to express my gratitude in this sense to Prof. Dr. h.c. Svasta, who did not only initiate TIE, but brought it to an excellent standard, at an international level. The fact that the contest reached the 23rd edition speaks for itself.

Moreover, I appreciate the transition between theory and practice, as the contest offers a frame, where both parties, universities and companies, work together to design PCBs for industrial applications. We need such events which offer students opportunities to have a real insight into what companies expect and how advanced the techniques in this competitive world are. Therefore, the contest also models the students into well-prepared, practical, down to earth human resources of the near future.

And last but not least, I am glad that Miele is part of this event. Thus, we can share our long term experience and know-how and benefit of the fresh perspectives and new paths students offer and accordingly contribute to the progress of science.

Braşov, the 25th of March

Hartmut Hohaus
General Manager
SC Miele Tehnica SRL

How to win TIE 2014
(suggestions coming from the TIE 2013 Contest Winner)

TIE event is a great opportunity for passionate students to work and to be evaluated by specialists. The good thing is, that there are more and more companies, providing CAD tools or are involved in developing electronic modules, interested in this contest. In this perspective, well know companies like Continental Automotive, Siemens, Microchip, Yazaki, and more others, are present at TIE event with their representatives engineers which are involved in the TIE Industrial Advisor Committee.

To be successful at TIE, first of all, you have to like everything with electronics related topics and to be skilled in design PCBs. This should be done with pleasure and enthusiasm, in other words this should be at the beginning a hobby, and later maybe, as professional, a full time job.

How to divide your time during contest:

1. Read the subject with calm and attention, in the allocated time before competition.
2. Ensure your copy of the schematic is correct and clear.
3. Assign the footprints to components, and if you don't have the specified footprint, built it. This is a critical step, if you put a wrong footprint and if you design a faulty one, during the contest you may not be aware of your mistake and you'll lose precious points.
4. Design the board outline specified in the rules.
5. Read carefully which subsection is more valuable.
6. Start routing.

From a personal point of view training for this competition was very useful for me because these kinds of activities place your resume in a bright light, and makes you understand how to handle big projects in short period of time. During competition it is very important to understand the rules, and how they are aplied in a real project.

Bucharest, March 31, 2014

Adrian BOSTAN, Eng. MTS
First place at TIE 2013 Contest
Microchip Technology Romania

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TIE 2014 Program

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<tr><th colspan="4">Thursday, April 10, 2014</th></tr>
<tr><th></th><th>“Students” Track</th><th>“Steering Committee” Track</th><th>“Technical Committee” Track</th></tr>
<tr><td>08:00-10:00</td><td></td><td></td><td rowspan="3">Technical meeting
(local members only)
A105</td></tr>
<tr><td>9:15</td><td colspan="2">Gathering for Continental Automotive visit.
Location: Faculty of Electronics and Telecommunications,
Main Entrance, Bd. Vasile Parvan 2</td></tr>
<tr><td>10:00-12:45</td><td colspan="2">Visit to Continental Automotive Romania</td></tr>
<tr><td>13:00- 14:00</td><td>Registration of the participants
Electro Hallway
Lunch
1MV</td><td>Lunch
1MV</td><td>Lunch
1MV</td></tr>
<tr><td rowspan="2">14:15-19:00</td><td colspan="3">Opening Ceremony
UPT Senate Room</td></tr>
<tr><td colspan="2">International Workshop
„Advanced Topics in Electronic Assembling Technology”
UPT Senate Room</td><td>Technical meeting
A105</td></tr>
<tr><td>19:15-20:00</td><td colspan="3">Student Technical Session
Presentation of TIE 2013 subjects
Set-up and checking of contest computers, CAD environments
A108 + Cafeteria 1C</td></tr>
<tr><td>20:15-21:00</td><td colspan="3">Dinner
Cafeteria 1C</td></tr>
<tr><td>21:00-22:30</td><td></td><td>Steering committee meeting
AC Council Room</td><td>Technical meeting
+
Advertising Committee Meeting
A105</td></tr>
</table>

Friday, April 11, 2014			
07:00-07:30	Breakfast Cafeteria 1C		**Technical preparation** Library / Cafeteria 1C
07:30-08:00	**TIE 2014 contest preliminary activities**		
08:00-12:00	**TIE 2014 CONTEST** Cafeteria 1C	**09:00-10:30 AFCEA Student Clubs Meeting** A105	**Technical session** A116
12:00-13:00	Lunch Cafeteria 1C (competitors & supervisors) and 1 MV (all others)		
13:00-18:00	**Assessment of the TIE 2014 projects** Cafeteria 1C		
18:00-18.30		**Steering committee meeting** A105	
18.30-20.00	**TIE 2014 Awarding ceremony** UPT Senate Room		
20:00-22:00	Gala dinner TIE 2014 CP2		

Saturday, April 12, 2014	
07:30-08:30	Breakfast Cafeteria 1C
09:00-12:00	Ending session / Final remarks A105

Note:

1. Items in the program marked with **bold** type represent **compulsory activities** for the given track.

Workshop

„Advanced Topics in Electronic Assembling Technology”

10 April 2014

13.00-14.00 ***Registration***

14.15-14.30 **Welcome universities:**
Prof. Marius Oteşteanu, Ph.D., Vice-rector for Scientific Research and External Relations, “Politehnica” University of Timişoara, Romania
Welcome industries:
Dr. Christian von Albrichsfeld, Prof. onorific
General Manager Continental Automotive Romania
Welcome TIE technical workshop:
Prof. Dr. h. c. Paul Svasta, Ph.D. “Politehnica” University of Bucharest, Romania

14.30-16.30 ***First Session: Electronic Module Value Chain***

Session chairs
Prof. Dan Pitică, Ph.D., Technical University of Cluj Napoca, Romania
Detlef Bonfert, Ph.D., Fraunhofer EMFT, Munich, Germany

14.30-15.10 The role of simulation in high performance electronic design

Alain Michel, Business Development Manager Electronics, Europe Ansys France

15.10-15.50 Investigation on electrochemical migration in the microelectronics

Balint Medgyes, Ph.D., Electronic Technology Department, Budapest University of Technology, Hungary

15.50-16.30 Smart electronics in home appliances

Alexander Neufeld, Miele & Cie. KG | Werk Electronic, Germany

16.30-17.00 *Networking Break*

17.00-19.00 Second Session: Design for Manufacturing

Session chairs
Prof. Aurel-Ştefan GONTEAN, Ph.D., "Politehnica" University of Timişoara, Romania
Hartmut Hohaus, General Manager Miele Tehnica SRL

17.00-17.40 Life time prediction of solder joints

Prof. Dr.h.c. Zsolt Illyefalvi-Vitéz, Ph.D., Electronic Technology Department, Budapest University of Technology and Economics, Hungary

17.40-18.20 DFM Concept integrated in the predicted Life Cycle of a New Product

Lecturer Ioan Plotog, Ph.D., Politehnica University of Bucharest, Romania

18.20-19.00 Nano-characterization in tin whisker research

Balazs Illes, Ph.D., Electronic Technology Department, Budapest University of Technology and Economics, Hungary

TIE

DESIGN OF ELECTRONIC MODULES AND ASSEMBLIES

Student professional contest

Awarding Ceremony

11 April 2014 - UPT Senate Room

18:00-18:30 ***Registration***

18:30-18:45 ***Opening Ceremony Speeches:***
Prof. Aurel Gontean, Ph.D., TIE 2014 Chair, "Politehnica" University of Timişoara, Romania
Dipl. Eng. Alexandru Borcea, MBA, President of Romanian Association for Electronic and Software Industries

18:45 -19:10 ***Keynote speaker***
"Our future's innovative products through today's engineering capability"
Dr. Christian von Albrichsfeld, Prof. onorific
General Manager Continental Automotive Romania

19:10-19:20 ***State of the art TIE 2014***
Assoc. Prof. Norocel Dragoş Codreanu,Ph.D, Politehnica University of Bucharest,
TIE Technical Committee Chair

19:20-19:35 ***TIE 2014 Awarding***
Prof. Dr.h.c. Paul Svasta, Ph.D., Politehnica University of Bucharest,
TIE Steering Committee Chair
Prof. Dan Pitică, Ph.D., Technical University of Cluj Napoca,
TIE Steering Committee Co-Chair

19:35-19:55 ***PCB Designer Certification recommended by TIE IAC***
Dipl. Eng. Cosmin Moisa, Continental Automotive Timişoara,
TIE Industrial Advisor Committee Chair
Assoc. Prof. Gabriel Chindriş, Ph.D., Technical University of Cluj Napoca,
TIE Industrial Advisor Committee Co-Chair

20:00 ***Looking Forward TIE 2015***
Prof. Cornelia Gordan, Ph.D.,University of Oradea, ***TIE 2015 Chair***
Gala Dinner TIE 2014

TIE Past Editions Winners

Year	Name	University
2013	Bostan Adrian	“Politehnica” University of Bucharest
2012	Aldea Alin	University of Piteşti
2011	Precup Călin	“Politehnica” University of Timişoara
2010	Dungă Tudor Dan	“Politehnica” University of Timişoara
2009	Răducanu Bogdan	“Politehnica” University of Bucharest
2008	Oşan Adrian	“Politehnica” University of Timişoara
2007	Tamaş Cosmin Andrei	“Politehnica” University of Bucharest
2006	Moscalu Dragoş	“Gh.Asachi” Technical University Iaşi
2005	Andreiciuc Adrian	“Politehnica” University of Timişoara
2004	Berceanu Cristian	“Politehnica” University of Timişoara
2003	Munteanu George	“Politehnica” University of Bucharest
2002	Rangu Marius	“Politehnica” University of Timişoara
2001	Toma Corneliu	“Politehnica” University of Bucharest
2000	Vlad Andrei	“Politehnica” University of Bucharest
1999	Savu Mihai	“Politehnica” University of Bucharest
1998	Alexandrescu Dan	“Politehnica” University of Bucharest
1997	Gavrilaş Cristian	“Politehnica” University of Bucharest
1996	Vintilă Mihai	“Politehnica” University of Bucharest
1995	Ştefan Marius Sorin	“Politehnica” University of Bucharest
1994	Bucioc Mihai	“Politehnica” University of Bucharest
1993	Teodorescu Tudor	“Politehnica” University of Bucharest
1992	Teodorescu Tudor	“Politehnica” University of Bucharest

TIE Industrial Advisor Committee
Recommended PCB designers from 2010-2013

Participant Name	University	Year
Dungă Tudor Dan	"Politehnica" University of Timişoara	2010
Pică Zamfir	Technical University of Cluj-Napoca	2010
Gross Péter	BME Budapest	2010
Antonovici Dorin	"Ştefan cel Mare" University of Suceava	2010
Condrea Daniel	"Ştefan cel Mare" University of Suceava	2010
Lupuț Cătălin	"Politehnica" University of Timişoara	2010
Banciu Alexandru	"Politehnica" University of Bucharest	2010
Fülöp Krisztián	BME Budapest	2010
Tudose Mihai Liviu	"Politehnica" University of Bucharest	2010
Burghiau Mihai	"Ştefan cel Mare" University of Suceava	2010
Knizel Alexandru	"Politehnica" University of Timişoara	2010
Pandelică Ovidiu	University of Piteşti	2010
Caracațeanu Cătălin	"Dunărea de Jos" University of Galați	2010
Țibuleac Cătălin	"Politehnica" University of Bucharest	2010
Blănaru Andrei	"Transilvania" University of Braşov	2010
Malinetescu Adrian	North University of Baia Mare	2010
Ungureanu Vlad	“Transilvania” University of Braşov	2010
Precup Călin	"Politehnica" University of Timişoara	2011
Antonovici Dorin	"Ştefan cel Mare" University of Suceava	2011
Mareş Mihai	University of Piteşti	2011
Gordan Cristian	"Politehnica" University of Timişoara	2011
Burghea Mihai	"Ştefan cel Mare" University of Suceava	2011
Crăciun Gabriel	"Politehnica" University of Timişoara	2011
Țibuleac Cătălin-Ciprian	"Politehnica" University of Bucharest	2011
Bostan Adrian	"Politehnica" University of Bucharest	2011
Fiastru Bogdan	Technical University of Cluj-Napoca	2011
Aldea Alin	University of Piteşti	2011
Andrieş Lucian	"Ştefan cel Mare" University of Suceava	2011

Caracaţeanu Cătălin Paul	"Dunărea de Jos" University of Galaţi	2011
Aldea Alin	University of Piteşti	2012
Turdean Mihai	Technical University of Cluj-Napoca	2012
Andrieş Lucian	"Ştefan cel Mare" University of Suceava	2012
Avădanii Alexandru	"Politehnica" University of Bucharest	2012
Mares Mihai	University of Piteşti	2012
Marin Marian Valentin	University of Piteşti	2012
Burgheaua Mihai Alexandru	"Ştefan cel Mare" University of Suceava	2012
Tănase Mihai	"Politehnica" University of Bucharest	2012
Boţilă Alexandru	"Politehnica" University of Timişoara	2012
Ţibuleac Cătălin	"Politehnica" University of Bucharest	2012
Gordan Cristian	"Politehnica" University of Timişoara	2012
Antonovici Dorin	"Ştefan cel Mare" University of Suceava	2012
Ardelean Mihaela	"Politehnica" University of Timişoara	2012
Ştefan Andrei	"Politehnica" University of Bucharest	2012
Bostan Adrian	"Politehnica" University of Bucharest	2013
Bota Claudiu	"Politehnica" University of Timişoara	2013
Ilie Mihai	Technical University of Cluj-Napoca	2013
Timoficiuc Ovidiu	"Ştefan cel Mare" University of Suceava	2013
Olenici Alexandru	Technical University of Cluj-Napoca	2013
Sofîlca Ionuţ-Bogdan	“1 Decembrie 1918” University of Alba Iulia	2013
Grigoraş Eduard	"Ştefan cel Mare" University of Suceava	2013
Chitic Mihail	“Transilvania” University of Braşov	2013
Petric Cristian	"Politehnica" University of Timişoara	2013
Cervis Alexandru	Maritime University of Constanţa	2013
Moise Mădălin-Vasile	University of Piteşti	2013
Lăcătuş Daniel	"Politehnica" University of Bucharest	2013

TIE 2014 Workshop Abstracts

The role of simulation in high performance electronic design

Abstract: Simulation is an essential step in the design flow of high performance electronic devices. Throughout the design process, designers will use several levels of simulation system, circuit and physical. This presentation will define these different levels and explain when and why to use them during the design process.

Keywords: Simulation, 3D Electromagnetic, Electronic, System, Circuit

Several factors like higher frequency of operation, increasing signal speed, and more complex integrated devices increase the risk of failure when designing high performance electronic devices. Using simulation earlier in the design process will help to reduce this risk.

The design process will start with the definition of the system using behavioural model. This step allows to validate the operation of the complete system and to define specification for each sub-system. As an example the communication system shown in Fig.1 includes sub-system such as baseband transmitter, RF transmitter, RF receiver and baseband receiver.

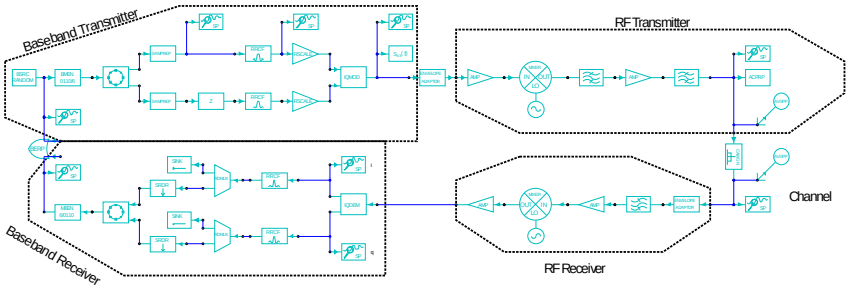

Fig. 1: Communication system

Each sub-system includes component such as modulators, filters, amplifiers, mixers … and will be designed by different teams. Let's take the Low Noise Amplifiers (LNA) component from the RF receiver. Designer will use circuit simulator to simulate this function using components such as capacitor, resistor, inductor, transistor, diodes. These components have analytical model that can be used in linear, harmonic balance or transient simulation. Fig. 2 shows a part of the schematic entry used to define the LNA. To get one level down in the simulation process the designer will have to take in account the physical layout of the LNA. The layout effects are not fully captured by the circuit simulation and need to be simulated using electromagnetic (EM) simulation. Fig. 3 shows part of LNA layout. The top left part of Fig. 3 shows coupling between lines that are captured by EM simulation. Several type of EM simulation can be used 3D, 2.5D …

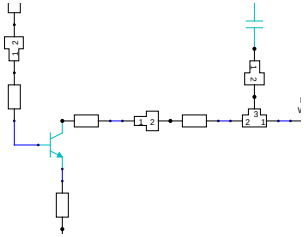

Fig. 2: Part of LNA schematic

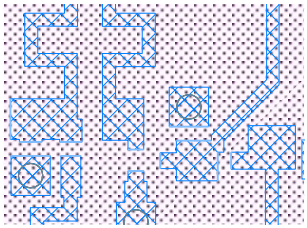

Fig. 3: Part of LNA layout

Using different method Finite Element Method (FEM), Method of Moment (MOM)… Circuit simulation and EM simulation can be combined to get accurate model of the LNA. This model will be used further in system simulation, replacing the behavioural model to get a final validation of the system. During this presentation each simulation level will be detailed. Interaction between levels will be shown and explained.

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Investigation on electrochemical migration in the microelectronics

Abstract: It will be presented a novel in situ and real time monitoring system which is suitable for optical observations and simultaneous electrical parameter measurements during electrochemical migration (ECM) processes inside climatic chambers. The monitoring system provides extended information about the ECM phenomenon; on the other hand it could be used for other failure investigations (e.g.: corrosion) as well.

Keyword: electrochemical migration, environmental test

Nowadays, because of the keen competition in the electronic industry, customer requirements must be ranked first. Therefore, it is increasingly important to ensure the reliability and quality of electrical devices by using cost effective technologies. Depending on the applications, the requirements of the customers are different, but all of them would like to know whether the lifetime, quality and reliability of the devices will meet their requirements.
From the aspect of ECM reliability problems, the main topics are investigations of the physical and chemical behaviors on different surface finishes, solder alloys and joints. The Restriction of Hazardous Substances (RoHS) operative directive has just increased the complexity of this challenge as lead bearing solders have to be replaced with lead-free ones. In this context, alternative binary alloys have been examined as replacements for SnPb (traditional) solders, such as near-eutectic SnAg, SnCu, and SnZn alloys. However, ternaries (SnAgCu, SnZnAg, SnZnIn, etc.) and even quaternary alloys (SnZnAgAl, SnAgBiCu, SnInAgSb) have also been studied as candidates for lead-free solders. The reliability investigation of lead-free solders is still a very current issue among the researchers and one of the important topics is the electrochemical migration (ECM) failure phenomenon.

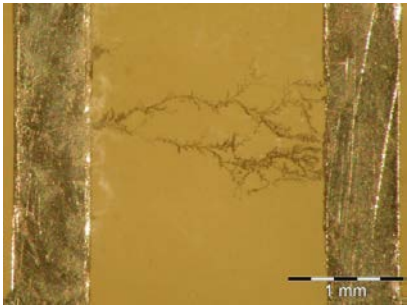

Fig. 1. Dendrites caused by ECM.

The common characteristics of the ECM phenomenon include the presence of moisture on conductor-dielectric-conductor systems under bias voltage, the electrochemical process and the metallic dendrite (see Fig. 1.) growth. This process is driven by an applied electric field from the anode to the cathode. Dendrite growth occurs as a result of metal ions being dissolved into a solution. These escape from the anode and are deposited at the cathode, growing in needle or tree-like formations. This effect causes short-circuits in the electronic circuits, which may lead to a catastrophic failure. Usually, the investigations are carried out in two different scenarios: one of them is done under laboratory circumstances (at room temperature and humidity), while the other one is carried out in extreme climatic conditions. The latter one is carried out by environmental tests, which provide high temperature and humidity levels, while the patterns are followed by some kinds of electrical parameters, such as surface insulation resistance, leakage current or voltage changing. However, the environmental tests provided data mainly about the ECM processes (fault detection) and gave very little useful information about the antecedent processes such as water condensation mechanism and time. Therefore, I have developed an innovative monitoring system, which allows "in-situ" and "real-time" observation of the process of water condensation and the subsequent dendrite formation under extreme conditions.

Budapest, 19 March 2014

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Smart electronics in home appliances

Abstract: Miele is a manufacturer of premium home appliances and machines for commercial use, well known for quality and durability of the products. The presentation provides an insight into the integrated electronics with a focus on the development of electronics.

Keyword: Electronics, Development, Hardware, Simulation

Miele is the world leader in the field of premium domestic appliances, including cooking, baking and steam-cooking appliances, refrigeration products, coffee makers, dishwashers and laundry and floorcare products. This line-up is augmented by dishwashers, washer-extractors and tumble dryers for commercial use as well as washer-disinfectors and sterilisers for use in medical and laboratory applications (Miele Professional).

Miele started very early to integrate electronics into home appliances. The first electronic controlled washing machine was introduced in the late seventies. By 1993, all Miele washing machines and dryers were controlled by microprocessors. Today, electronics is an indispensable part of modern domestic appliances. The use of electronics guarantees perfect results, helps reduce the consumption of energy, water and detergent, makes the operation more comfortable and allows innovative designs. For these reasons, the development and production of electronics is done by Miele itself.

Fig. 1. Electronic appliance control

An electronic circuit board appears at the first glance as an amount of

electronic components which are connected via tracks. However, when one looks a little more closely into the development of electronics, one notices that a lot of disciplines meet here together. This process begins by taking the electrical and mechanical characteristics. Combined with the characteristics of the thermal and lifetime properties of the electronic appliance a very wide and complex field opens here.

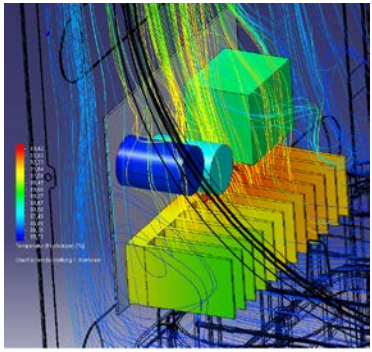

Fig. 2. Thermal simulation of heat sink behavior

Modern simulation tools open up possibilities to effective and target orientated development. That was not possible to achieve in the past. In this case, the thermal simulation of heat sinks (Fig. 2.) and other components can be used as an outstanding example of modern engineering. The thermal simulation allows us to test a variety of different versions, without time-consuming and costly prototypes.

One of the most important ambitions in the Miele development is the lifetime of twenty years for its products. The simulation of the lifetime is only partially possible, so that a lot of effortful and time consuming tests are necessary to guarantee a perfect result. There are still a lot of other things, which have to be taken into account to achieve the one result: a satisfied customer.

Gütersloh, 21.03.2014

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Life-time Prediction of Soldered Joints

Abstract: Study, modelling, investigation and comparison of reliability tests and failure mechanisms of micro-electronic packages soldered on laminate substrates are presented. The study is focusing on the principles of accelerated test methods, including standardized, conventional and new ones. Combined life-time test regimes are investigated that provide a better simulation of the real life conditions. In particular the effects of the lead-free reflow process and the self-alignment ability on the quality and life-time of soldered joints are investigated and evaluated. The effect of the reduced solder paste amount to process robustness and reliability is also tested.

Keyword: solder joint, reliability, life-time test, failure mechanism.

Estimation and prediction of the reliability and the life-time of microelectronic modules is one of the most important questions in any applications. The most frequent failure types are delamination, corrosion, joint crack, passivation crack and chip crack. The causes of the failures usually relate to temperature and/or humidity changes.

Solder joint cracking appears at the interface between the solder material and, either the copper pad on the board or the metalized terminal of the component side. Cracking usually propagates almost parallel to the interface and finally causes the break of the joint and the circuit as well. The most common cause of solder joint cracking is temperature change that produces strains in the solder joints due to the mismatch of thermal expansion coefficients (CTE) of the materials resulting in fatigue of the joint. Humidity, in particular, when it is accompanied by higher pressure, can accelerate the propagation of cracking: the moisture penetrates into the cracks, increases the stress there and causes corrosion as well.

Accelerated life-time tests are used to accelerate the formation of failures and thus to shorten the duration of reliability tests.

The different accelerated test methods usually use higher temperature, higher humidity, higher air pressure etc. In order to compare the effect of the acceleration parameters, Thermal Shock (TS), Temperature & Humidity (TH), Highly Accelerated Stress Test (HAST) and their combinations were applied to solder joints fixing different size ceramic chip resistors on FR4 test boards. The test regimes were compared by optical inspection, resistance measurements and shear force tests. Some optical inspection photos are shown in Figure 1.

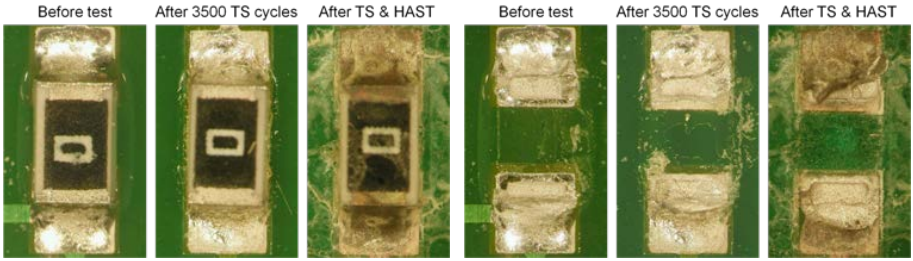

Fig. 1. Optical inspection of soldered joints of 0805 resistors on FR4 board (left) and the photos of the sheared traces of the same broken joints (right)

When modelling the acceleration tests, the Arrhenius-type thermal activation model, the Coffin-Manson (inverse power law) humidity-related relationship and the combined Peck's S-H model were analyzed and compared. The S-H model was found to provide realistic acceleration factor within identified limits of TH tests. However, in case of hard environmental conditions provided by HAST, it is recommended to use higher values for activation energy of diffusion in order to make the model more precise and reliable.

Budapest, 21 March 2014

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DFM Concept Integrated in the Predicted Life Cycle of a New Product

Abstract: According to the Design For Manufacturing concept, the high level of reliability of the electronic modules in condition of cost optimized, request achieving "zero defects" in assembling stage using modern surface mounted technologies (SMT), with respect of the constrains resulted by analyzing entire life cycle of a new electronic product. In the presentation, will be analyzed the influencing factors of manufacturing processes, the most important assembling defects and their causes, will be identified the Key Process Input Variables (KPIV) and proposed a structural model for assembling processes, 4P Soldering Model, as an useful tool in engineering of electronic product in order to assure the assumed goal for assembling stage.

Keyword: Reliability, reflow soldering processes, "zero defects"

In the context of globalization, the pressure weighing on electronic original equipment manufacturers (OEMs) and of those that are contract-based (EMS) in case of new product development requires reducing the conception-production-market time interval, high quality and low production cost in order to ensure the profit margin and

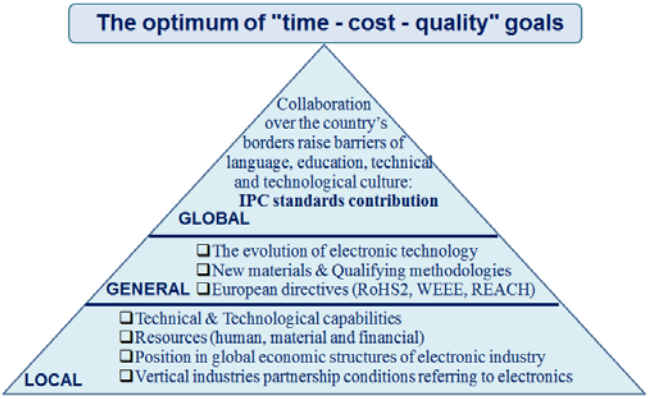

Fig. 1. The influencing factors of manufacturing processes.

therefore aiming to streamline assembly technologies required for assuring the optimum of "time-cost-quality" goals. Achieving a reliable electronic module, shortly and having low production cost, requires consideration of all the local, general and global requirements and constraints which characterize an OEM/EMS entity (Fig.1.) and come to complete those that are required in the conception and design stages according to the development, production and his future use. This means that a multidisciplinary work team will:

- reviewed all aspects derived from the predicted life cycle of this new product and optimize all factors which contribute to its production (manufacture, assembly, test, supply, transportation, delivery, service and recycling);
- identified assembling defects and their causes;
- characterized the Key Process Input Variables (KPIV).

The complex problems of collaboration as multidisciplinary working team, organizing information exchange and establishing their goals, demand a structural model for assembling processes in order to be used for optimizing collaboration between contributors at different levels. The 4P Soldering Model concept is proposed as solution for one of this kind of structural model for reflow soldering processes.

Applying the 4P model a company will be able to ensure the best cost - quality ratio, reliability, reduced time to market and customer satisfaction, thereby improving process performance with notable implications on increasing profits and, ultimately, to increase the company's competitiveness by overcoming manufacturing problems early stages of design and prototype.

Timişoara, 10.04.2014

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Nano-characterization in tin whisker research

Abstract: Since the implementation of the European Union's RoHS regulation, pure tin coatings have been used by the electronics industry in order to replace the traditional Sn/Pb. Unfortunately, tin coatings has a high risk of developing tin whiskers on its surface. Tin whisker can cause short circuits in fine pitch electronics and this phenomenon decreases the reliability of our appliances. Discover how nano-characterization methods are becoming more and more important in today's tin whisker researches in order to find the root causes of whisker growth.

Keyword: tin whisker, nano-characterization, TEM, FIB, SAED

The formation of tin whiskers is a well-known reliability issue in electronics: conductive crystalline tin whiskers (Fig. 1) spontaneously grow from the tin surface finish of the component leads and can cause current leakage or short circuits. Since the implementation of the European Union's RoHS regulation, pure tin coatings have been used by the electronics industry in order to replace the traditional Sn/Pb. Unfortunately, tin coatings has a high risk of developing tin whiskers on its surface due to developing compressive stresses in the tin layer. The stress can originate from residual stresses caused by electroplating; stresses caused by the diffusion of different metals during the intermetallic layer formation or the growth of oxide in the tin layer; and thermally or mechanically induced stresses.

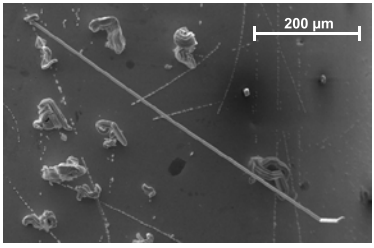

Fig. 1. Tin whiskers

Several years ago, whisker researches started with simple observation of the developed whiskers with optical and electron microscopy. The results were evaluated by statistical methods. The researchers tried to find relations between the parameters of the coating technology and the aging methods, etc... The obtained results were

important steps towards the elimination of whisker, however for deeper understanding of whiskering deeper analyses are necessary.
Concerning the workshop, the presentation will deal with the possible application of nano- characterisation methods – such as Scanning Ion Microscopy (SIM), Transmission Electron Microscopy (TEM), Selected Area Electron Diffraction (SAED) – which could be useful in order to find the root causes of whisker growth.

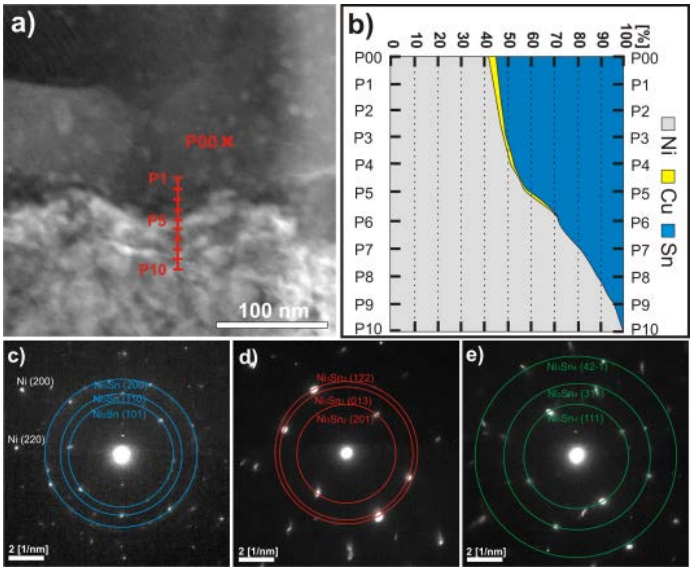

Fig. 2. TEM and SAED analyzes of a whisker root

In the beginning, a sample preparation methods will be summarized, how we can prepare cross-section from the tin whisker for metallurgical and microstructural analyses (Fig. 2). Then the latest results obtained by nano-characterisation in the field of tin whiskers will be presented.

Budapest, 09.04.2014

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TIE 2014
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Sponsored by:

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Sponsored by: Continental

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Sponsored by: Continental

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TIE 2015

New destination, new challenges

Electronic components and systems are essential for Romanian industrial development. They underpin product and productivity innovation across the whole economy and play a critical role in addressing societal challenges. Based on these ideas, Oradea City Hall developed the Euro Business Industrial Park containing some important companies involved in electronic industry and manufacturing (Celestica, Plexus, Connectronics, Emerson).

Because our industry must cope with fierce global competition, high research costs and the very fast technology development, the answer is to cooperate, pool resources and build common expertise. So, the link between the Oradea industrial park and University of Oradea is very strong.

In spite of the fact that our university is a young one, there are teams of professors deeply involved in developing the connection between industry and technical academic courses. One of them has a growing interest for electronic packaging and therefore, for students professional training.

The Electronics and Telecommunication Department from University of Oradea is aware that a very important target in near future is to develop a network that promotes the development of human resources for innovation in electronics, with the purpose of having a solid Romanian electronics industry.

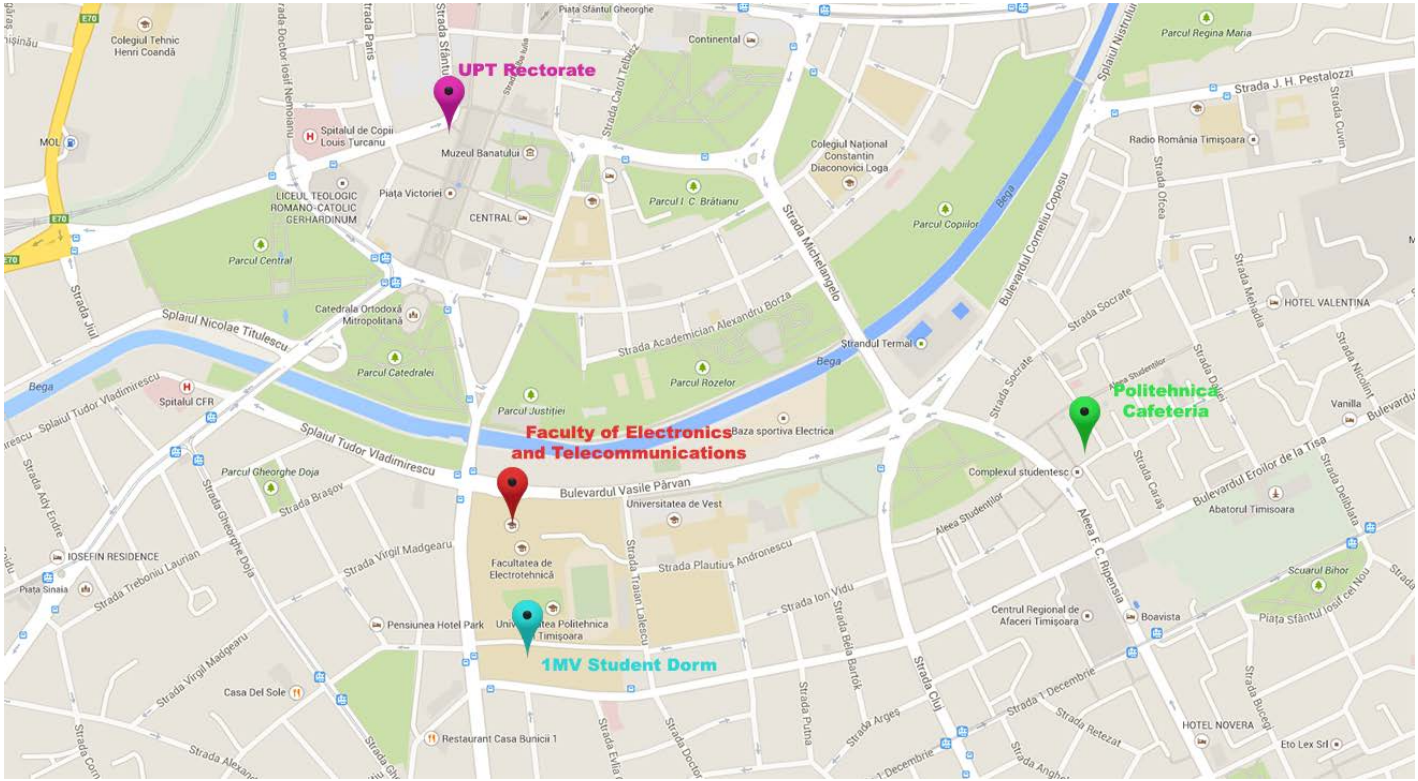
Therefore, our department is a perfect host for the 24th TIE event, which, in 2015, April 22-25, will take place in Oradea. This event will be a chance for companies in the electronics industry and Romanian technical academic environment to unite their interests and activities.

The local organizing committee invites you all to Oradea, a north-west border Romanian city, a multicultural town which is highly appreciated by the different ethnic groups living on the banks on the Crişul Repede River.

See you in Oradea!

Oradea, March 4th, 2014

Prof. Cornelia Emilia Gordan, Ph.D.
Head of Electronics and Telecommunications Department
University of Oradea



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