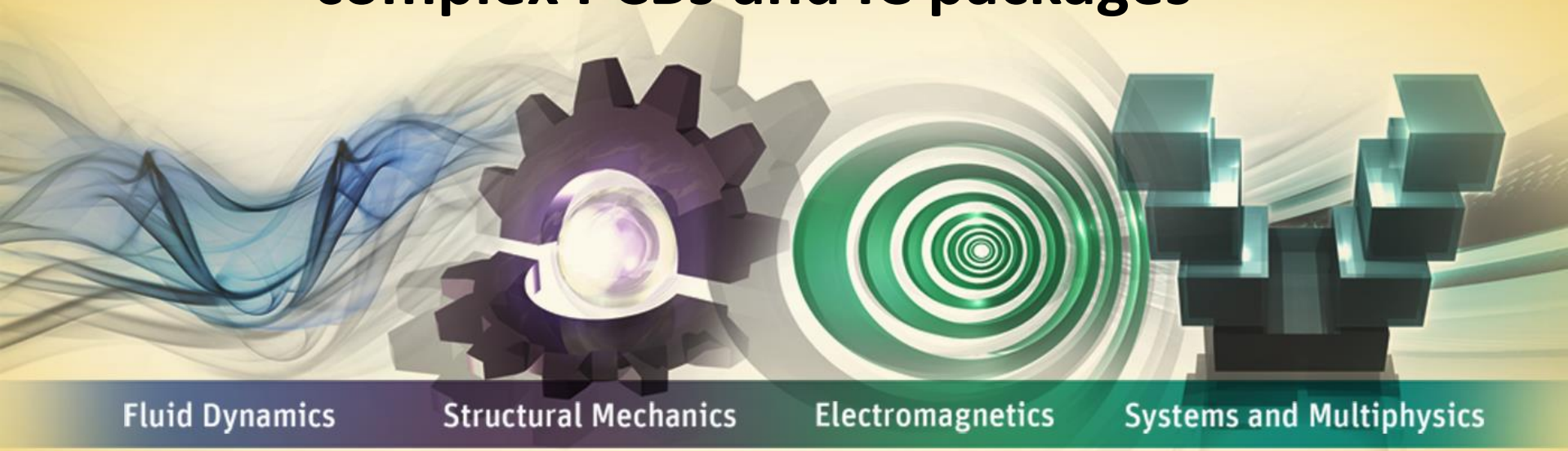
ANSYS

Realize Your Product Promise™

SIwave Training

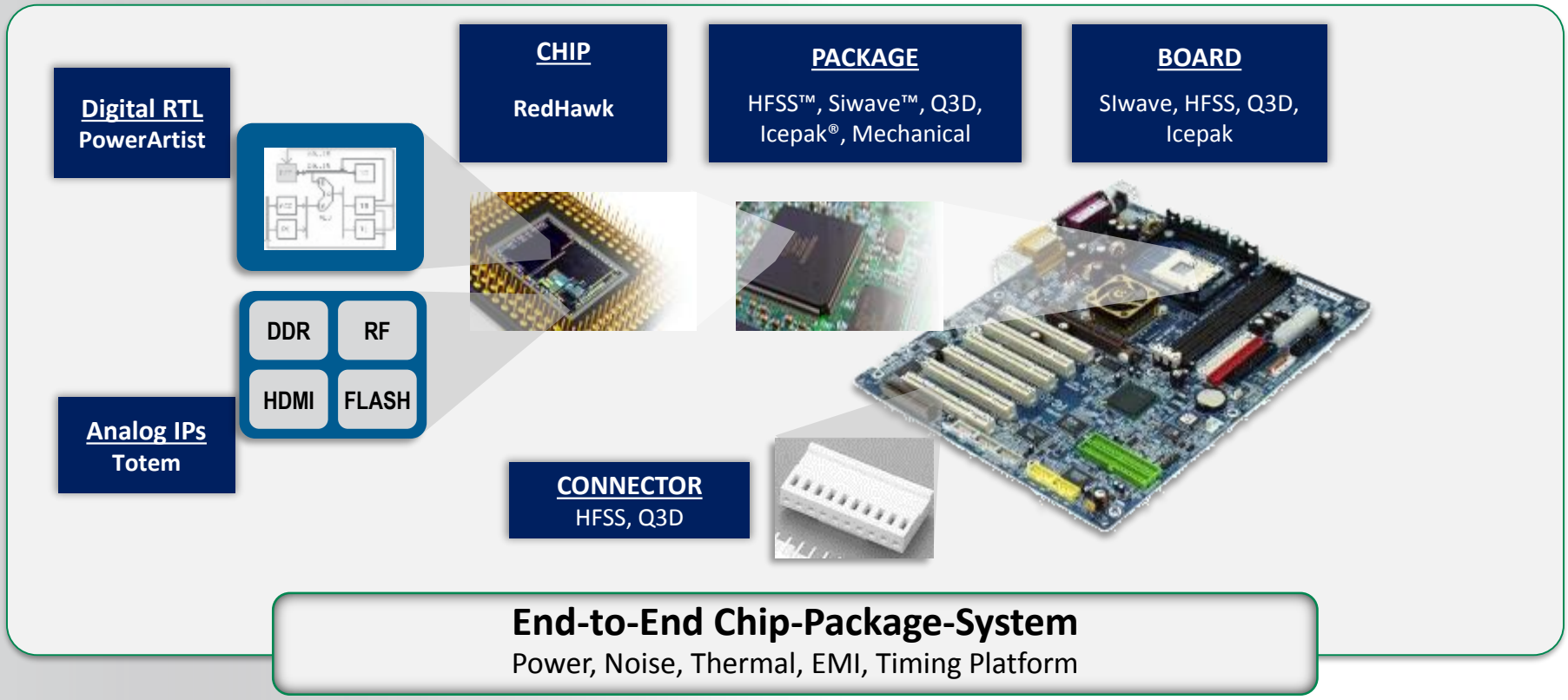
Signal and power Integrity analysis for complex PCBs and IC packages



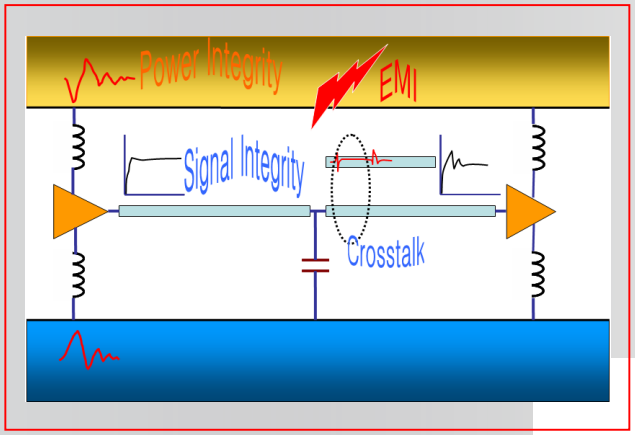
EBU Vision: Electronic Systems

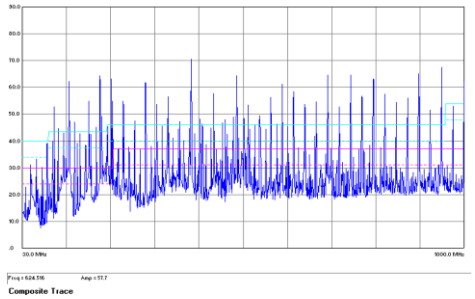
- Signal Integrity
- Power Integrity
- Touchscreen
- EMI/EMC
- Antennas/RF
- Thermal
- Vibration / Stress

ANSYS Electronic Business Unit
Driving Chip-Package-System Convergence



High Speed Digital Design Issues





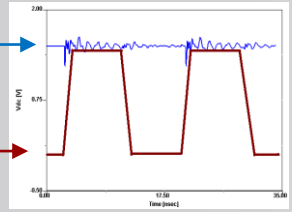
Display Panel

EMI/EMC

- Common mode radiation
- Differential mode radiation

Pwr Noise

Signal

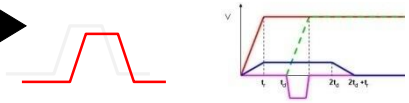


Control IC

Memory

Driver IC

PCB



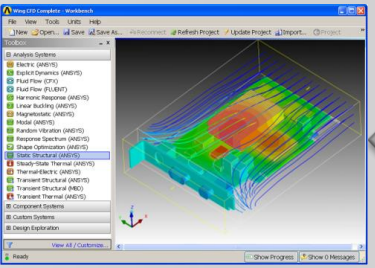
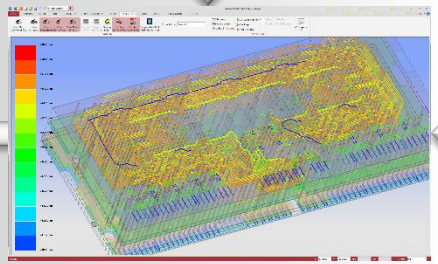
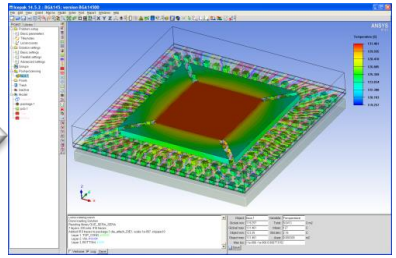
Power Supplies

Power Integrity

- DCIR drop
- Switching Noise (SSO/SSN)
- Impedance Profile
- Power/Gnd Plane Resonance
- Return Path discontinuities

Signal Integrity

- Impedance
- Crosstalk
- Reflection
- Termination
- Dielectric Losses

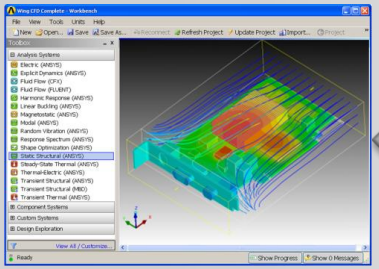
PowerArtist
RedHawk
Totem
RH-CTA
RTL
SoC
Analog/IP
Thermal
IC Extraction



Multi-physics
Workbench
SIwave
Icepak
HFSS
SIwave
PSI Solver
Full-wave Extraction
Q3D (TPA) Solver
Q3D Extractor
CPA Solver
RLC Parasitic Extraction
Nexxim
Circuit Simulation
HSPICE

ANSYS

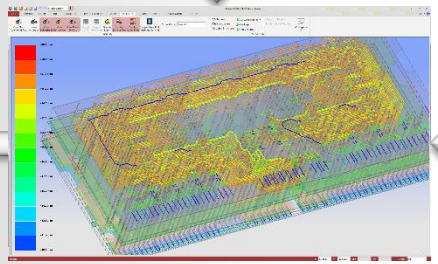
PowerArtist RedHawk Totem RH-CTA

RTL SoC Analog/IP Thermal

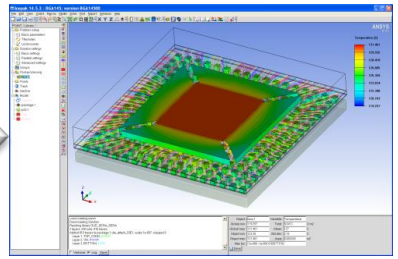
IC Extraction



Workbench



SIwave Core Solvers



Icepak

DC

ALinks for EDA: ECAD Translation

AC SYZ

Plane Resonance

Loop Inductance

Frequency Sweep

PI Advisor: Decoupling Optimization

Near/Far Field

Signal Net Analyzer Z_o & X-talk Scans

SI Circuit Analyses: IBIS, IBIS-AMI, Transient

SIwave-DC

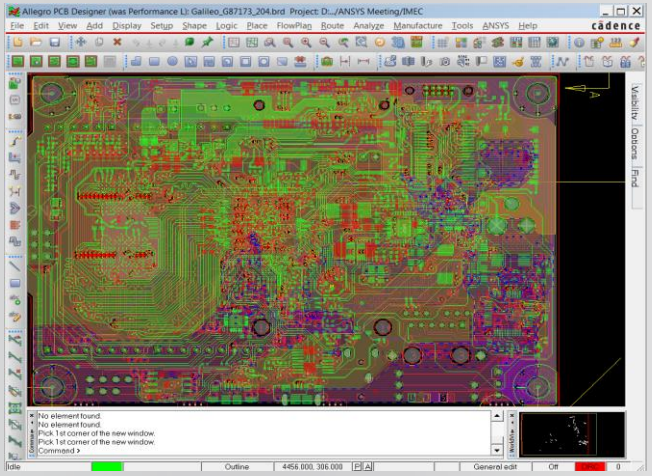
SIwave-PI

SIwave

SIwave

Functionality	SIwave – DC	SIwave – PI	SIwave
ECAD Translation	✓	✓	✓
SIwave & 3D Layout GUI	✓	✓	✓
I^2R DC solver	✓	✓	✓
DC Path Resistance Solver	✓	✓	✓
Leadframe Editor New	✓	✓	✓
Plane Resonance Solver		✓	✓
Automated Decoupling Analysis Optimization		✓	✓
SYZ Solver		✓	✓
Frequency Sweep Solver		✓	✓
Synopsys HSPICE Integration		✓	✓
AEDT Integration AC SYZ Solver Integration New		✓	✓
Zo & Crosstalk Scanner New			✓
TDR Wizard			✓
Near-Field solver			✓
Far-Field Solver			✓
Signal Net Analyzer			✓
Circuit Analysis (IBIS, IBIS-AMI, QE, VE, …)			✓
PSPICE syntax model support in Nexxim New			✓

ANSYS Typical SI/PI Design Flow



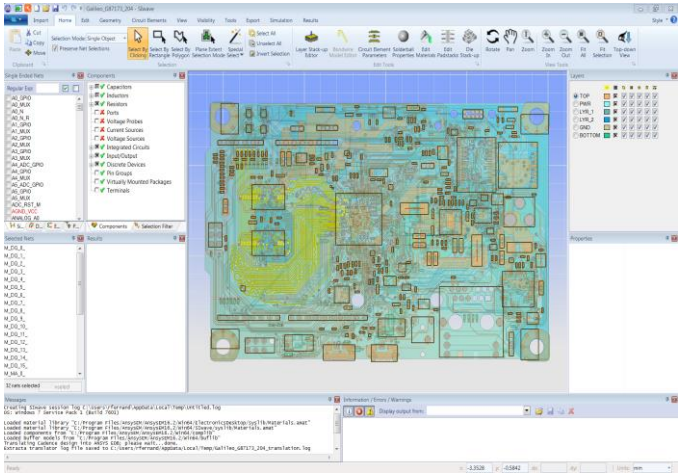
Electronic Design Environment

(Cadence, Mentor, Zuken, Altium ...)

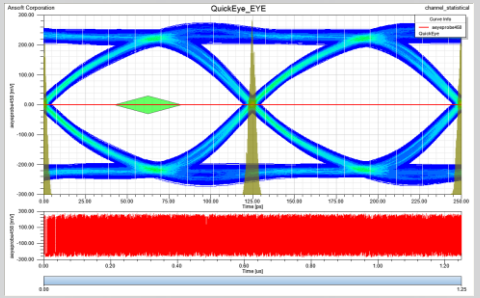
Database Import

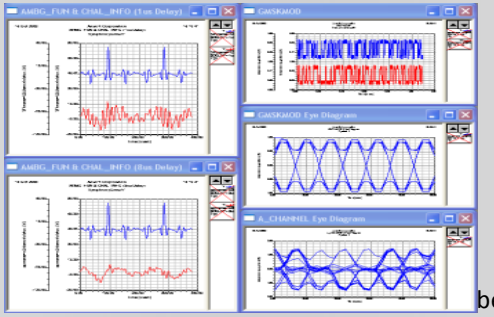
Geometry, Stack up, Components

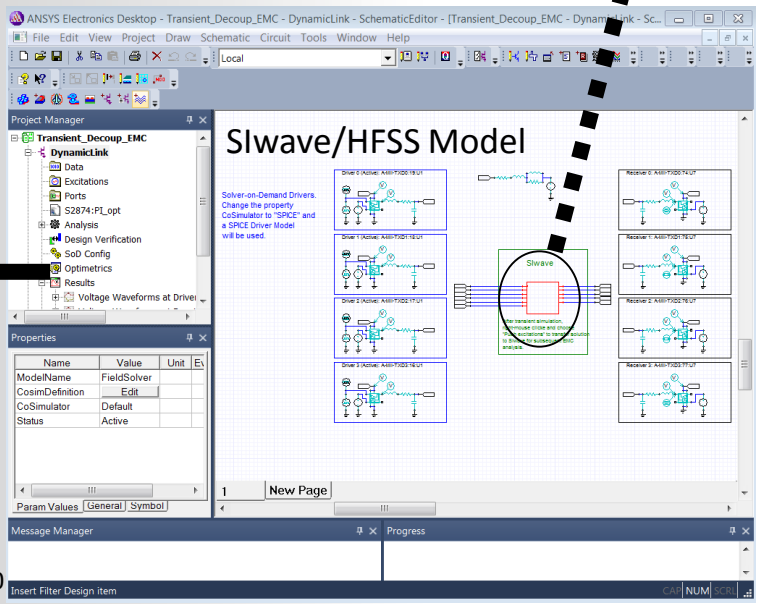
Simulate & Extract Parasitics



Circuit Simulation







EM Model

Spice

S Parameter

Verilog-A

IBIS 5

IBIS AMI

What is ALinks for EDA ™ ?

- Integrate Electrical CAD (ECAD) to ANSYS Software

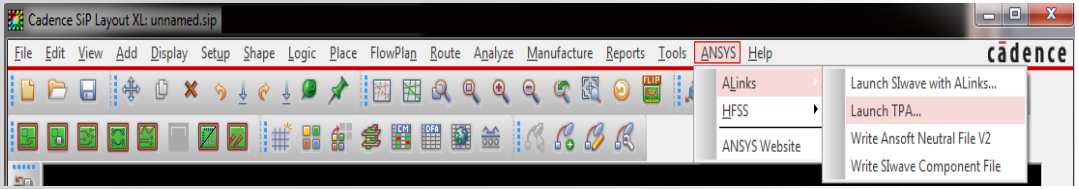
Electronic Design Environment
(Cadence, Mentor, Zuken, Altium ...)

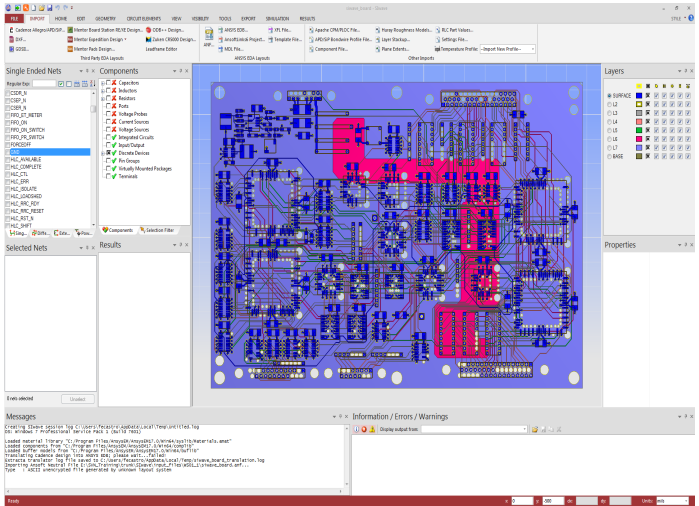
→

ANSYS Simulation Products

- ANSYS ALinks for EDA (once called AnsoftLinks for ECAD) streamlines the transfer of design databases from popular third-party EDA layout tools into ANSYS electromagnetic, thermal and mechanical simulation products. EDA links are available for a number of tools offered by Altium, Cadence, Mentor Graphics, Sigrity and Zuken.

- This license give you access to an **ANSYS menu in your layout tool** (after installing ECADtranslator) and to the **SIwave GUI** to prepare your simulation project.
- *Translator / Editor / Link from a 3rd party layout tool to ANSYS Solvers*





Supported ECAD Translations

Cadence

- Allegro ⇒ 16.0, 16.1, 16.2, 16.3, 16.5, & 16.6
- APD ⇒ 16.0, 16.1, 16.2, 16.3, 16.5, & 16.6
- SiP Digital/RF ⇒ 16.0, 16.1, 16.2, 16.3, 16.5, & 16.6
- Virtuoso ⇒ 5.10, 6.14, 6.15, & 6.16 (Linux only)

Mentor Graphics

- Expedition ⇒ v2005, v2007.1 thru EE7.9 (uses HKP design flow)
- Boardstation ⇒ 8.x (uses HKP design flow)
- Boardstation XE ⇒ v2007, v2007.1, v2007.2, v2007.3 and v2007.7 (uses HKP design flow)
- PADS ⇒ PowerPCB v5.2a, v2005 and v2007 (ASCII Flow)

Zuken (Sold by Zuken)

- CR5000 ⇒ 10 and higher (Zuken translator for .anf & .cmp)
- CR8000 ⇒ 2013 and higher (Zuken translator for .anf & .cmp)

ODB++

- Altium Designer ⇒ R10 and greater
- Mentor Expedition ⇒ EE7.9.1 and greater
- Mentor PADS ⇒ 9.4 and greater
- Zuken Cadstar ⇒ 12.1 and greater

IPC-2581

- Pulsonix ⇒ Revision 8.5 build 5905 and greater
- Altium Designer (BETA) ⇒ v2015 and greater

Other ECAD Formats

- .anf ⇒ ANSYS neutral file format
- .gds ⇒ IC Chip format
- .xfl ⇒ Apache Sentinel format
- .dxf ⇒ AutoCad drawing format

Added Lead Frame Editor capability to SIwave and ANSYS Electronics Desktop

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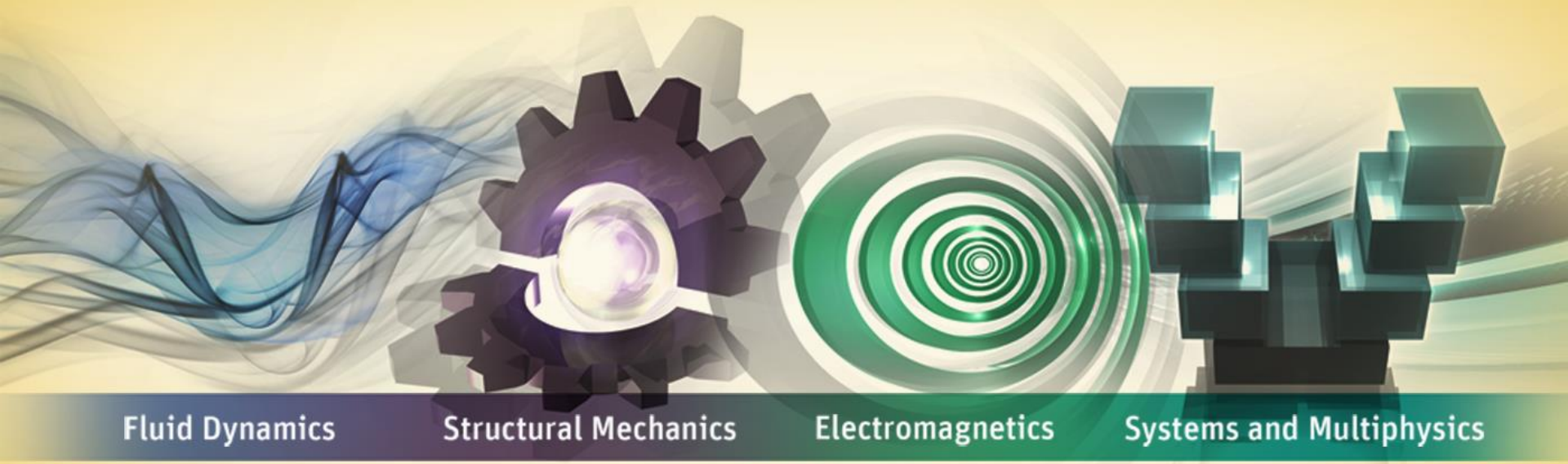
Design Automation for Layout



Software Installation

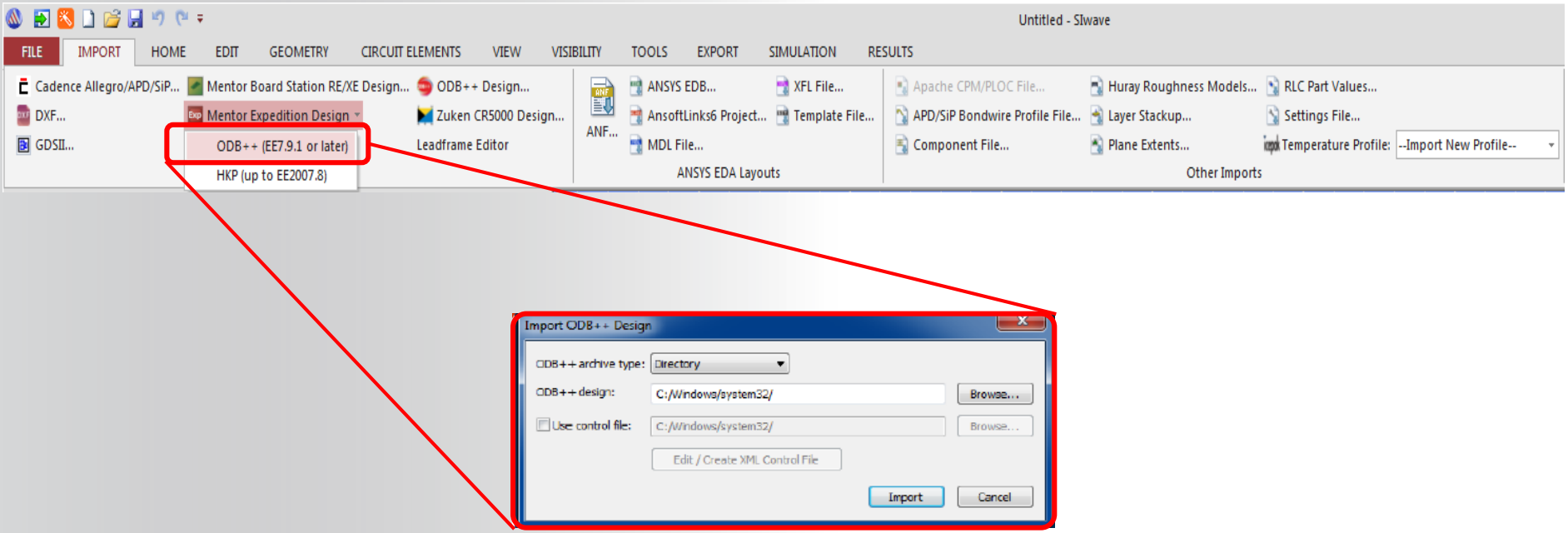
- **Software needed for this training class**
  - **ECADtranslator** (for file translation), **SIwave** and **ANSYS License Manager**
  - A user is able to download all of the above software from ANSYS Customer Portal. Click on **Download > Current Releases (17.x)** and then choose "**ANSYS Electromagnetics products**" to select the above products.

- **ANSYS License Manager installation**
  - ANSYS License Manager package on **Tools** section
  - Specify license server during installation

- **ECAD translators**
  - **ECADtranslator 17.x**
    - It is a common installation Add-on package that will install ANSYS menu in your layout tool. After ECADtranslator installation, a user should see an ANSYS menu item in Cadence Allegro SIP /APD and can translate a layout file to SIwave with Alinks or create an .anf file.

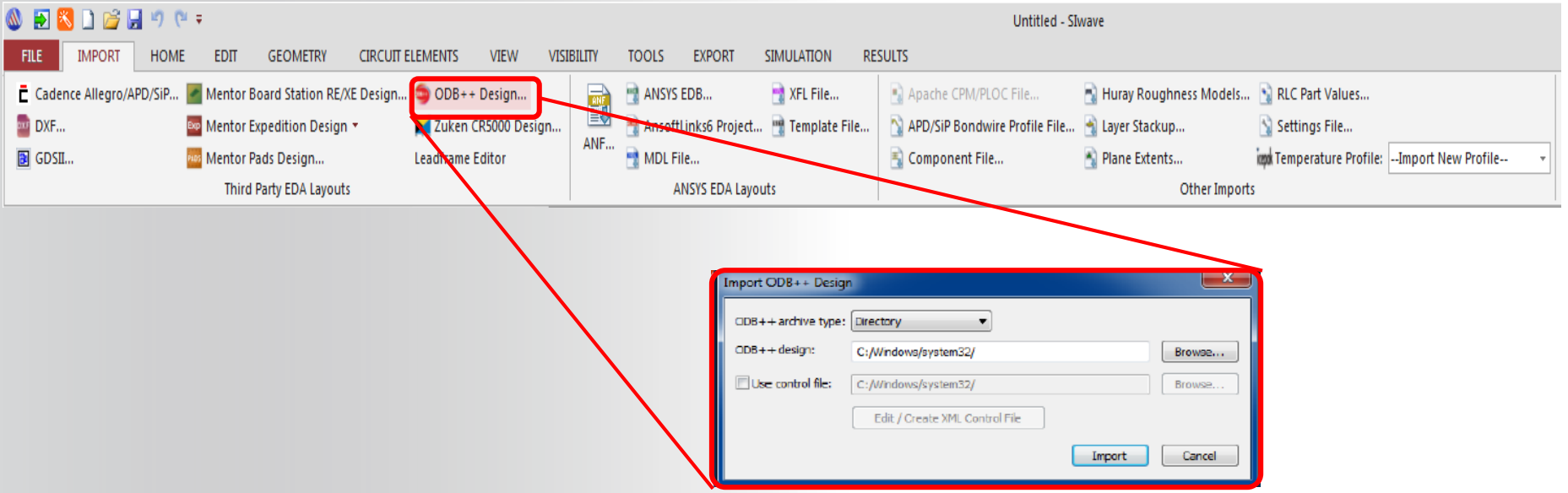
- **SIwave installation**
  - Install **Electronics** primary package : All EM tools will be installed at the same time.

Importing a Layout with ALinks from Mentor



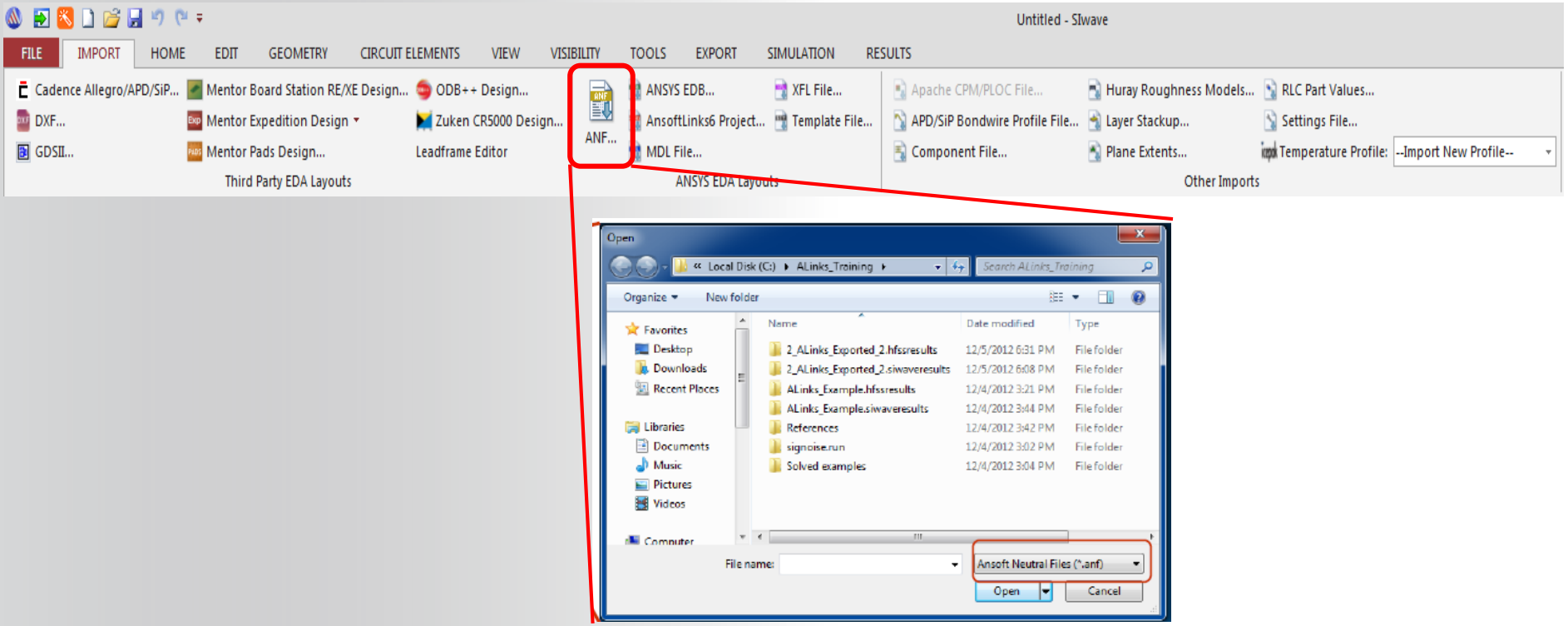
- **Path to import Mentor ODB++ layouts:**
  - **Import > Mentor Expedition Design > ODB++ (EE7.9.1 or later)**

Importing a Layout from a ODB++ Design



- **Path to import ODB++ layouts:**
  - **Import > ODB++ design**

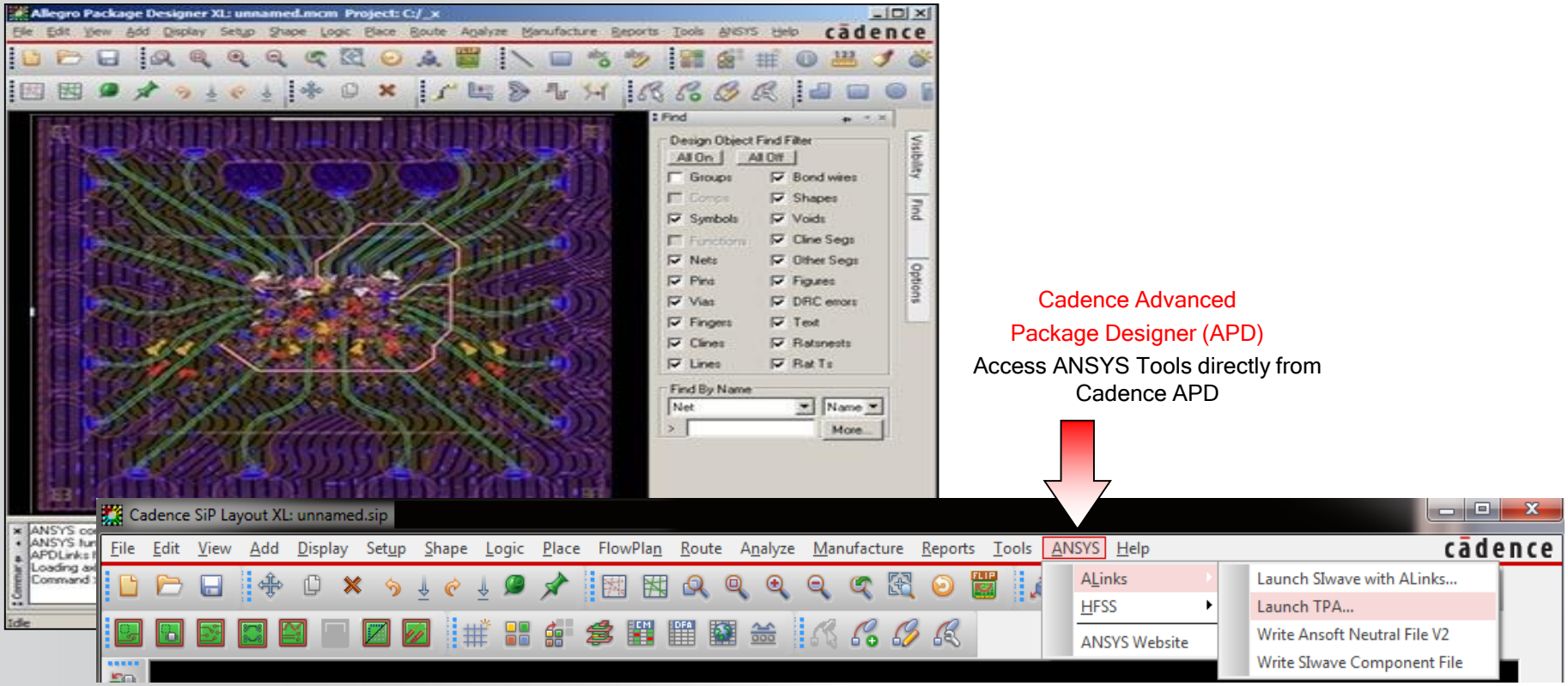
Importing a Layout with ALinks from Zuken



- **The recommended path to import Zuken layouts:**
  - **Import > ANF…**
- **Otherwise use the ASCII files exported from Zuken (.pcf & . Ftf)**
  - **Import > Zuken CR5000 design…**

How to translate Cadence database to ANSYS tools?

- **Two Modes of Operation :**
  - **Direct Launch from 3rd party layout tool**
    - Requires installation of ECAD Integrations executables (**ECADtranslator**)
  - **Stand Alone Editor**
    - Export / Import of .ANF files
- **Here is the view of this integration inside of Cadence APD**

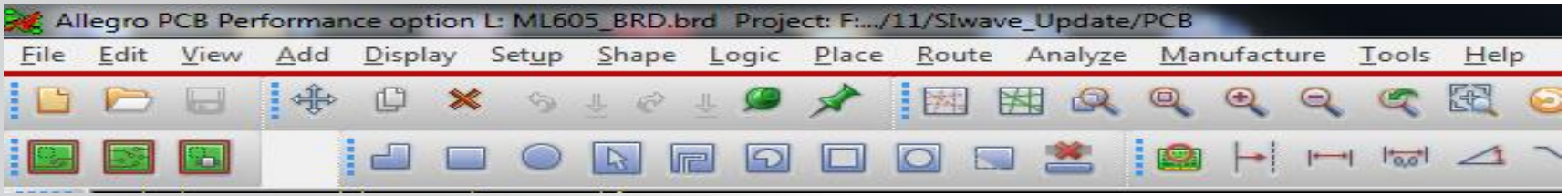


Cadence Advanced Package Designer (APD)

Access ANSYS Tools directly from Cadence APD

Cadence Layout Translation

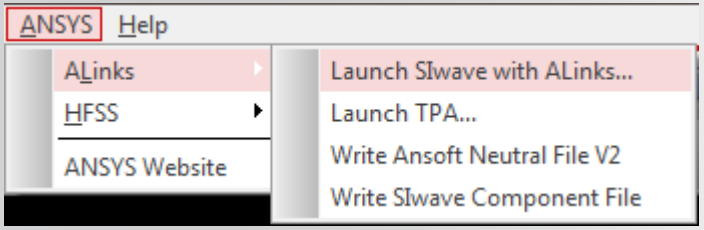
- **Before Integration**

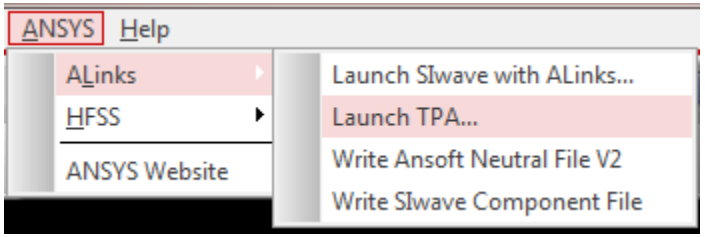


- **After the Integration**

1) Direct link to *SIwave with ALinks*

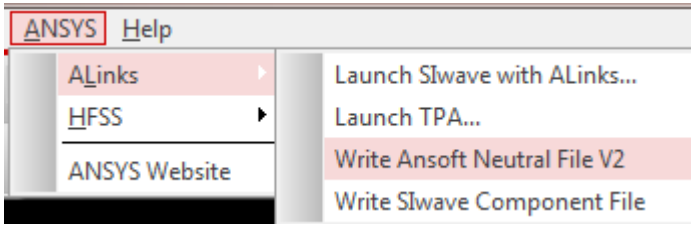
- Cadence and ANYS EM tools are available on the same machine





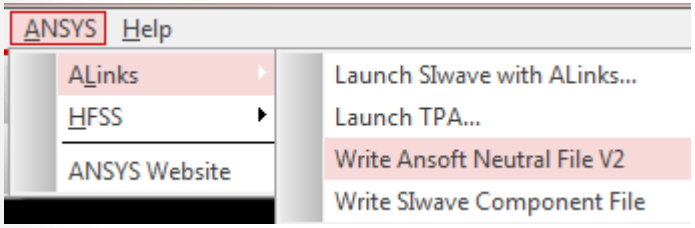
2) Write an .anf file and then import it into *SIwave with ALinks*

– Cadence and ANYS EM tools are installed on different machine

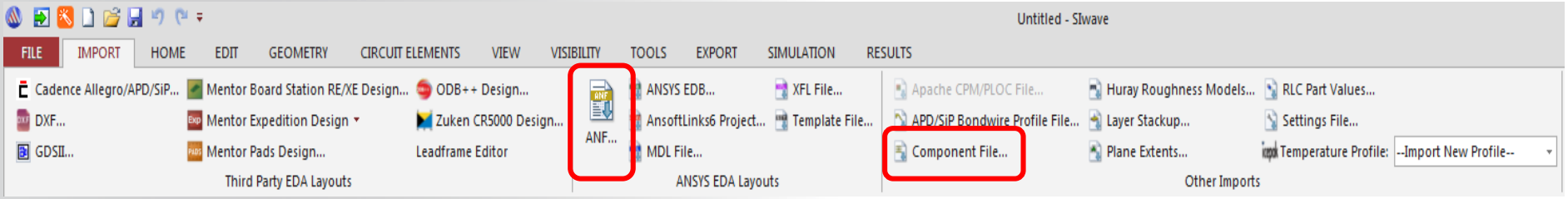


When to use *.anf file?

- **Direct link from Cadence is not appropriate if SIwave is not installed on the same machine. *.anf (Ansoft Neutral File) is required :**
  - Select « Write Ansoft Neutral File v2 »

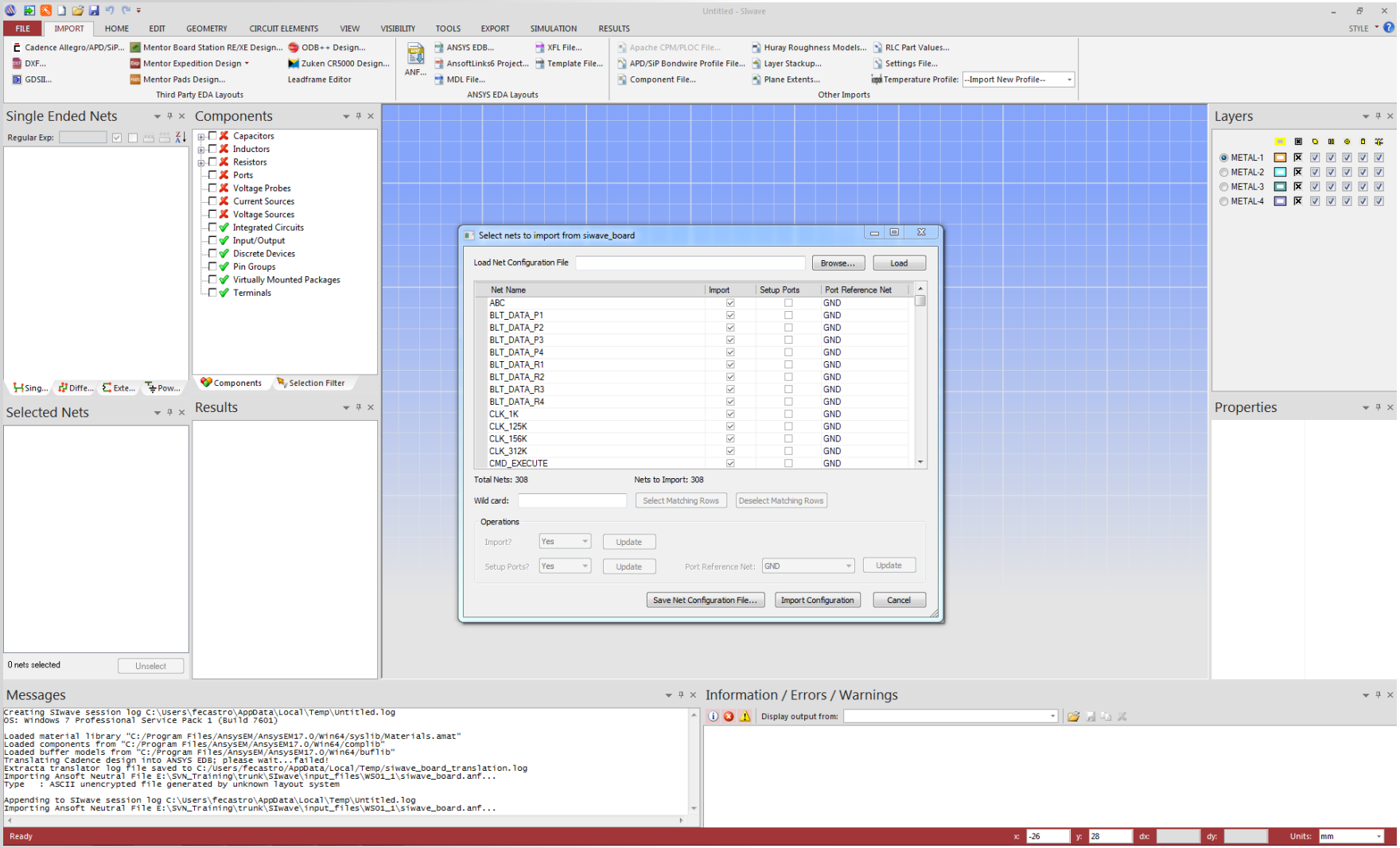


- To get all components, a .cmp file is also required :
  - Select « Write SIwave Component File »
- **Launch SIwave :**
  - File > Import > ANF or Component File…

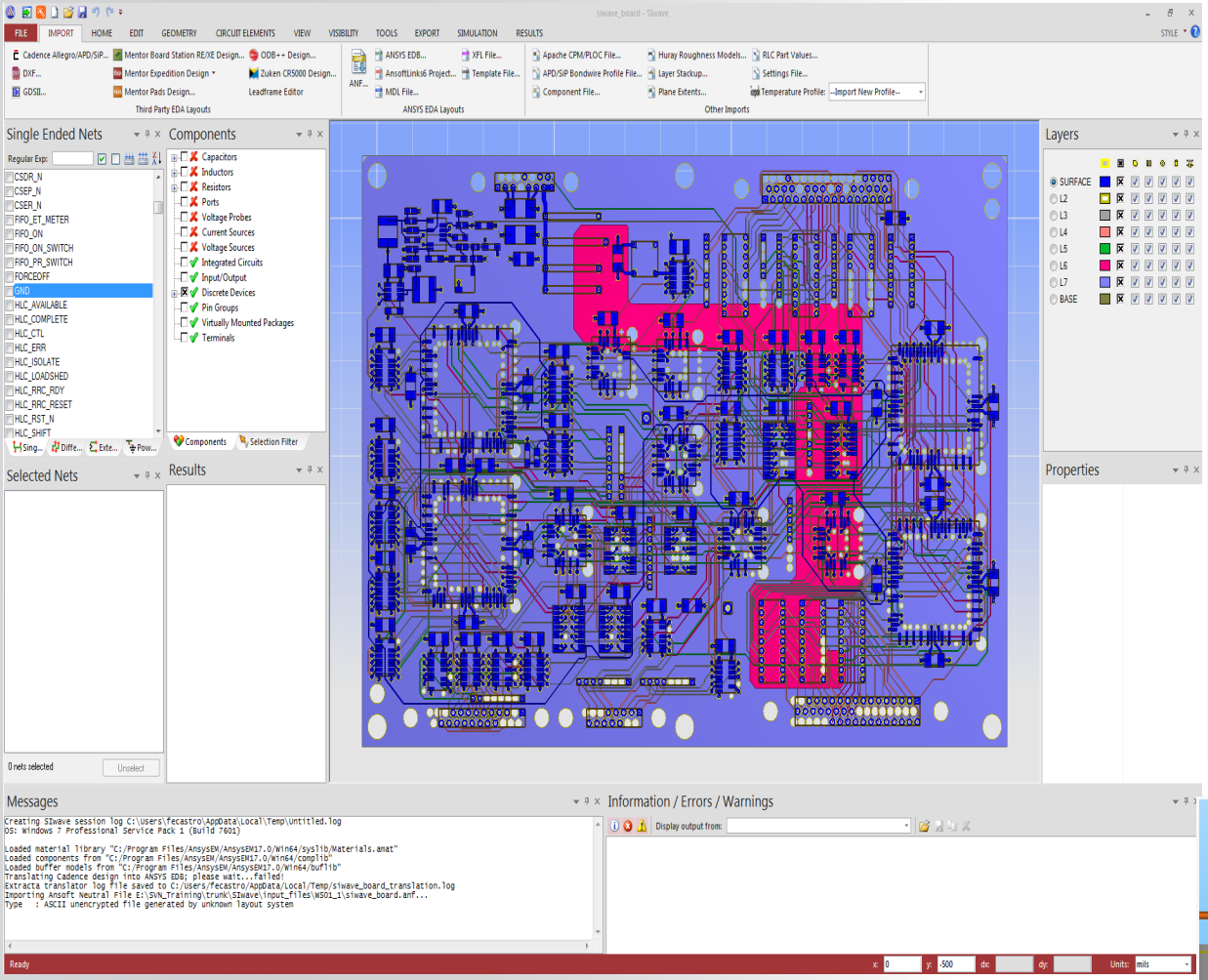


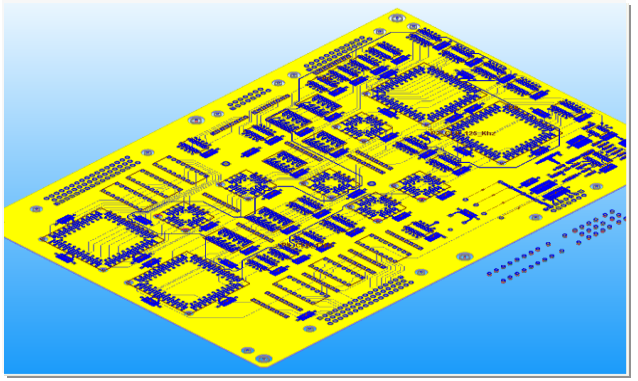
Drag & Drop the Cadence project In SIwave

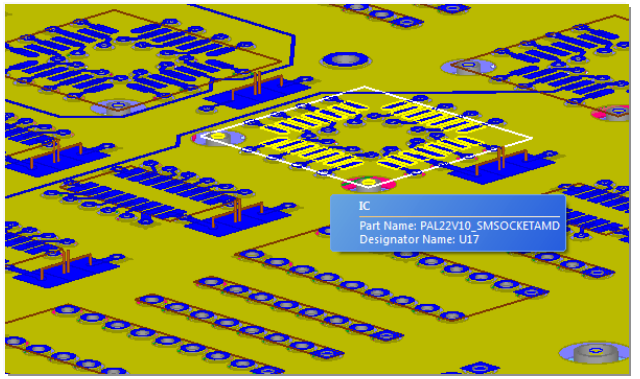
- **Select Nets to import.**

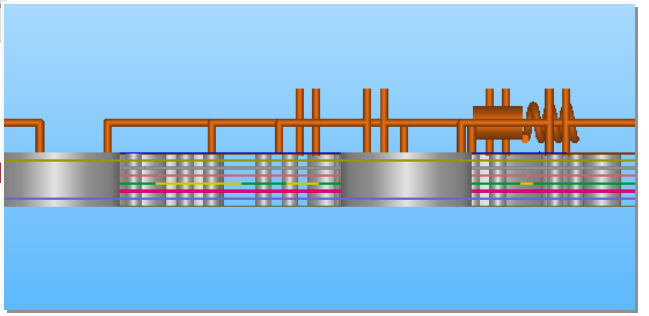


SIwave GUI









- 3D model automatically created

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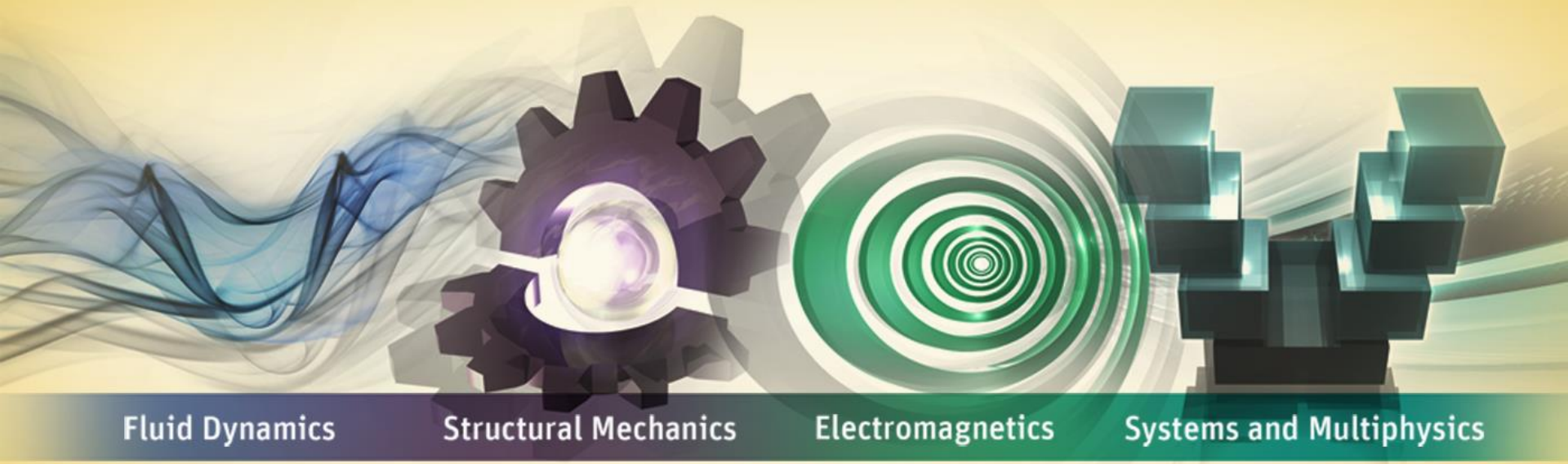
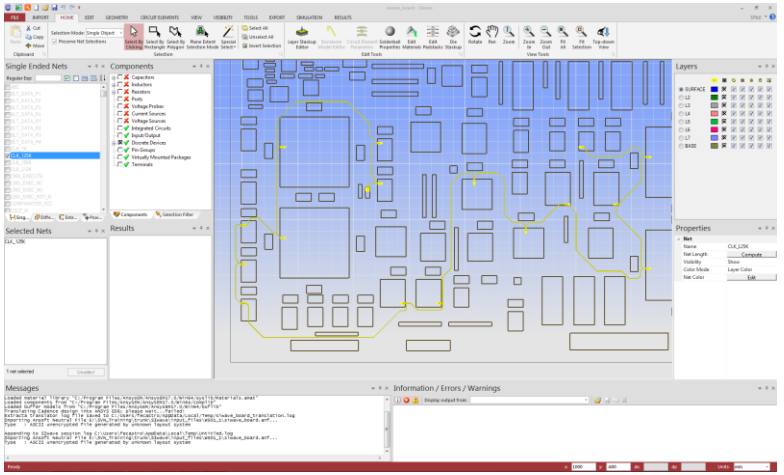
Overview of Siwave GUI

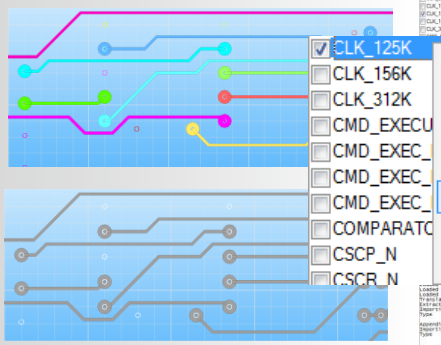


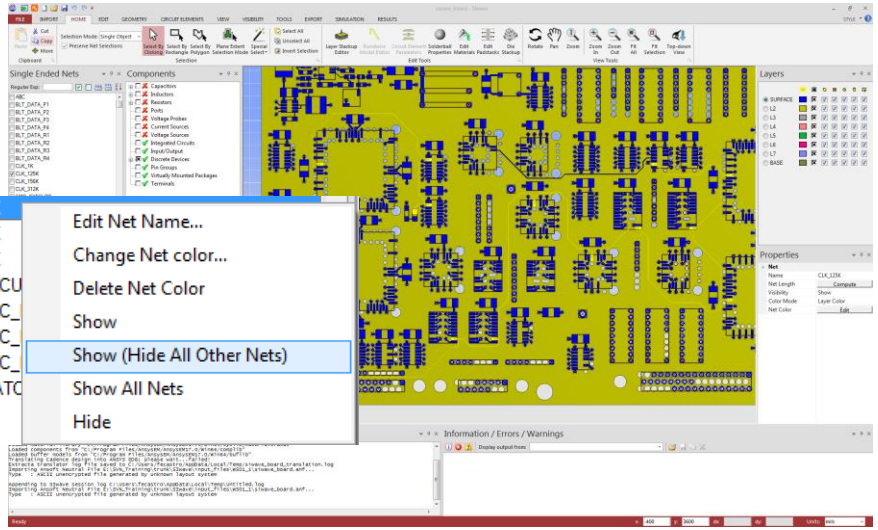
SIwave GUI

GUI Ease of Use Improvements

- Undo/Redo
- Recent project history
- Net Selection Ease of Use
  - Show only highlighted nets
  - Automated differential net identification
  - Automated extended net (ENET) identification
  - Automated pwr/gnd identification
- Net Properties
  - Net properties by hovering cursor
  - Net filtering
  - Detect close edges
  - Measure
  - Check Net Length
  - Calculate Electrical Properties (R, L, C, G, delay, Zo, …)
  - Change Trace Width
- Color Mode
  - Color by layer
  - Color by net
  - Control highlighting color
  - Control background color
  - Control lighting
- Interactive Options
  - Z Stretch
  - LMB Pan, Roller Zoom
  - Dynamic Zoom or Fast Zoom
  - View Cross-section
  - Hot Keys (standard ALT/SHIFT/LMB commands)

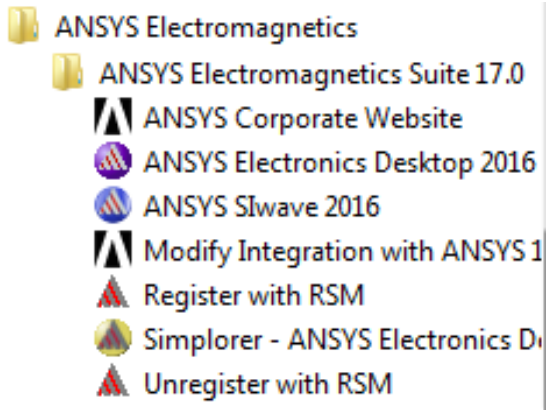






GUI Controls – Desktop

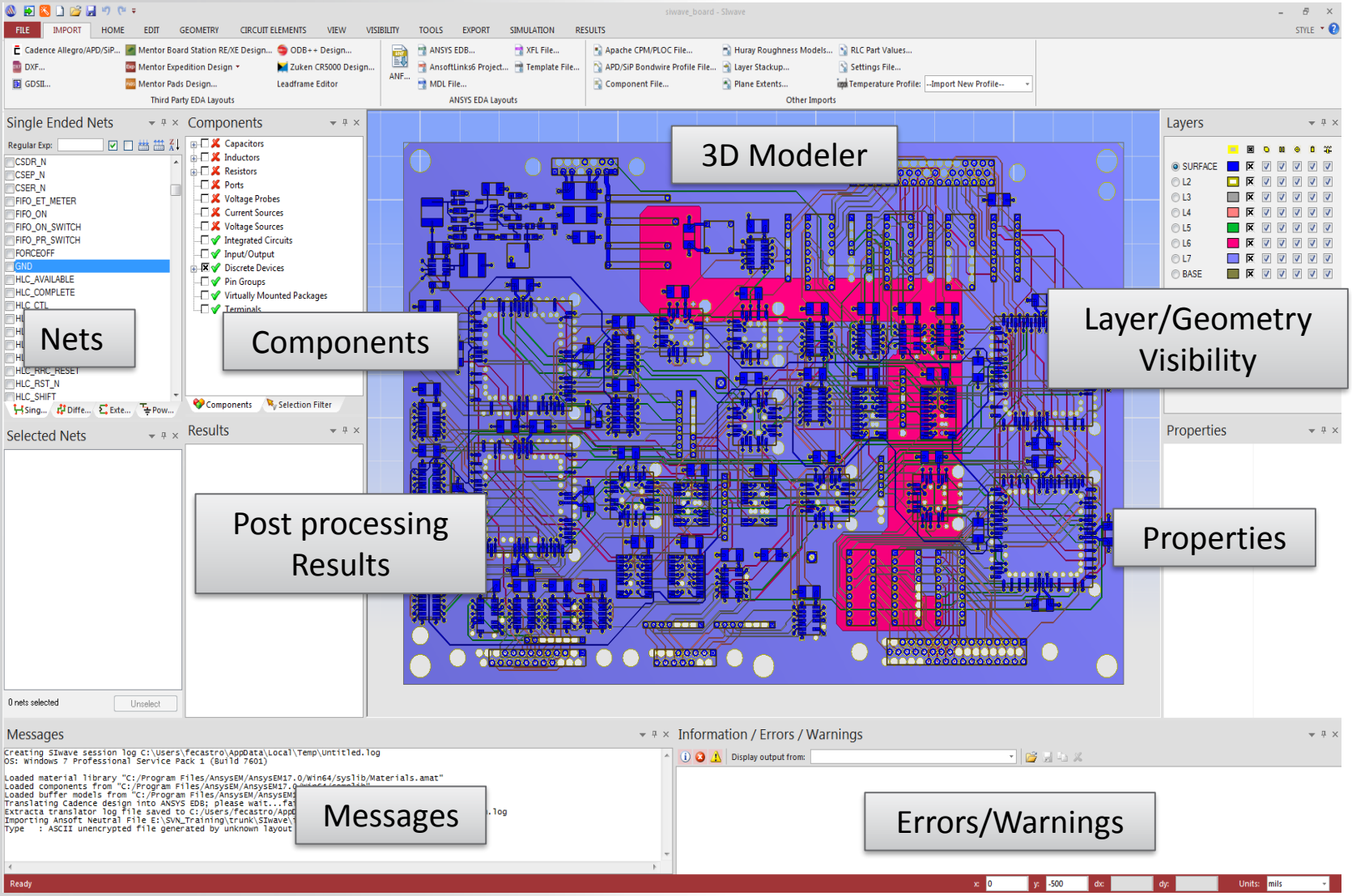
- **Starting SIwave on Windows**
  - **Click the Microsoft Start button**
  - **Select All Programs**
  - **Select Ansys Electromatgnetics Suite 17.0**
    - **ANSYS SIwave**



- **Or Double click on the icon on the Windows Desktop**

- **Starting SIwave on Linux, Go to the install directory :**
  <u>/opt/AnsysEM/AnsysEM17.0/Linux64/</u>
  Siwave

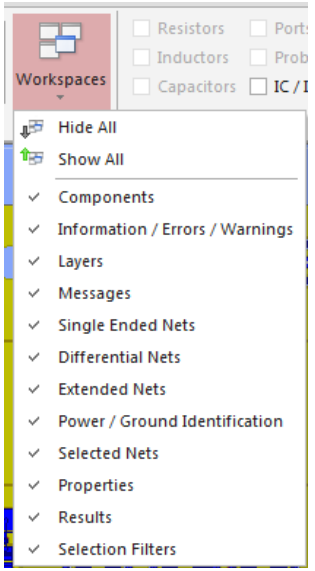
SIwave User Interface



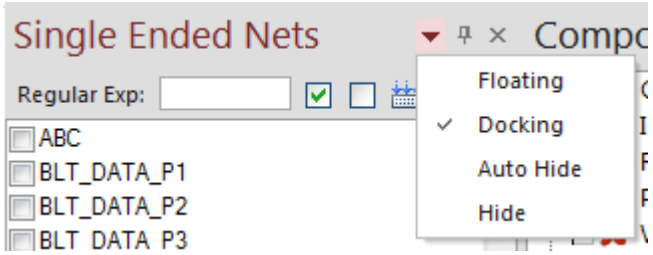
SIwave Workspaces

SIwave Visibility > Workspaces

- The SIwave window has several optional workspaces:
  - Selection Filters
  - Components
  - Information/Errors/Warnings
  - Messages
  - Layers
  - Nets (Single Ended, Differential, Extended, PWR/GND…)
  - Properties
  - Results



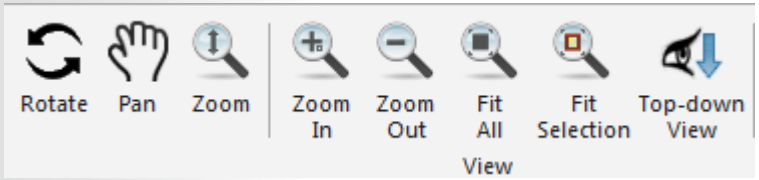
Each window can be Floating or Docking



GUI Controls – View

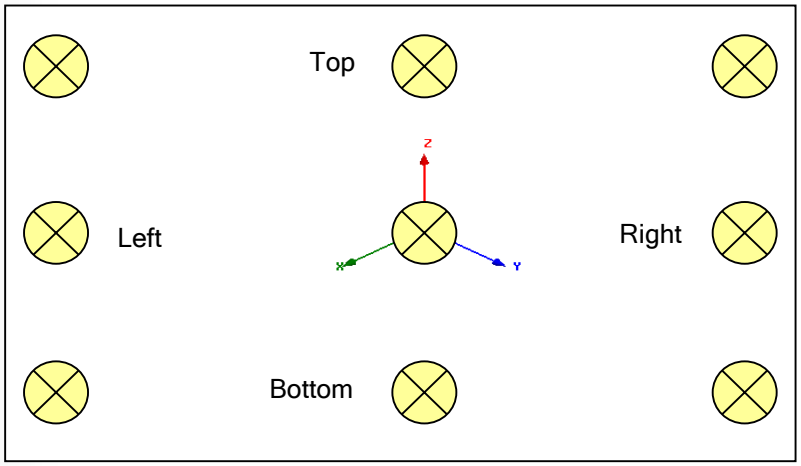
Changing the View

- **Toolbar**



- **Shortcuts**
  - **Since changing the view is a frequently used operation, some useful shortcut keys exist. Press the appropriate keys and drag the mouse with the left button pressed:**
    - **ALT + Drag – Rotate**
      - **In addition, there are 9 pre-defined view angles that can be selected by holding the ALT key and double clicking on the locations shown on the next page.**
    - **Shift + Drag - Pan**
    - **ALT + Shift + Drag – Dynamic Zoom**

Predefined View Angles



GUI Controls – Desktop

Layers Window

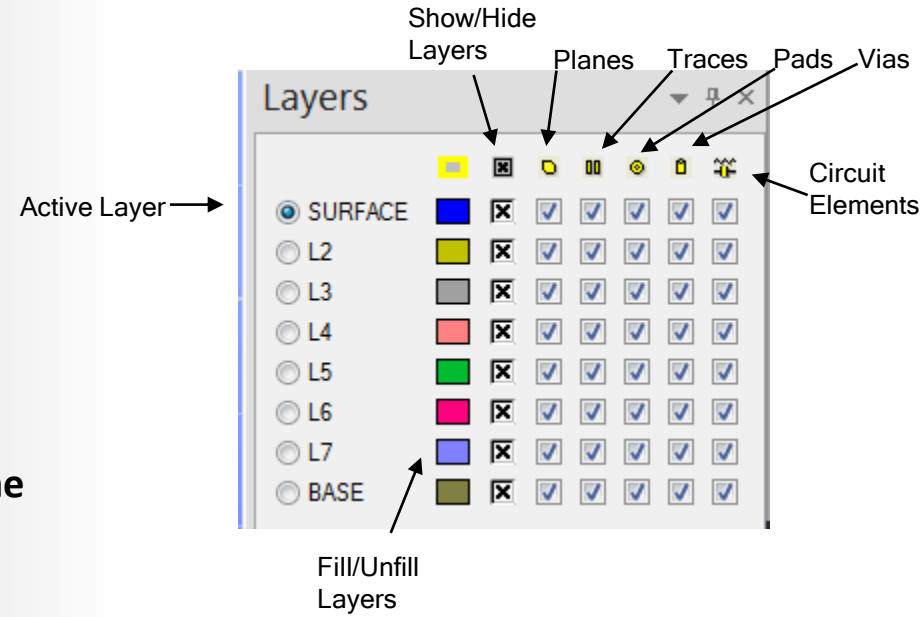
- **Layer Selection**
  - **Select the active layer by clicking on the circular radio button. The active layer is important when geometry is being created in the SIwave interface**

- **Fill/Unfill Layers**
  - **Toggle between Opaque and Wireframe layer views**

- **Show/Hide Layers**
  - **Click the X to either view or hide a layer**

- **To select planes, traces, pads, vias or circuit elements in a particular layer, select the corresponding check boxes**

- **Click on the icons to hide or view all layers**



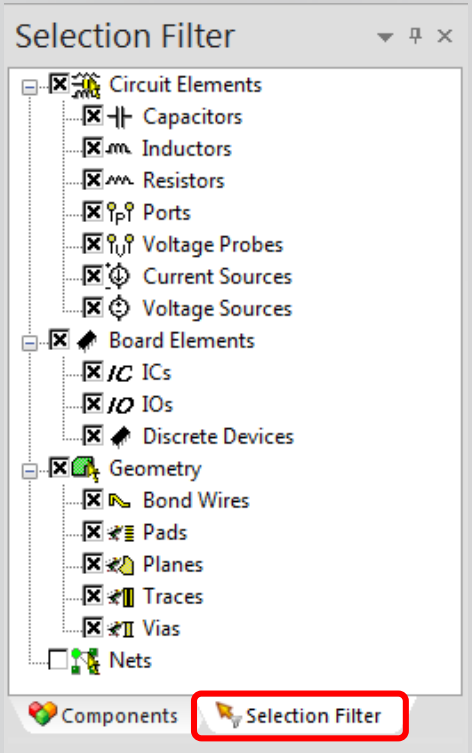
GUI Controls – Desktop

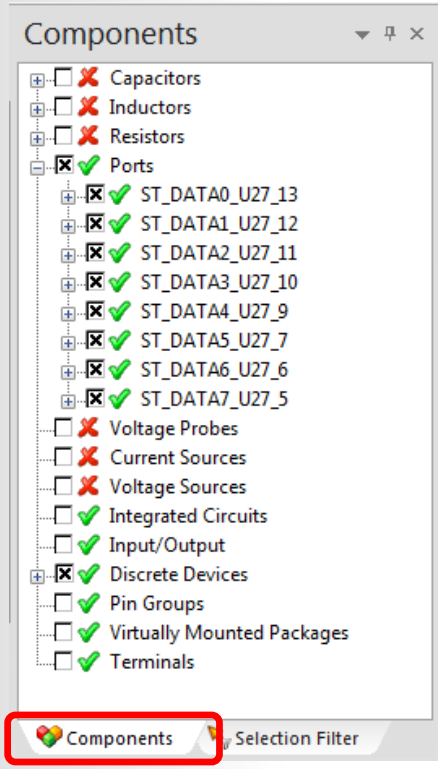
Selection Filter Window

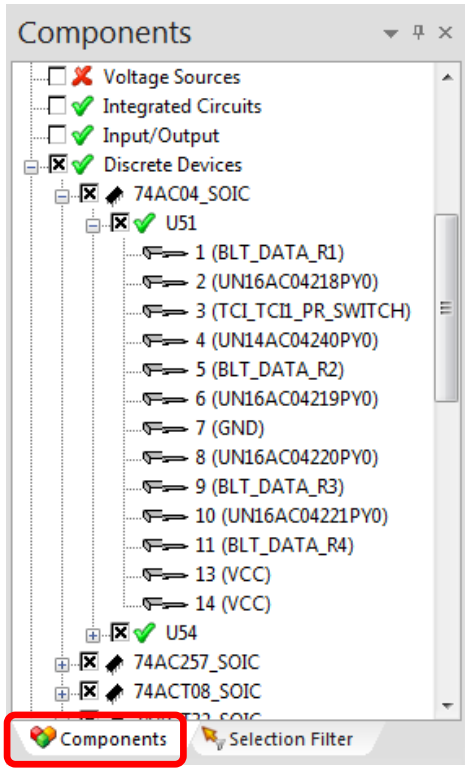
- **Check or uncheck boxes to select certain elements. For example, all types of elements can be selected except for Nets since the box is unchecked**

Components Window

- **For manufacturer supplied components the name, series number, global parts, circuit elements, and pins can be viewed**
- **For local components (created and placed by the user) the part name, circuit elements and pins can be viewed**



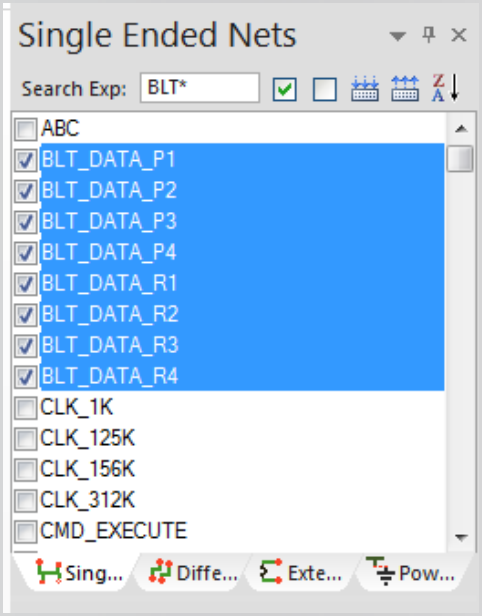


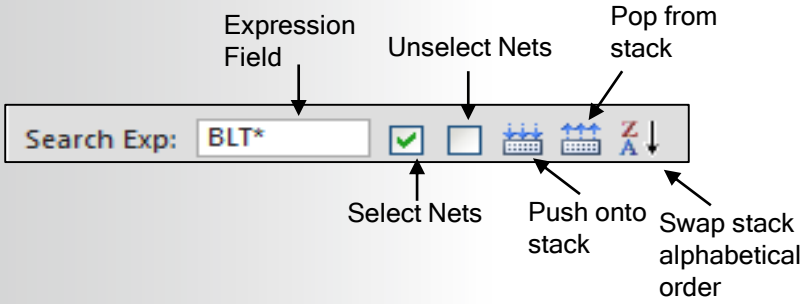


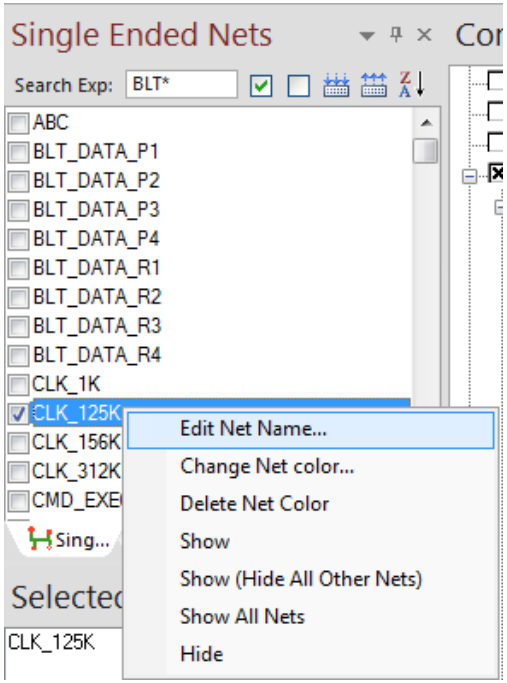
GUI Controls – Desktop

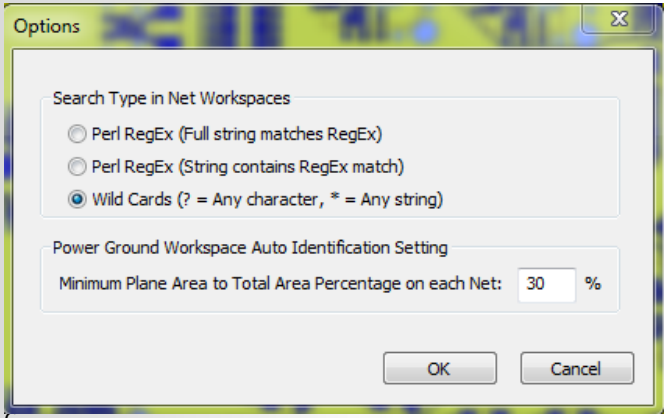
Nets Window

- **Select and Deselect Nets by clicking the checkbox. Also, Nets can be selected and unselected by using a Regular Expression. Note that the expression field is case sensitive and that both * and ? are supported. In the following window BLT_* selects all of the BLT_DATA nets**
- **NOTE: The option *Wild Cards* must be selected in *Tools > Options***





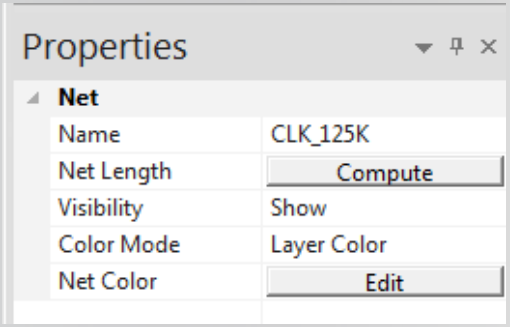




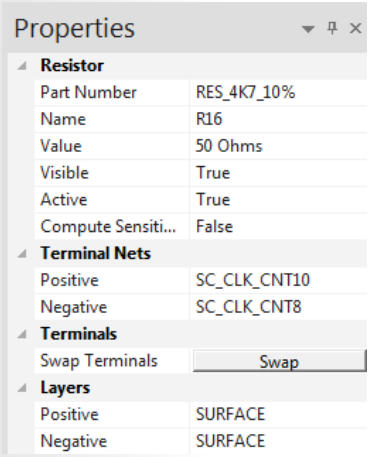
GUI Controls – Desktop

Properties Window

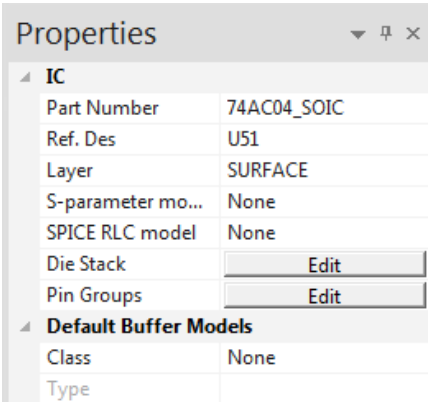
- Information displayed in the Properties Window will vary based on the type of object selected
- Types of Objects that can be selected graphically in the Modeler Window:
  - Circuit Elements
    - Capacitors, Inductors, Resistors
    - Ports, Voltage Probes, Current Sources, Voltage Sources
  - Board Elements
    - ICs
    - IOs
    - Discrete Devices
  - Geometry
    - Bond Wires, Pads, Planes, Traces, Vias
  - Nets



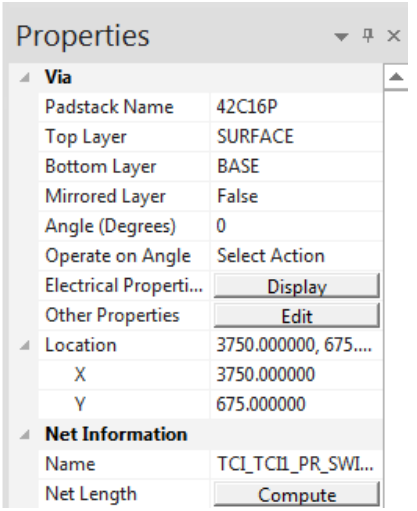
Net Properties



Circuit Element Properties



Board Element Properties

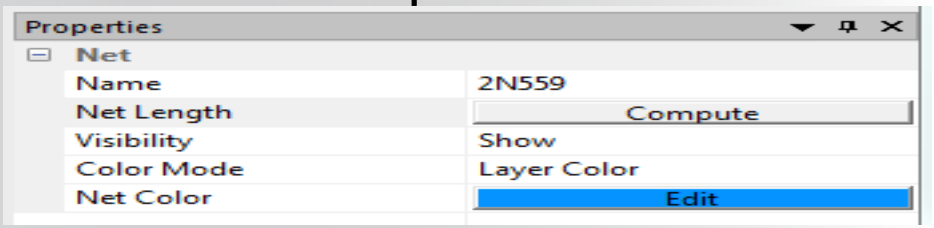


Geometry Properties

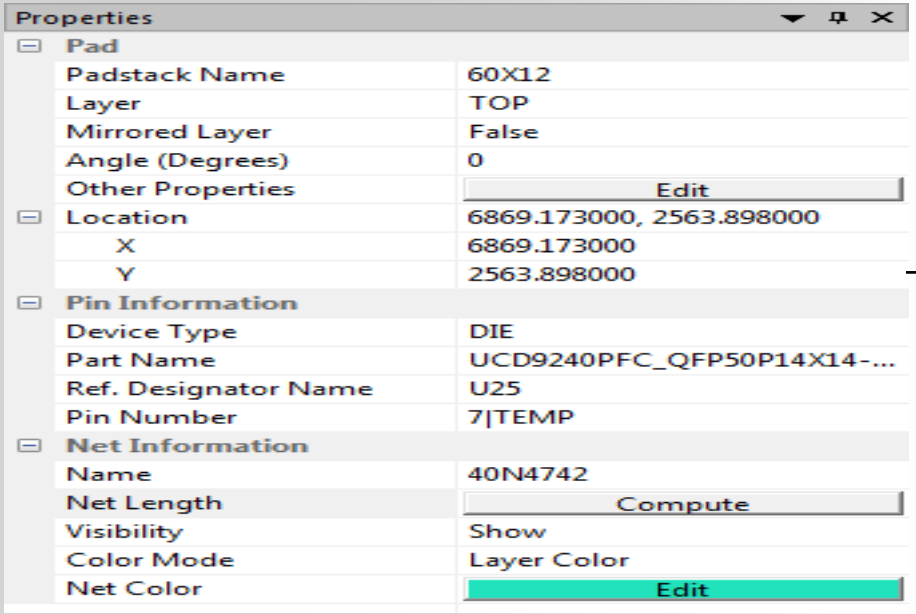
GUI Controls – Desktop

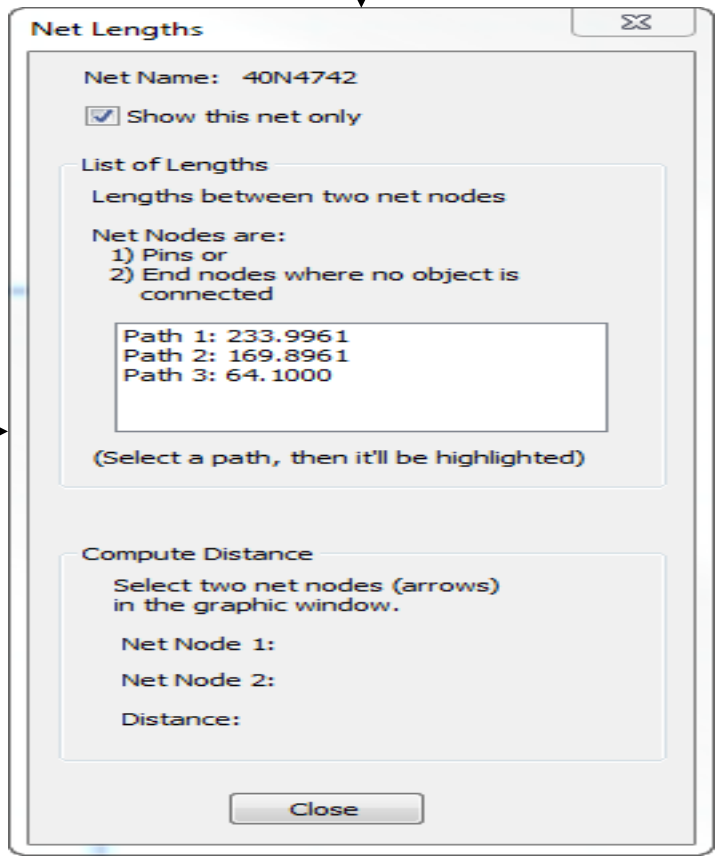
- Geometry
  - Bond Wires, Pads, Planes, Traces, Vias
- Nets

Net Properties

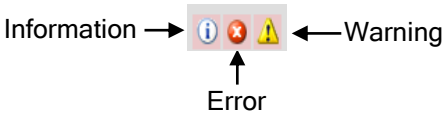


Geometry



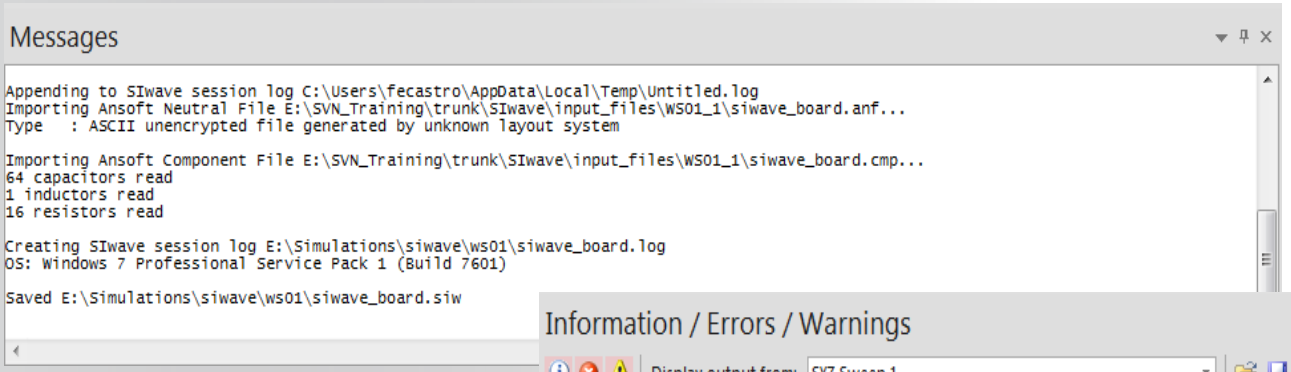


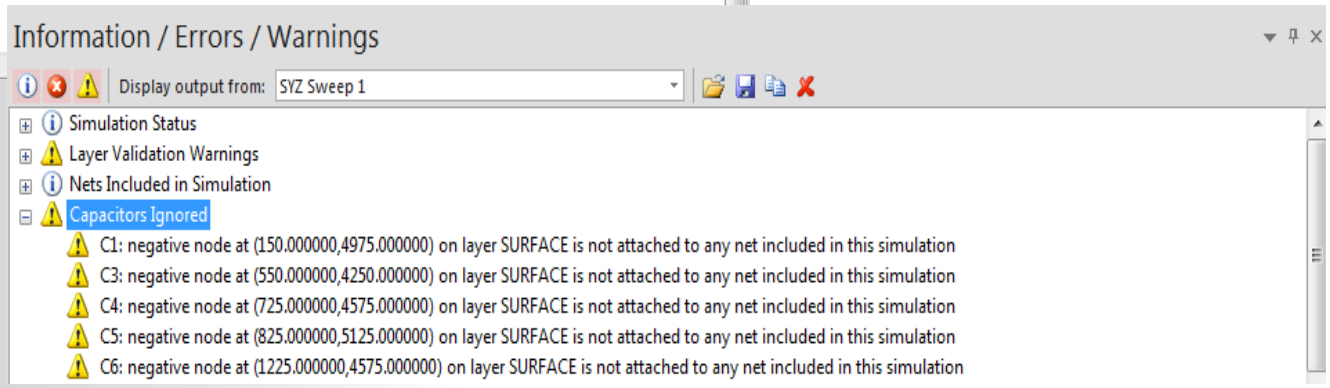
GUI Controls – Desktop



Information/Errors/Warning and Messages Window

- **Messages**
  - **General information related to various tasks will be displayed in the message window.**
- **Information/Errors/Warnings Window**
  - **Errors must be corrected before running the simulation**
  - **Warnings should be further investigated but SIwave will run the simulation**
  - **Information messages should be reviewed**

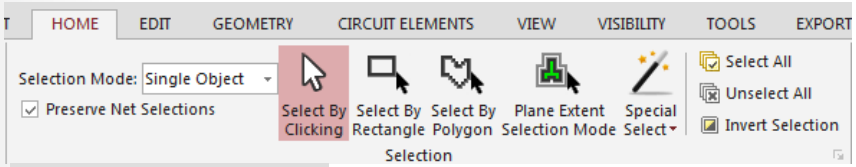


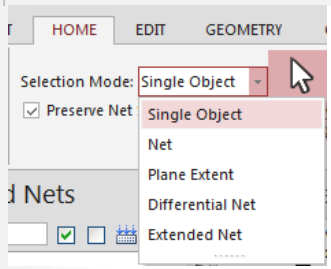


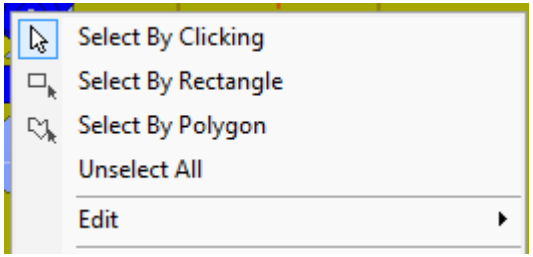
Selecting Mode

Several selecting mode

- **Home > Selection**
- **Right Mouse Button**





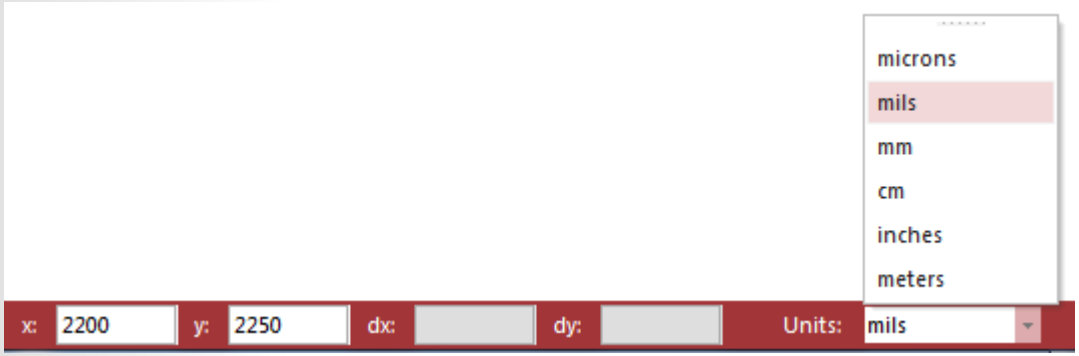


Units :

- **In the Toolbars, set the reference units**
  - **Usefull for drawing, measurement…**

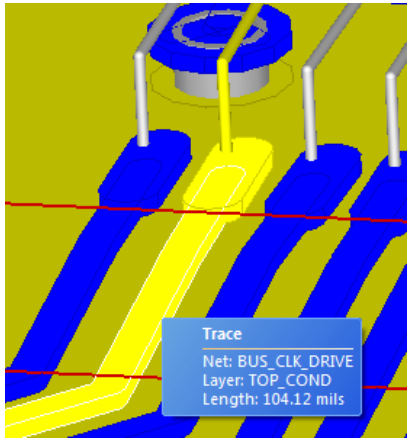
Coordinate of the mouse

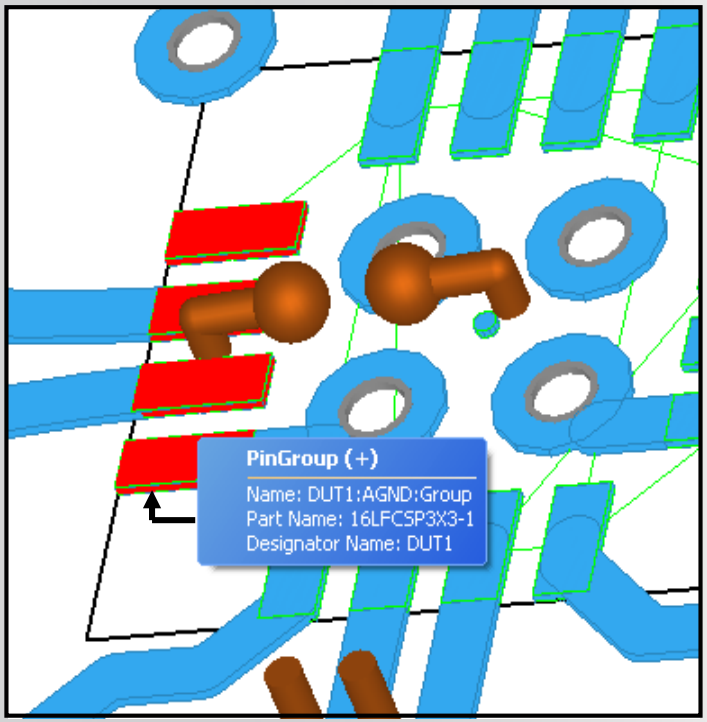
- **In the Toolbars**

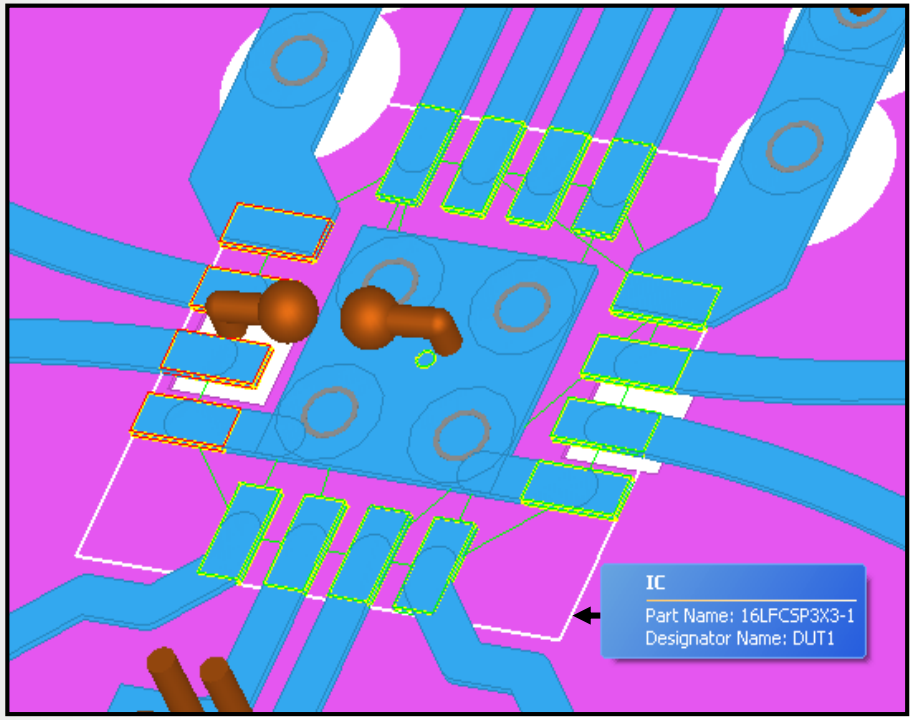


GUI Controls – Cursor Tool-tip

Cursor tool-tip shows information about the selected object: component, trace, net, device, etc

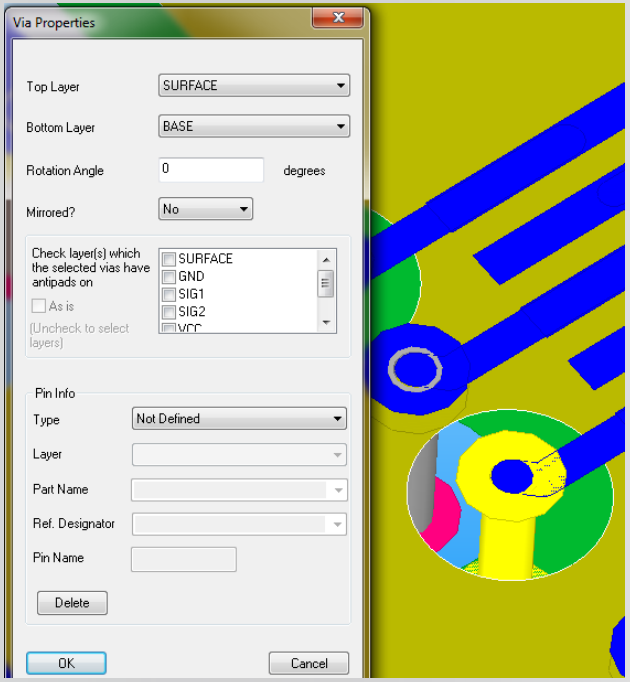


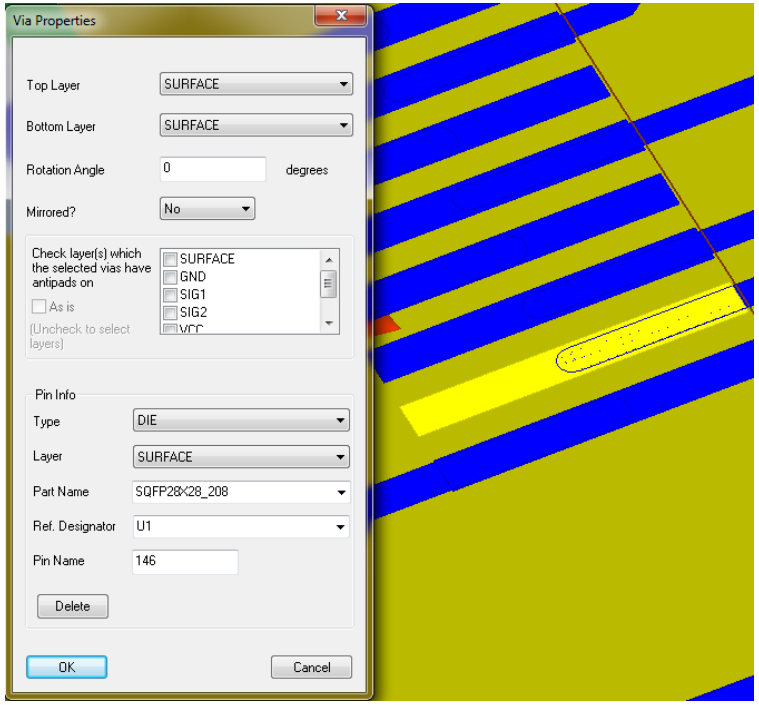




GUI Controls – Via Properties

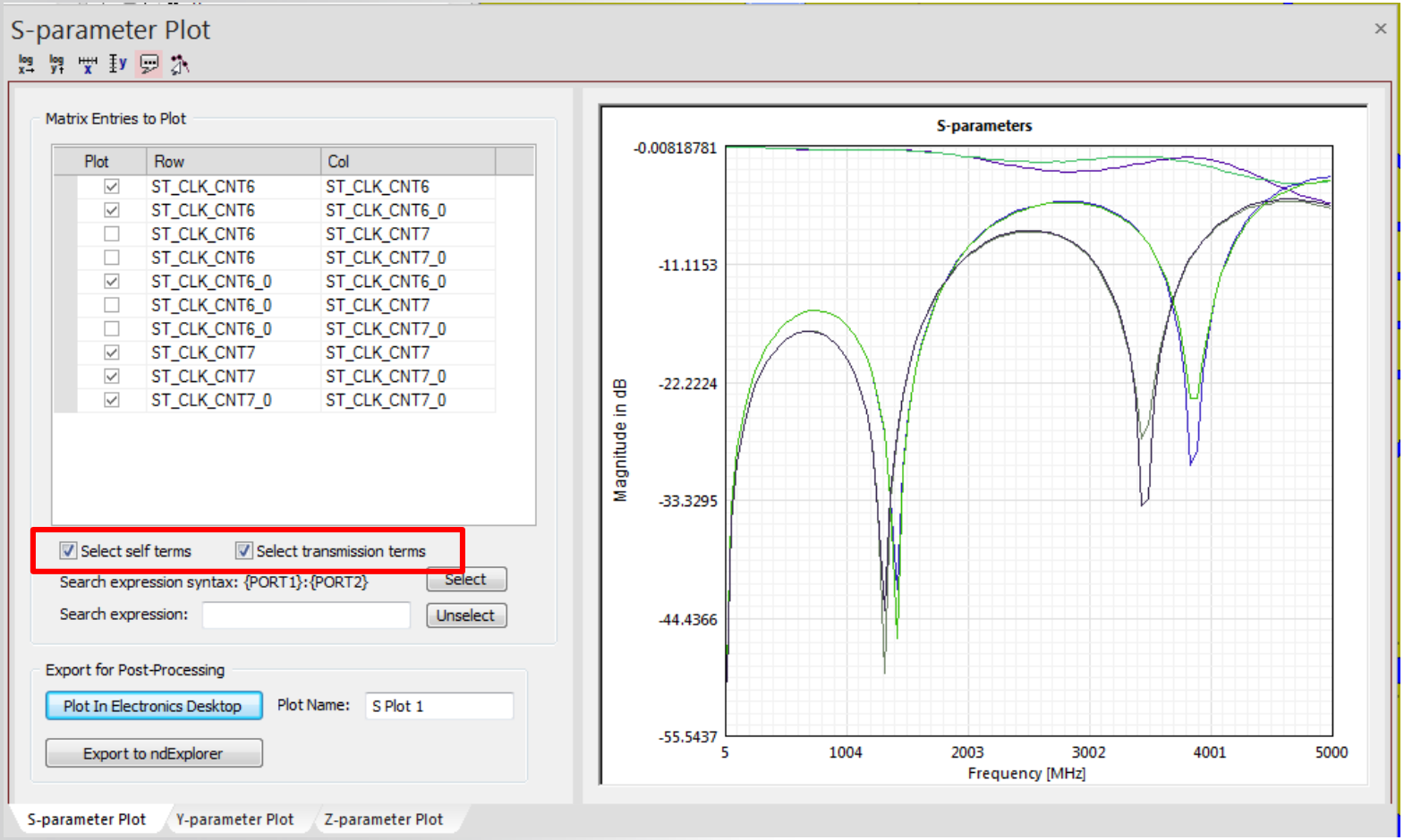
- **Via Properties**
  - Graphically select a via in the layout then select the menu item
    - *Edit > Via…* to bring up the Via Properties Window
  - Editing the properties in this window will override the padstack definition. For example, if a user would like to investigate whether or not to backdrill a via on a high-speed net the bottom layer can be changed. The antipad definition for a particular via can also be investigated without having to change the parameters of all of the other vias that share the same padstack
  - Pin Info provides the Type, Layer, Part Name, Reference Designator and Pin Name for the selected pad. The Part Name, Reference Designator and Pin Names can be edited from here as well





SIwave GUI Controls – Results

- **Plot Self terms or Transmission terms**
- **Click on “**Select self terms**” to quickly plot all the self term**



- **Ideal to plot all the “Reflexions” of the S parameters matrix.**

GUI Controls –Script Commands

Any script language that supports ActiveX objects may be used:

- **VBScript**
- **Jscript**
- **Python**

Extensive scripting support allows automation.

Online Help

- **Script Commands are available**

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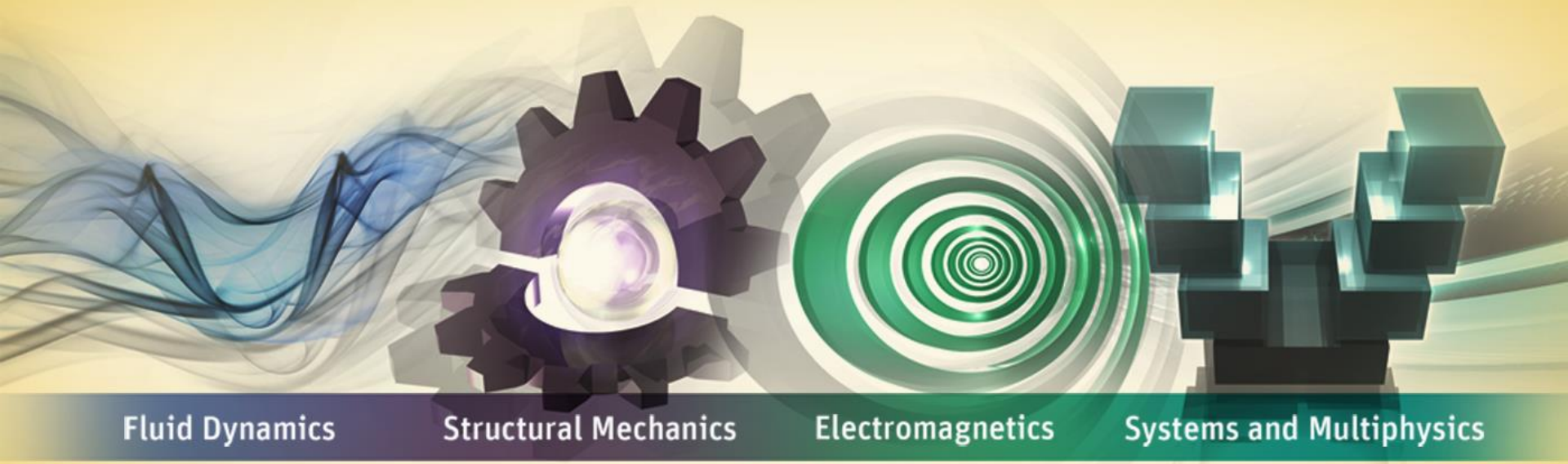
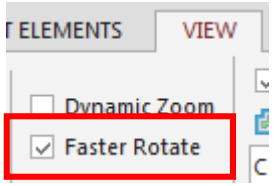
GUI Controls Visualization



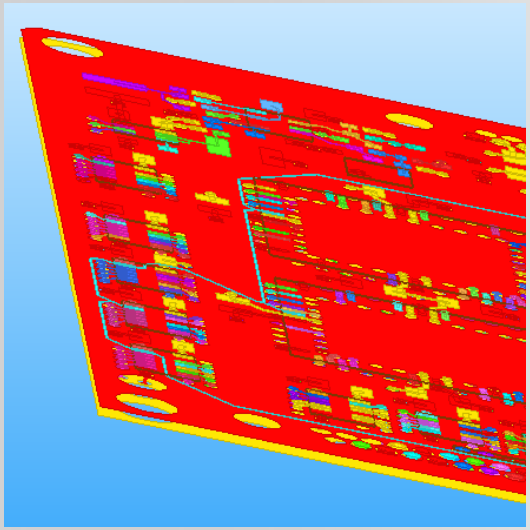
GUI Controls – Visualization



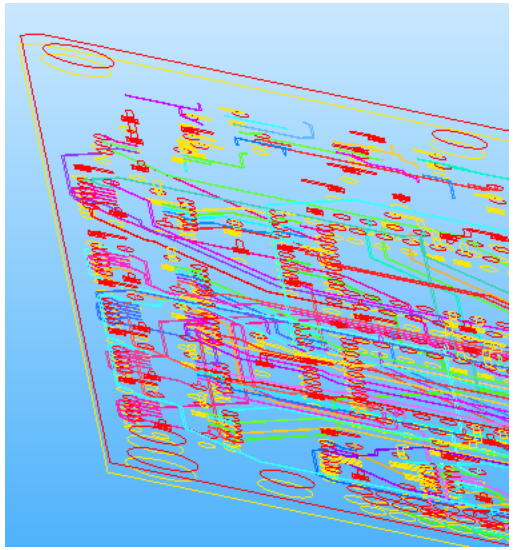
Performing Faster Transformations

- SIwave allows you to view a simplified model during rotate, zoom or pan operations.
- View>Faster Rotate.

Planes are represented in 2D, while vias and circuit elements are not displayed while you are rotating, zooming or panning in. The complete design is displayed only after you finish the operation.

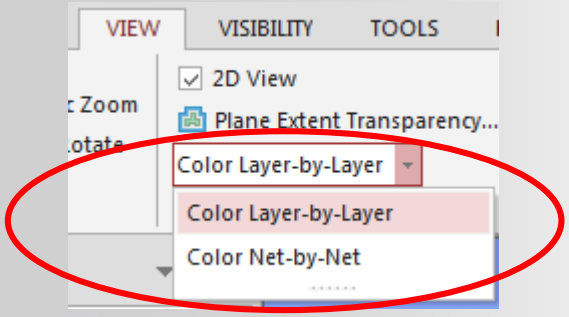


Before and After Rotation

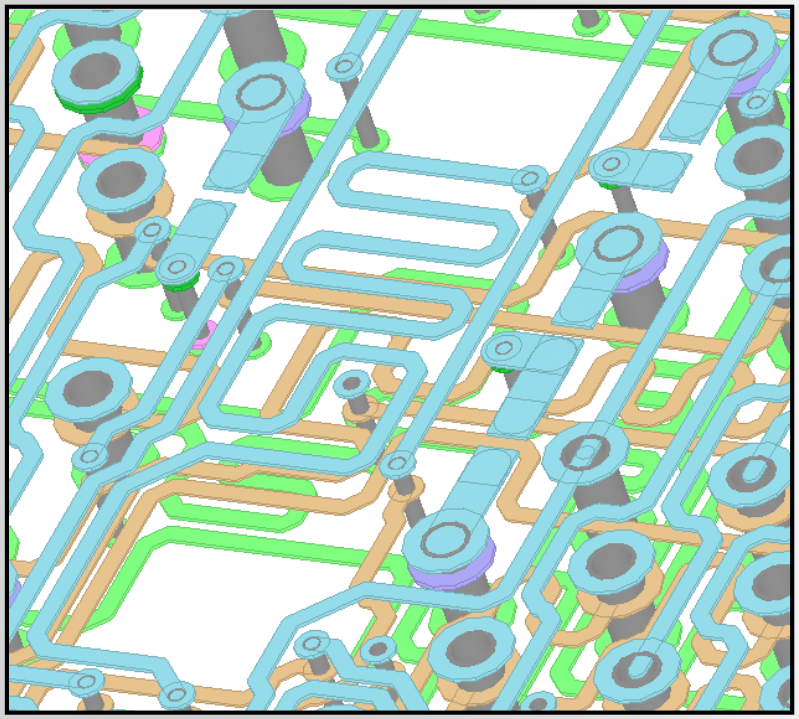


During Rotation

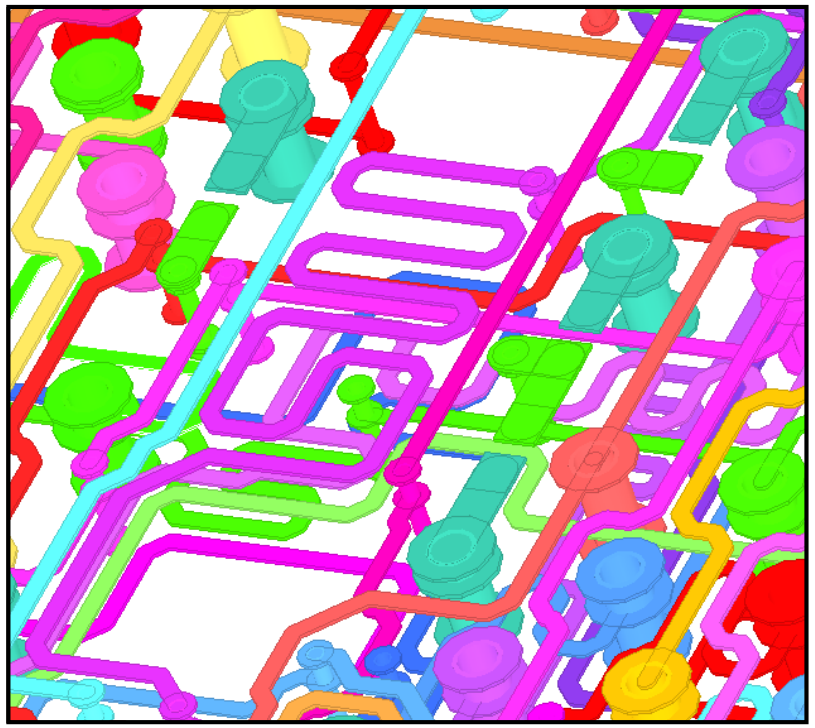
GUI Controls – Visualization



A user can toggle between the net and layer color modes



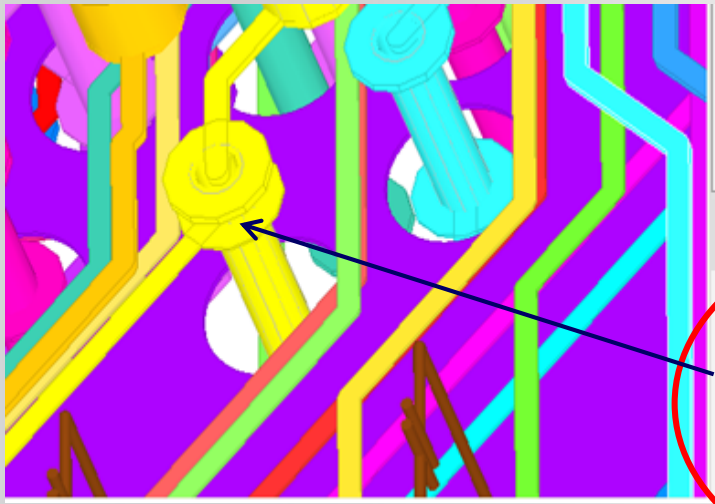
Layer Color Mode

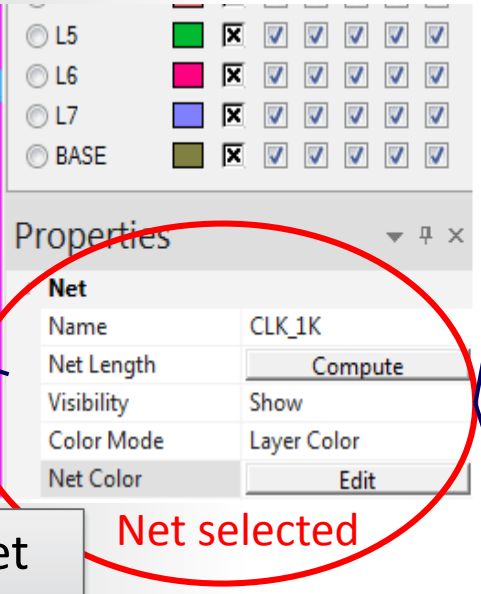


Net Color Mode

GUI Controls – Visualization

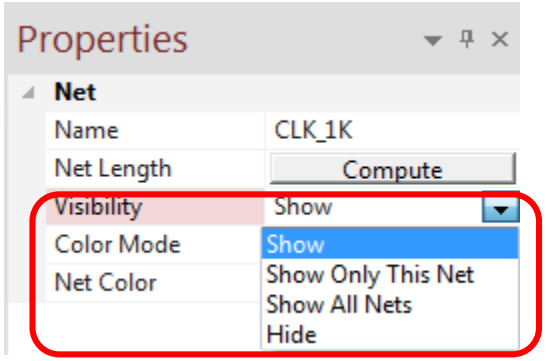
A dockable window displays the properties of the selected object



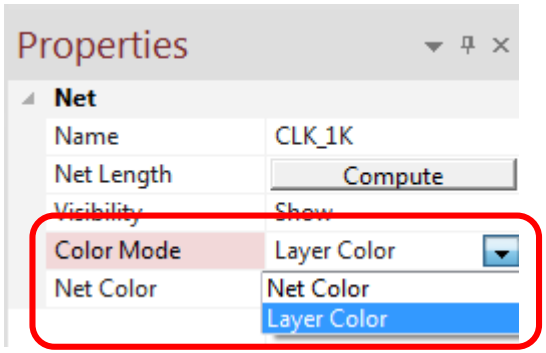


Net selected

For nets, users can change the net name, color, color mode and net visibility options



Only the selected net will be visible

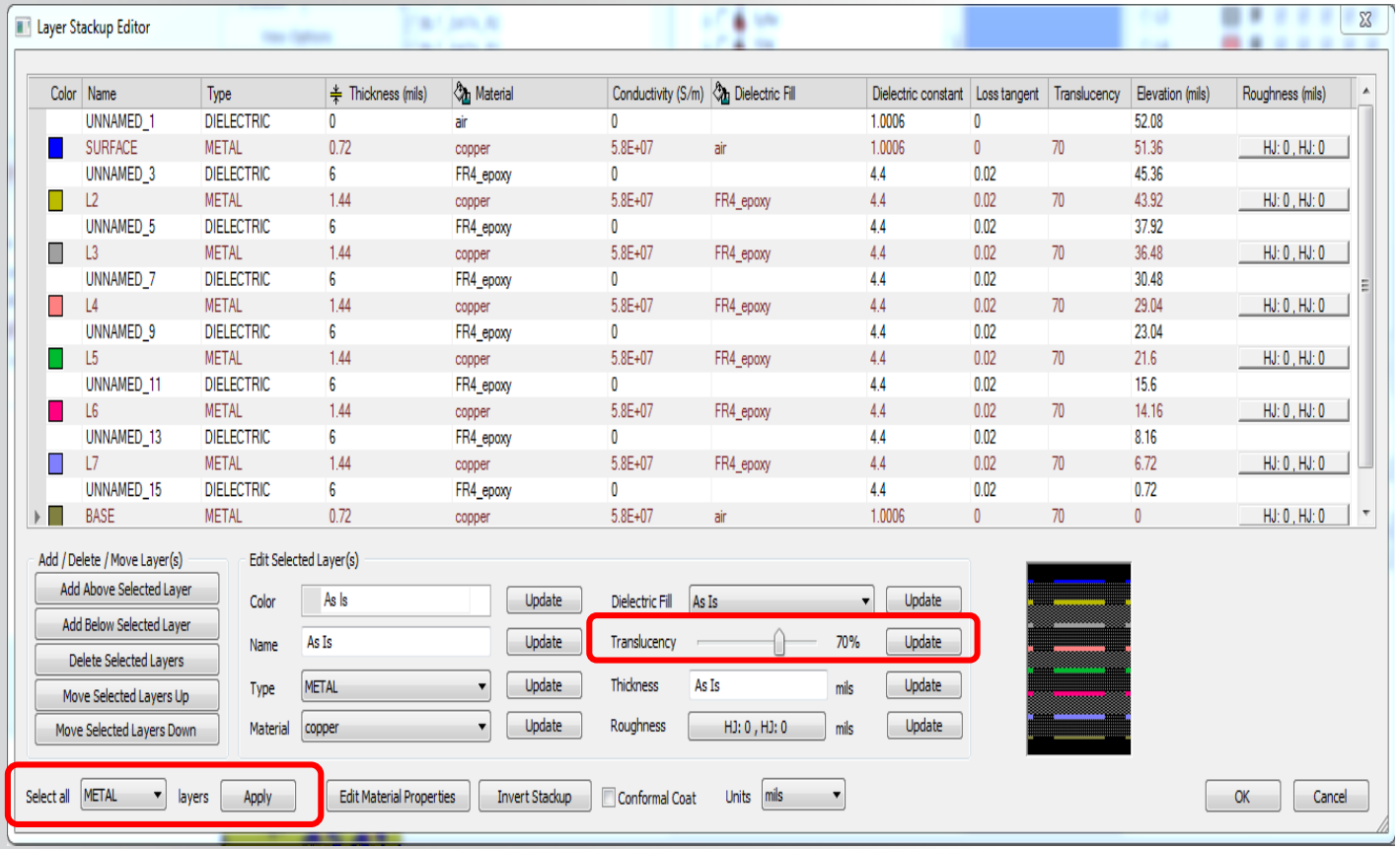


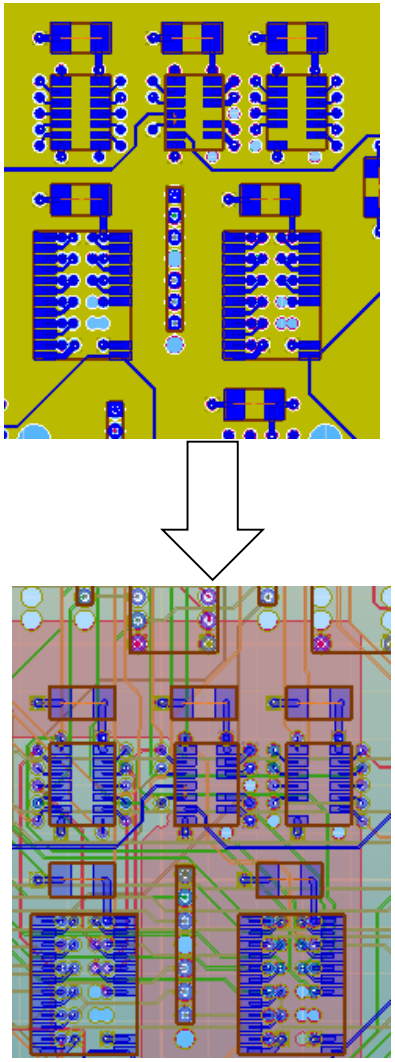
Toggling between two color modes

- **Object properties window**
- **Same options available using a right-click on the net list.**

GUI Controls – Visualization

- **Changing opaque view by setting Translucency for all metal**
  - Select all > METAL layers > Apply
  - Set Translucency to 70% > update
  - Better 3D visualization and rotation

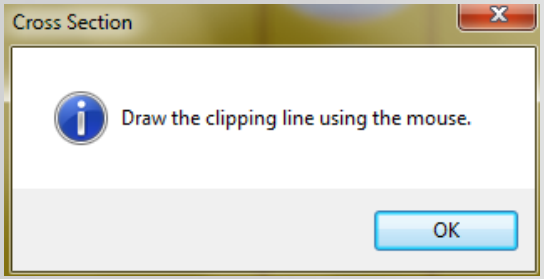


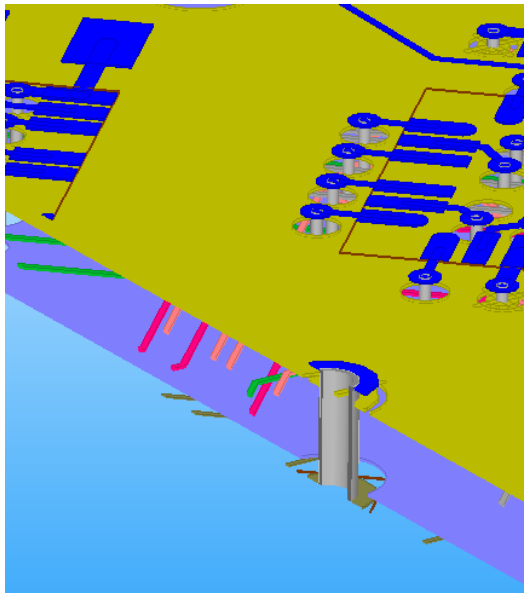


GUI Controls – Visualization

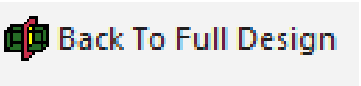
View > Compute Cross Section

- Draw a clipping line



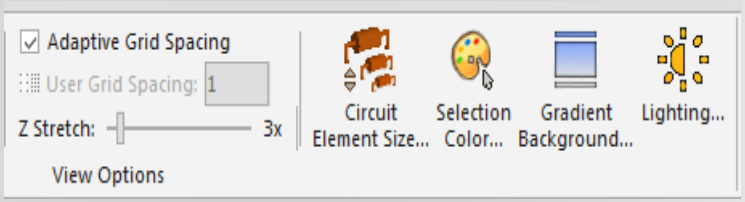


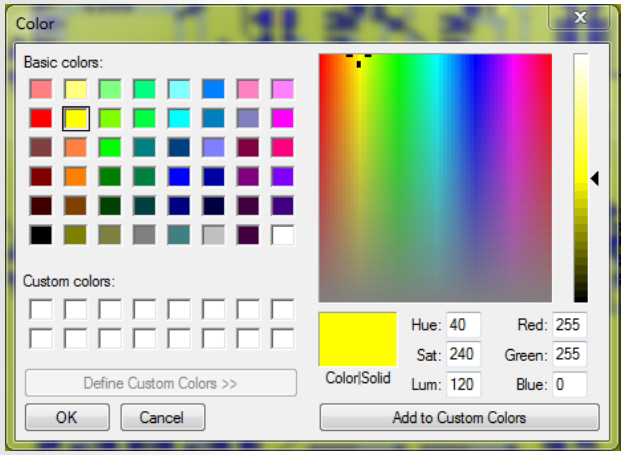
- View > Back To Full Design

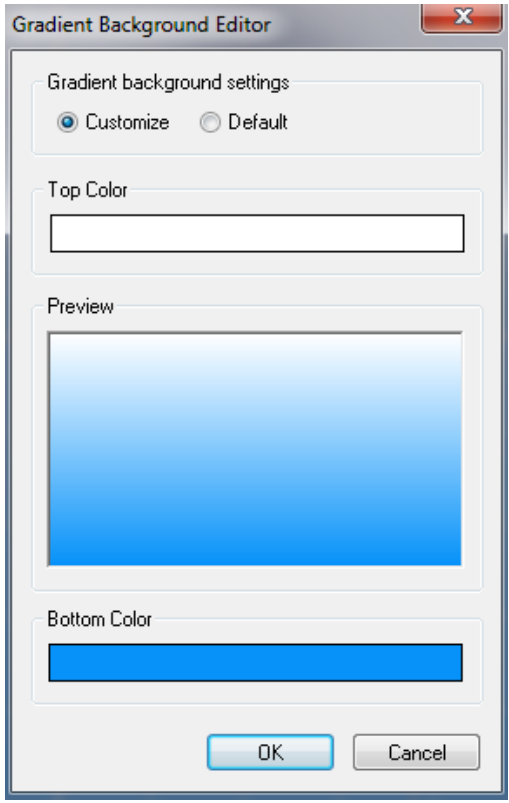


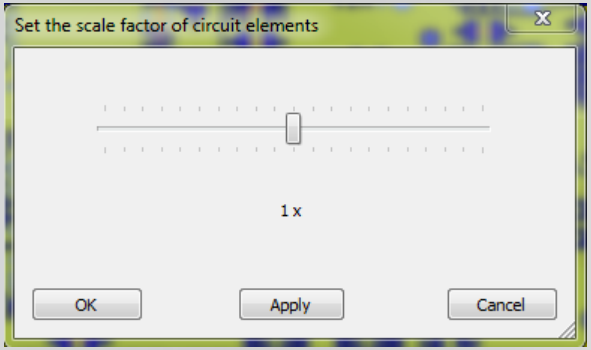
GUI Controls – Visualization

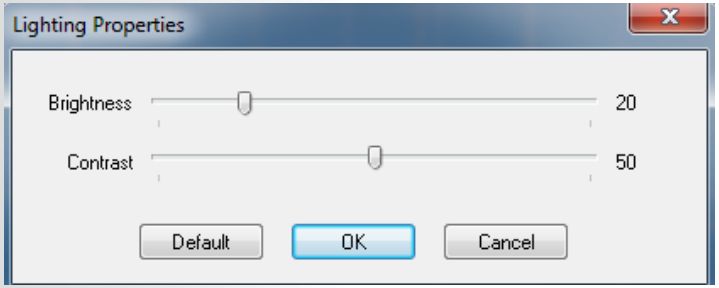
- **View > View Options**
  - Z Stretch– artificially scale Z values so that very thin planar objects have a 3D appearance. Choose any discrete value between 1 to 25
  - Change Selection Color - change default selection color (yellow)
  - Circuit Element Size - change the scale factor for circuit elements
  - Gradient Background - change default background colors
  - Lighting – change the Brightness and Contrast





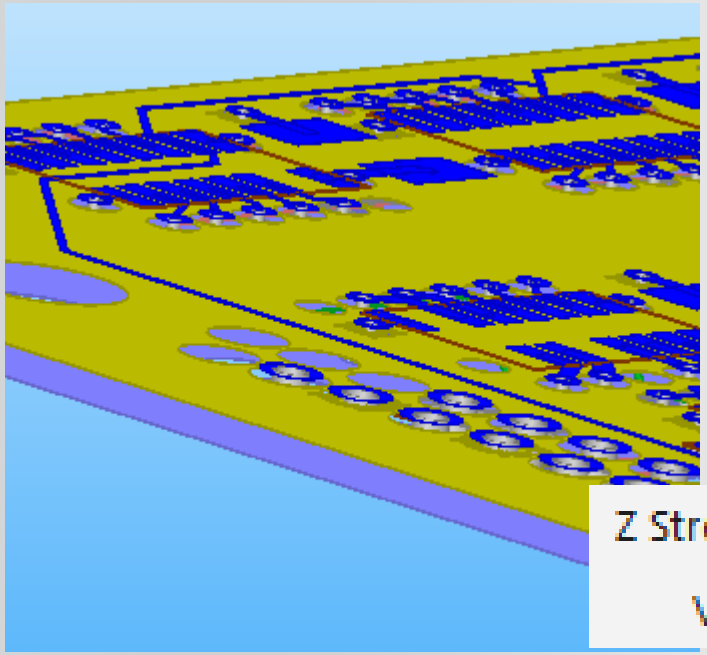


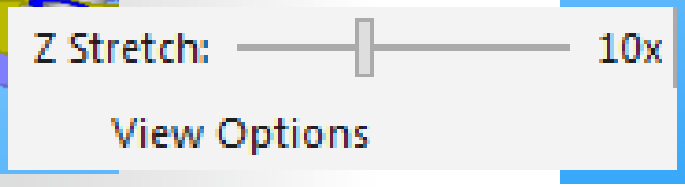


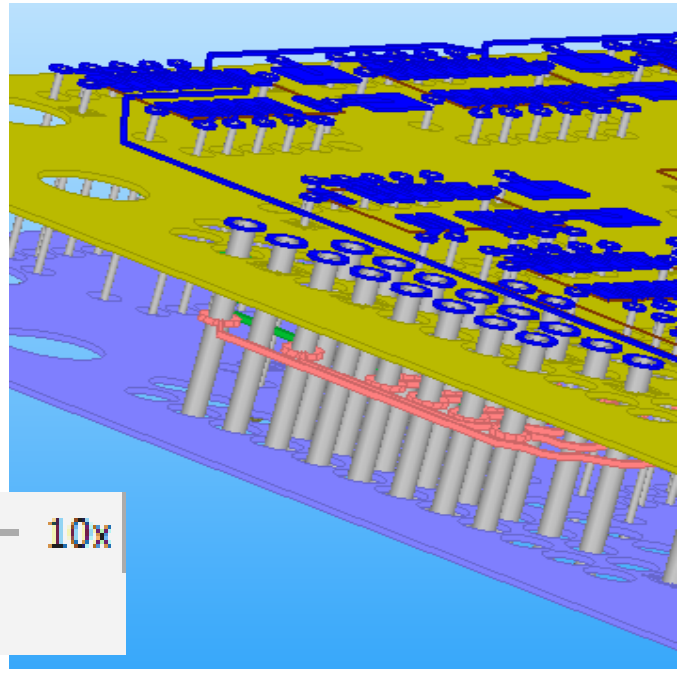


GUI Controls – Visualization

- **Stretching Z :**
  - To artificially scale Z values, so that very thin planar objects have a 3D appearance.
  - View>View Options>Z Stretch.
  - Choose any discrete value between 1 to 25, as the scaling factor.





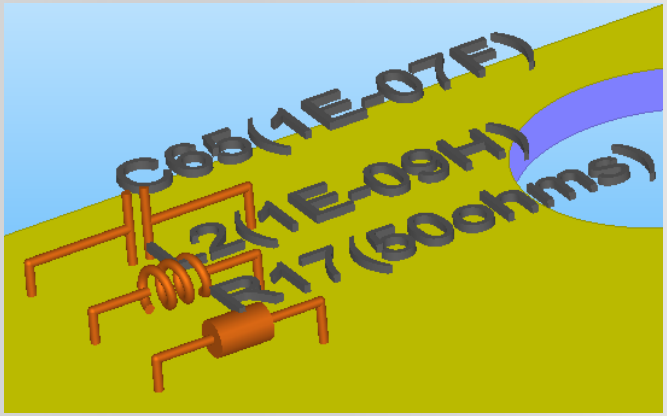


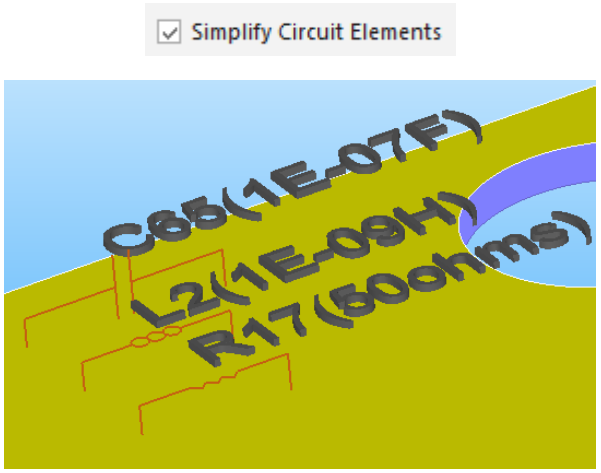
Original view : scaling factor = 1

Original view : scaling factor = 10

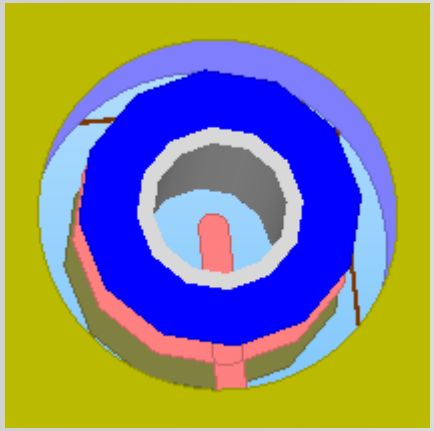
GUI Controls – Simplify Visualization

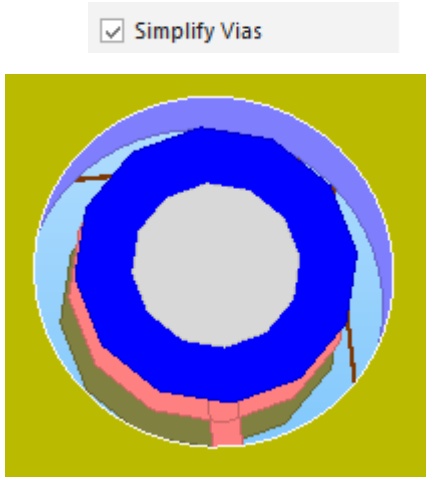
- View > Simplify Circuit Elements





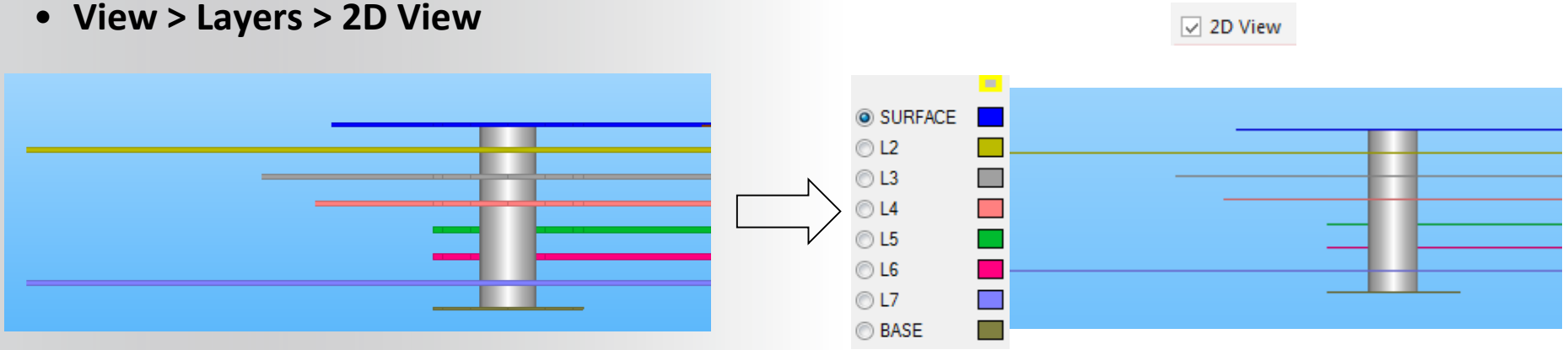
- View > Simplify Vias



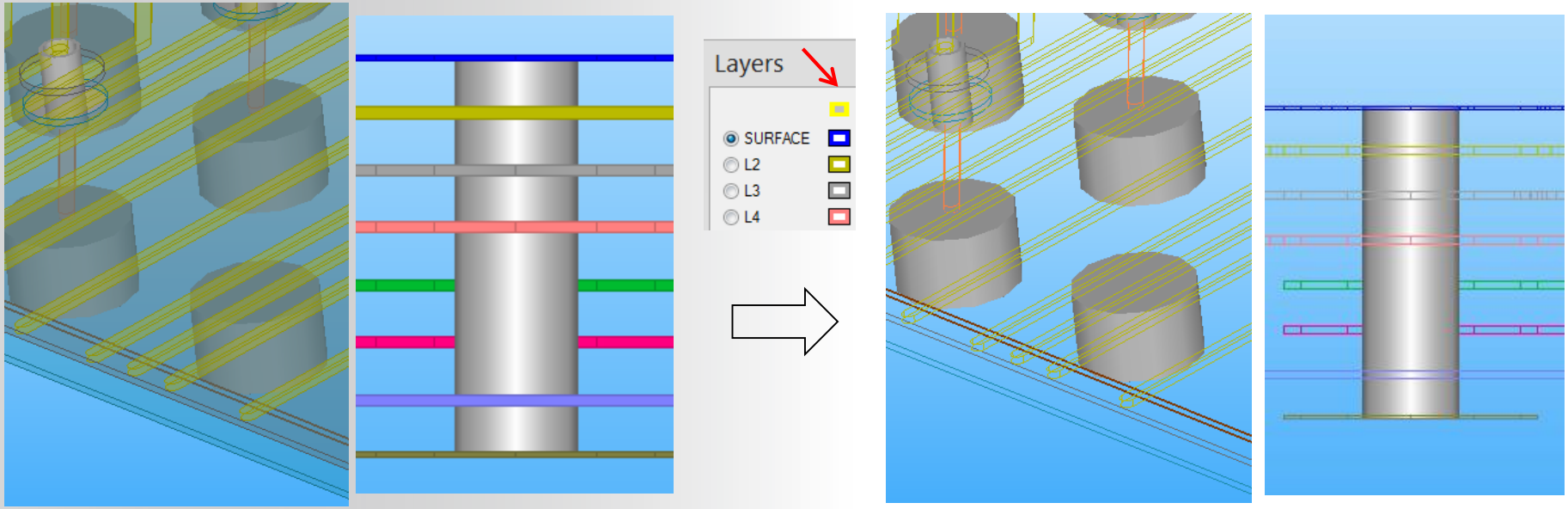


GUI Controls – Simplify Visualization

- View > Layers > 2D View

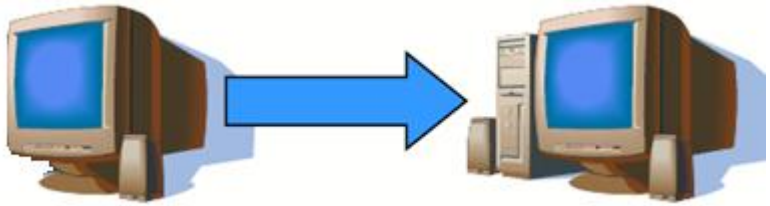


- Unfill All layers by clicking on the yellow rectangle in Layer workspace



Run in Remote

- To improve the response time when SIwave is running over a remote desktop:
  - OpenGL management is mandatory to support 3D
  - Informational tooltips will not appear.
  - Dynamic zoom is deactivated.
  - Faster transformation is activated.
  - Simplify all visualizations settings :
    - Vias
    - Circuit Elements
    - 2D view for layers
  - Use Translucency / Unfill layers



Batch mode

Syntax for SIwave:

<path to>/siwave -exec_eigen <path to>/<project name>.siw

The following flags are supported:

-exec_eigen

-exec_syz

-exec_ac

-exec_dc

Examples :

C:\installdir\siwave -exec_syz D:\Examples\Midplane.siw

C:\installdir\siwave -exec_eigen D:\Examples\switch.siw

C:\installdir\siwave -exec_dc D:\Examples\Blade.siw

ExecAcSim
ExecResModeSim
ExecPdnSim
ExecPsiPdnSim
ExecSyzSim
ExecSentinelPsiSyzSim
ExecSentinelPsiAcSim
ExecFfSim
ExecNfSim
ExecDcSim
ExecFwsSim
ExecPiOptSim

Non graphical Batch solve command

In R16, *siwave_ng* can be used as follows :

- This command, in addition to executing a requested simulation type, creates the necessary directory hierarchy and .asol file such that results can be post-processed in the UI after the siwave_ng run completes.

siwave_ng <path to .siw> <path to .exec> -formatOutput –useSubdir

Example :

C:\Program Files\AnsysEM\AnsysEM16.2\Win64\siwave_ng C:\projects\ssn.siw C:\test\execsyz.txt -useSubdir

ExecSyzSim
SetSwp 5e3 5e9 500 Linear

The .exec file, at the very least, should contain one of the following strings (which specify the type of analysis to execute):

ExecAcSim
ExecResModeSim
ExecPdnSim
ExecPsiPdnSim
ExecSyzSim
ExecSentinelPsiSyzSim
ExecSentinelPsiAcSim
ExecFfSim
ExecNfSim
ExecDcSim
ExecFwsSim
ExecPiOptSim

This file can also (optionally) contain commands to modify the sweep, change the number of CPUs, the licensing scheme, etc.:

SetSwp
SetNumCpus
AddSwp
SetInterpSwp
SetDiscreteSwp
InterpSwpCvg
NumInterpPts
EnableQ3dDomains
WaitForLicense
DistributeSIwaveSyz
HpcHostName
ComputeExactDcPt
SolverMemLimit
UseHpcLicenses

Non graphical Batch solve in detail

- **SetSwp <f_start> <f_end> <num_pts> <linear/log/linear step**

SetSwp 0 1e9 100 Linear

- **AddSwp <f_start> <f_end> <num_pts> <linear/log/linear step>**
  - use this like you are adding another sweep line in the UI; allows for changes to the number of points & the distribution type
  - use in conjunction with SetSwp

SetSwp 0 1000 10 Log
AddSwp 1000 5e9 500 Linear

- **SetNumCpus <number>**

SetNumCpus 4

- **SetDiscreteSwp**
  - no argument; just tells the simulation to use a discrete sweep for the sweep setup in the UI
  - can also use in conjunction with SetSwp

SetSwp 0 1e9 100 Linear
SetDiscreteSwp

- **SetInterpSwp**
  - no argument; just tells the simulation to use an interpolating sweep for the sweep setup in the UI
  - can also use in conjunction with SetSwp

SetSwp 0 1e9 100 Linear
SetInterpSwp

- **InterpSwpCvg <Relative error for S>**

InterpSwpCvg 0.005

- **NumInterpPts <num_points>**
  - number of points to be explicitly solved for during the interpolating sweep

NumInterpPts 30

- **UseHpcLicenses <pack | pool>**
  - *SolverMemLimit <% of memory to be used by the solver on a machine when using a HPC License>*

UseHpcLicenses pack
SolverMemoryLimit 80

- **ComputeExactDcPt <boolean>**

ComputeExactDcPt 1

- **EnableQ3dDomains <boolean>**

EnableQ3dDomains 1

- **WaitForLicense <boolean>**

WaitForLicense 1

- **DistributeSIwaveSyz**

no argument required

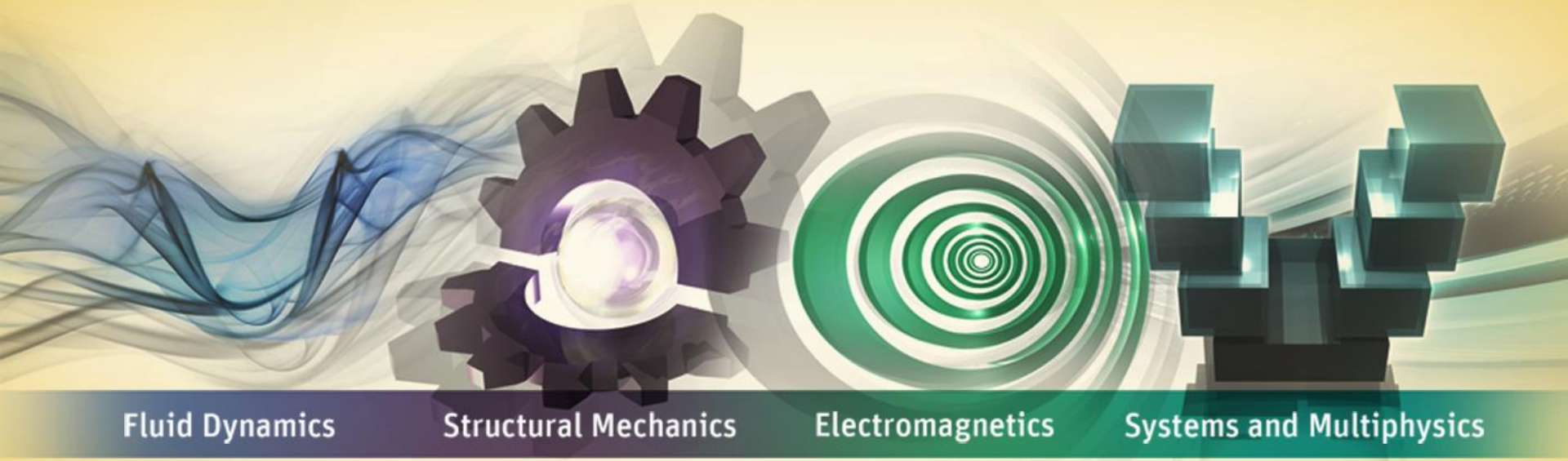
- **HpcHostName <machine_name|IP address> <CPUs_to_use> <%Memory>**
  - use in conjunction with DistributeSIwaveSyz
  - can use this command to enter multiple machines

DistributeSIwaveSyz
HpcHostName \\machineA 6 80
HpcHostName \\machineB 6 80
HpcHostName \\machineC 6 80

ANSYS

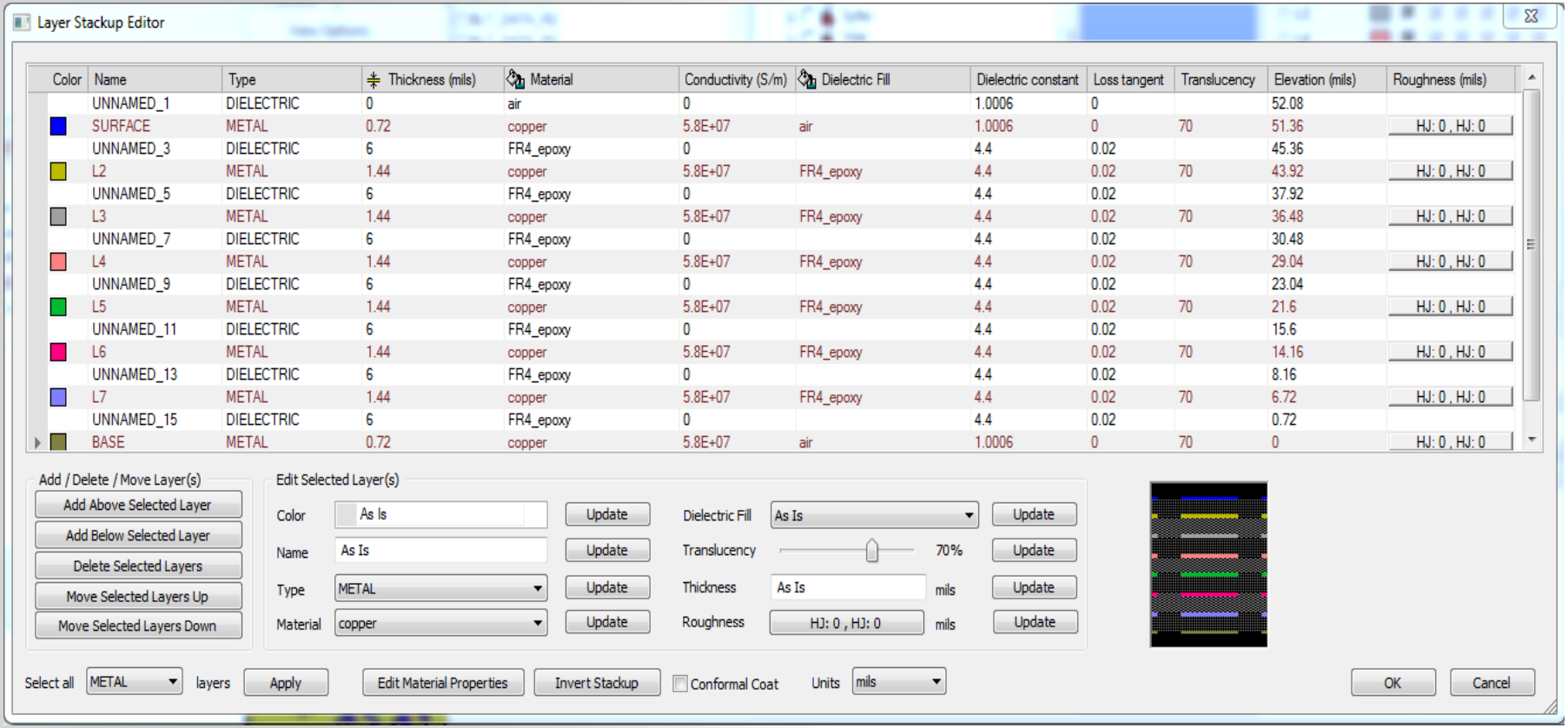
Realize Your Product Promise™

Stack up, Padstack, Balls/Bumps, Bondwire



Layer Stack-up Editor

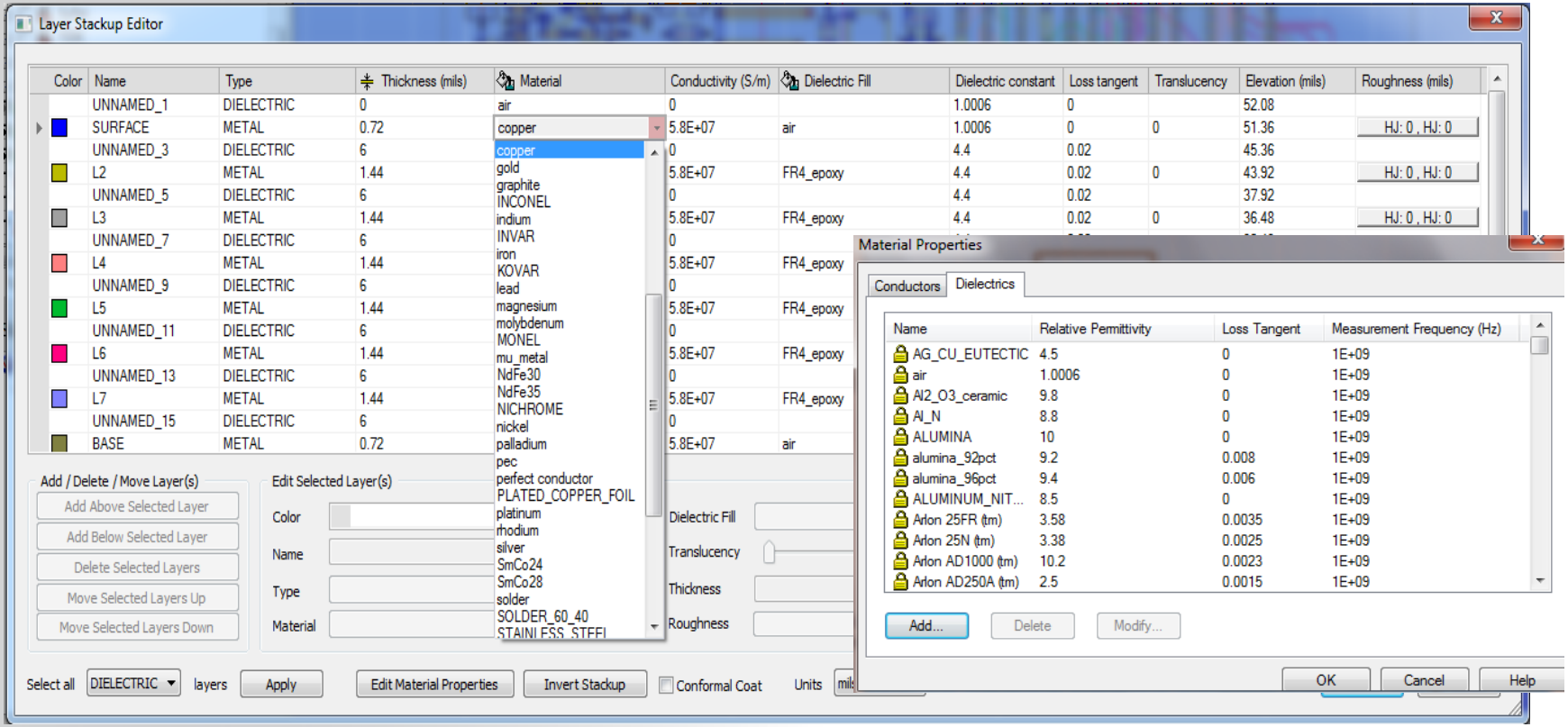
- All layers are imported with material properties and thickness



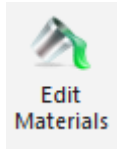
- Possible to edit and export/import the Layer stackup (“.stk” file)
  - File > export > Export Layer Stackup

Material

- **Easily change the material properties using the predefined Material library of SIwave or Add a new one.**

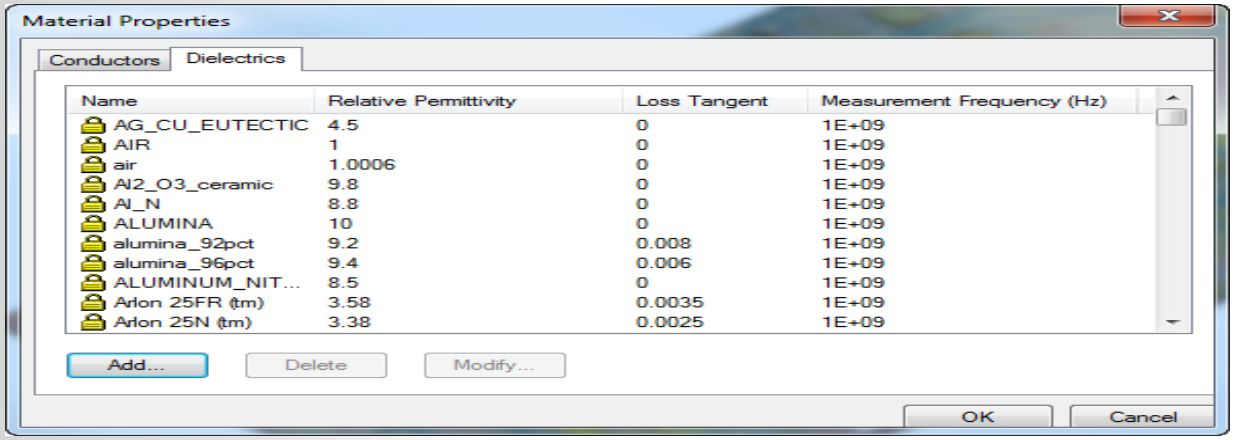


- **Add a new Material**
  - **You can click on Edit Material Properties > Add… or go to Home > Edit Materials**

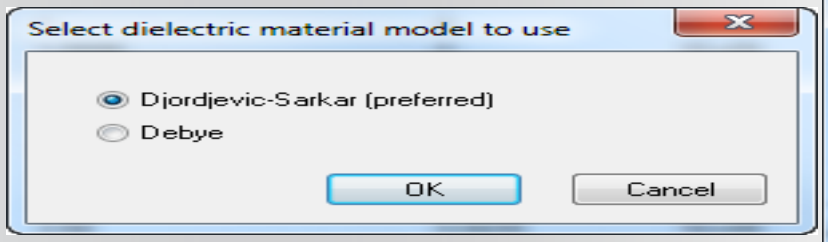


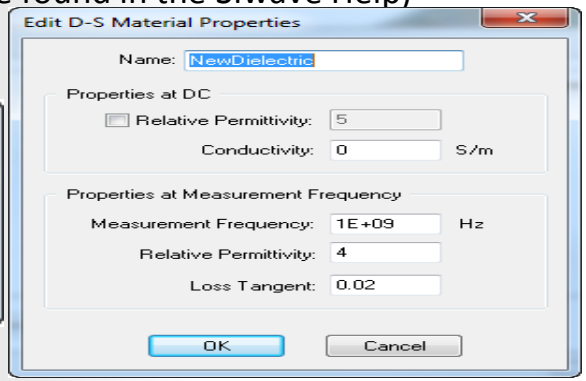
Materials – View / Edit /Create

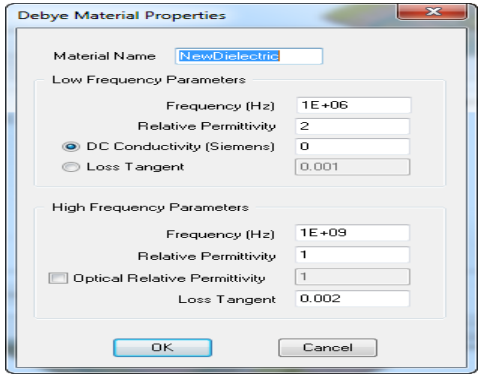
- **Materials**
  - View existing material properties or create a new material
  - Make sure that the correct material, Conductor or Dielectric, is selected then click the Add button to create a new material



- **Dielectrics**
  - Choose which dielectric material model to use
  - The preferred Djordjevic-Sarkar model is a causal frequency-dependent dielectric model developed specifically to model FR-4. It is also useful for many other low-loss insulator materials. The Debye model characterizes a lossy dielectric material by two measured values at a certain frequency. (More detailed information on both of these models can be found in the SIwave Help)

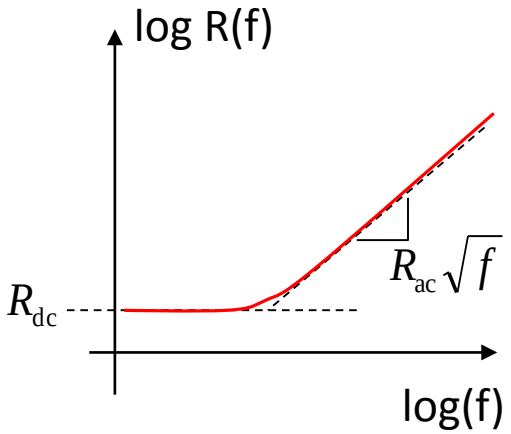




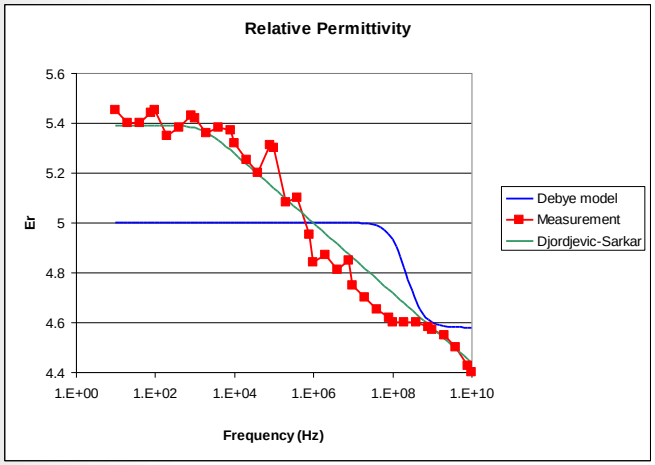


Material - Frequency dependent parameter

- **Have to consider :**
- **Conductor loss**
  - Skin Effect
- **Dielectric constant and loss**
  - Djordjević-Sarkar model



$$\varepsilon(\omega) = \varepsilon'(\omega) + j\varepsilon''(\omega)$$
$$= \varepsilon_\infty + \frac{\Delta\varepsilon}{\ln(\omega_B/\omega_A)} \ln\left(\frac{\omega_B + j\omega}{\omega_A + j\omega}\right) + \frac{\sigma}{j\omega\varepsilon_0}$$



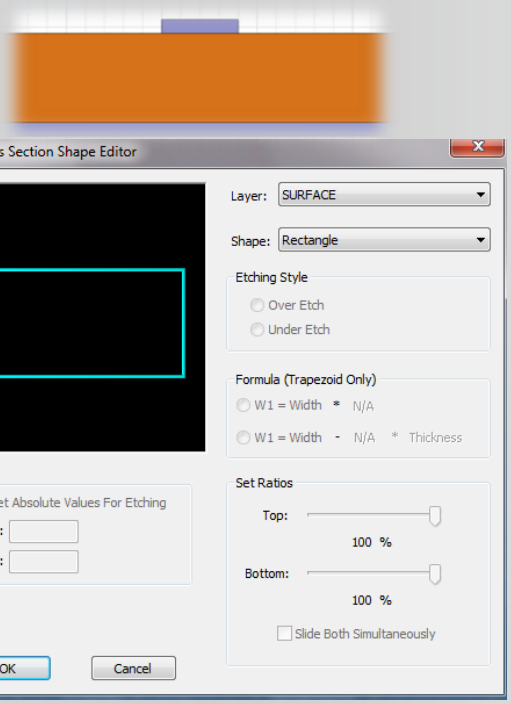
Frequency dependent models are default

Modeling of Traces

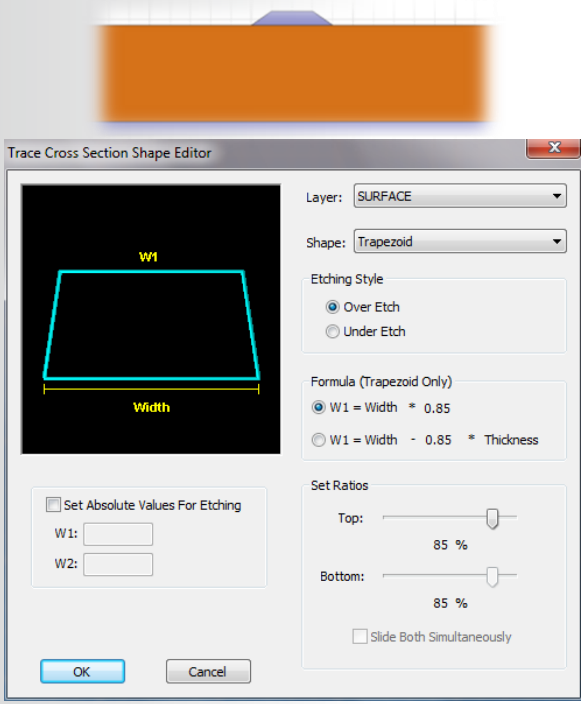
- **Define Trace Cross Section by choosing the appropriate shape by layer:**
  - Rectangular, Trapezoidal and hexagonal

- **Edit > Trace Cross Section…**

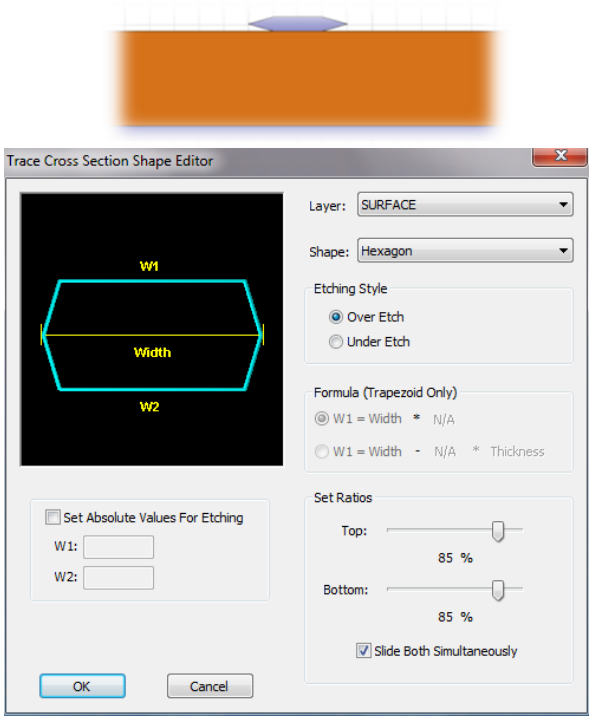
Rectangle



Trapezoid

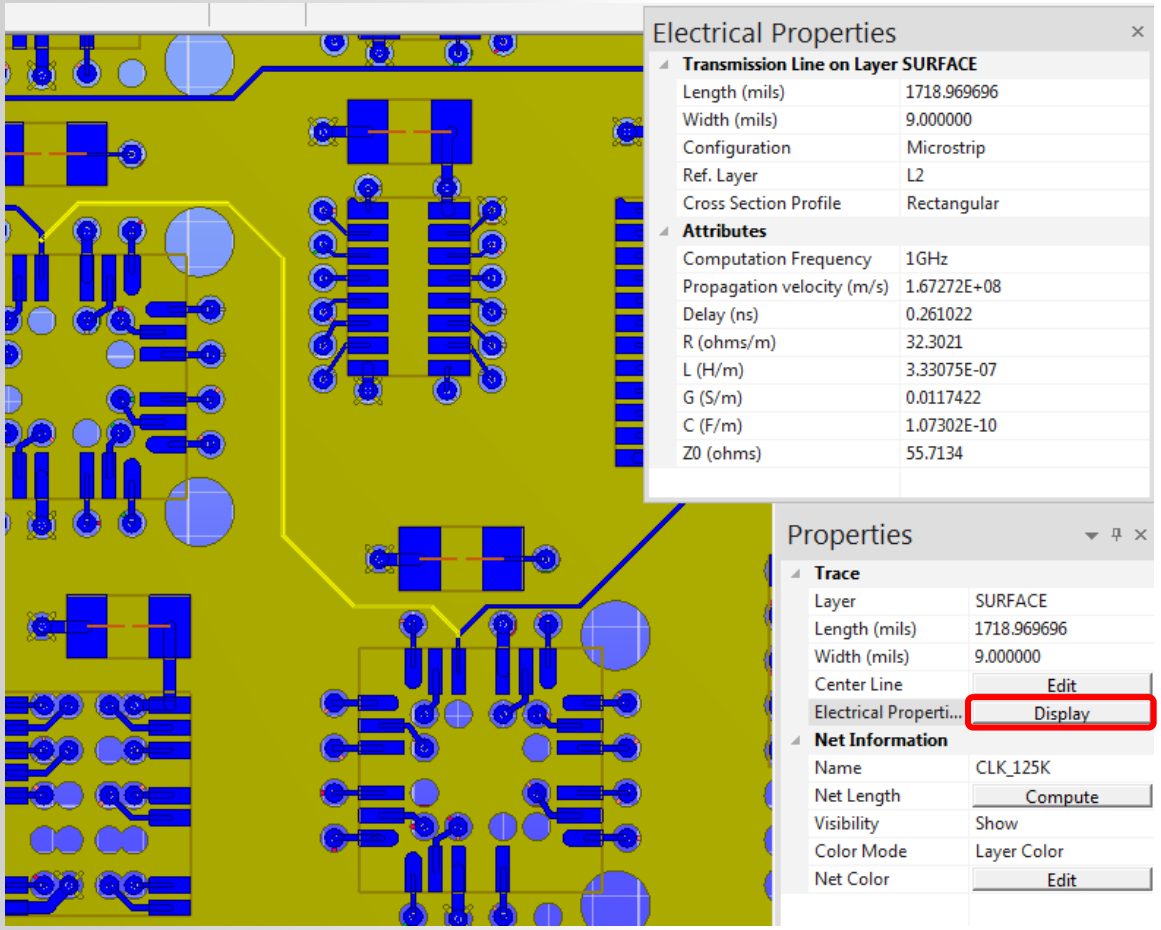


Hexagon

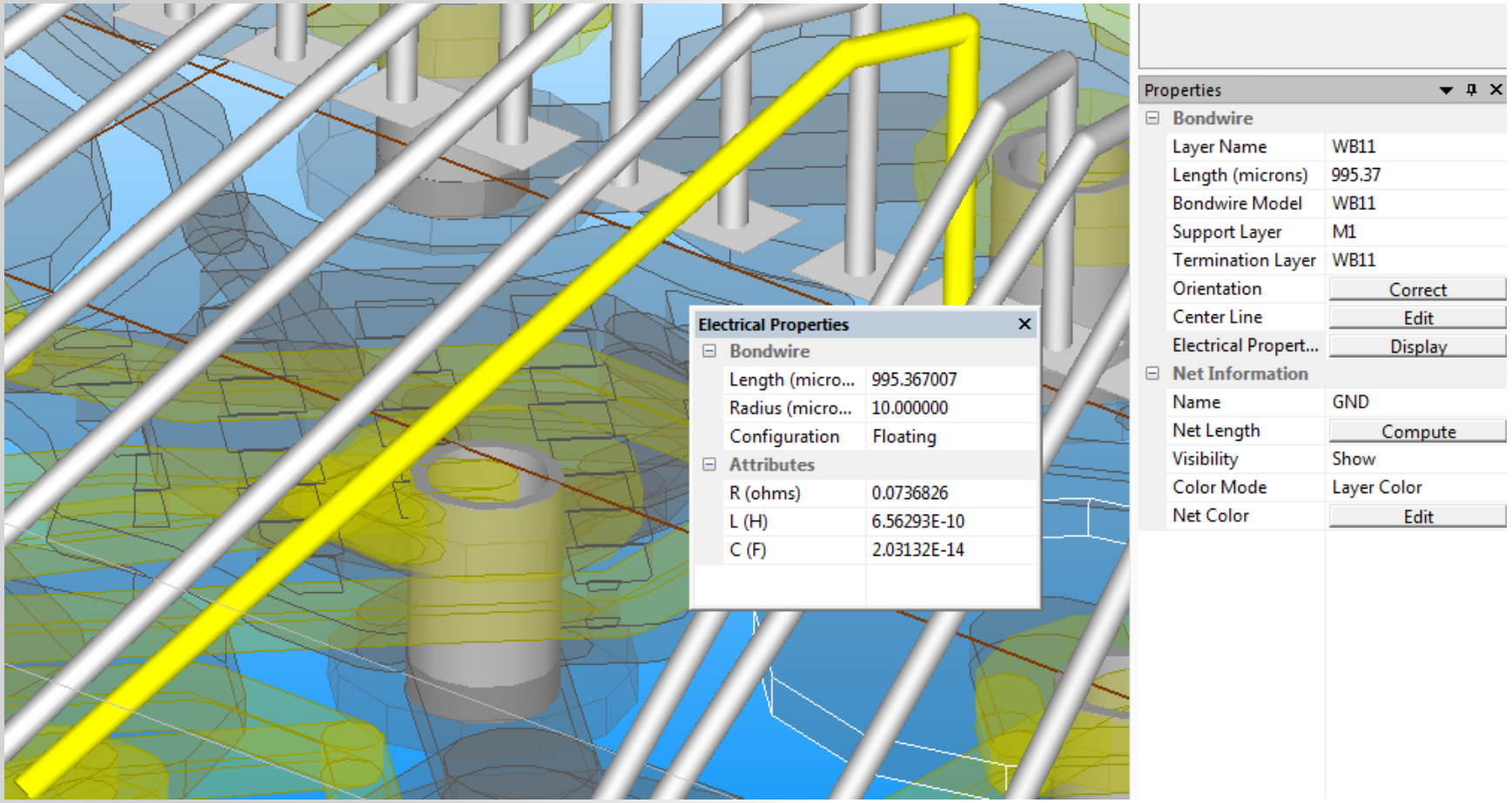


Trace Electrical Properties

- Display the electrical properties of the selected transmission line in real time.
- Selecting mode should be on “object”
- In the properties window, click on Display

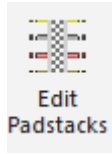


Bondwire Electrical Properties

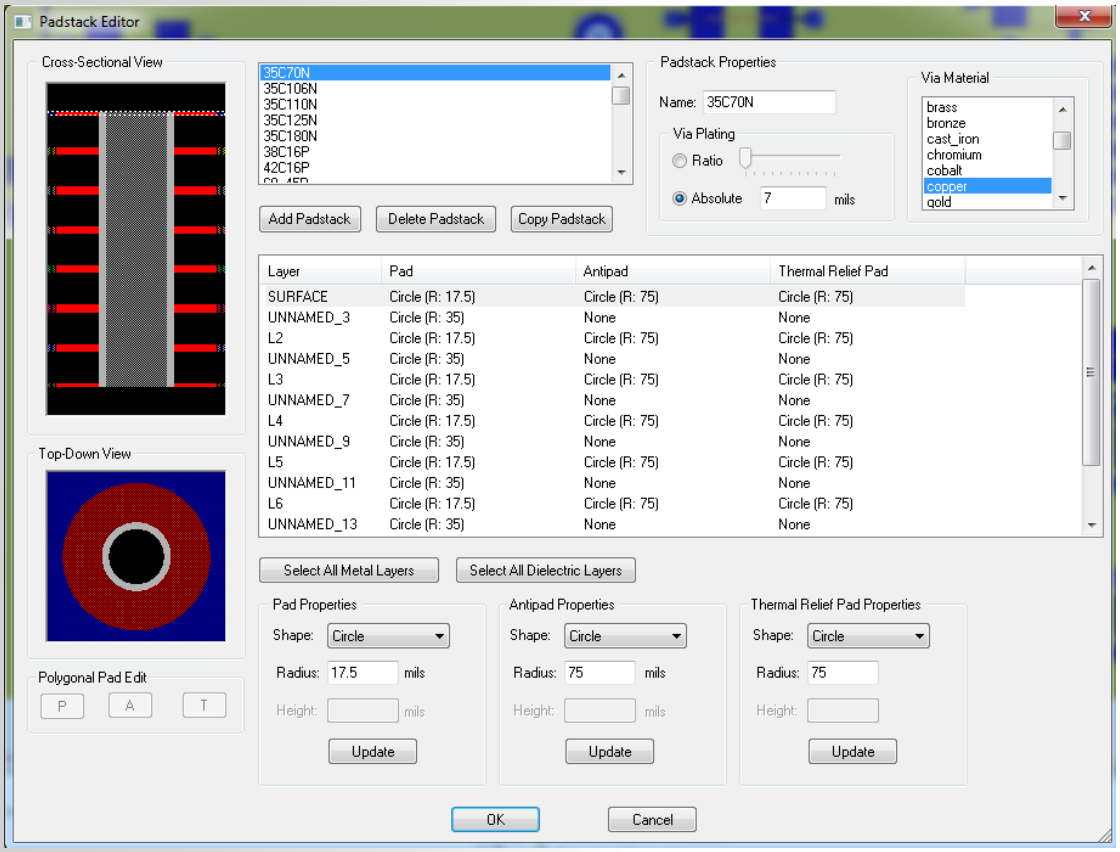


Padstack Editor

• Padstacks describe the stacking structure of shapes associated with pads and vias. They enable different shapes on different layers and contain drill information, plane layer information, and inner layer information. In the editor, padstacks can be added, modified or deleted



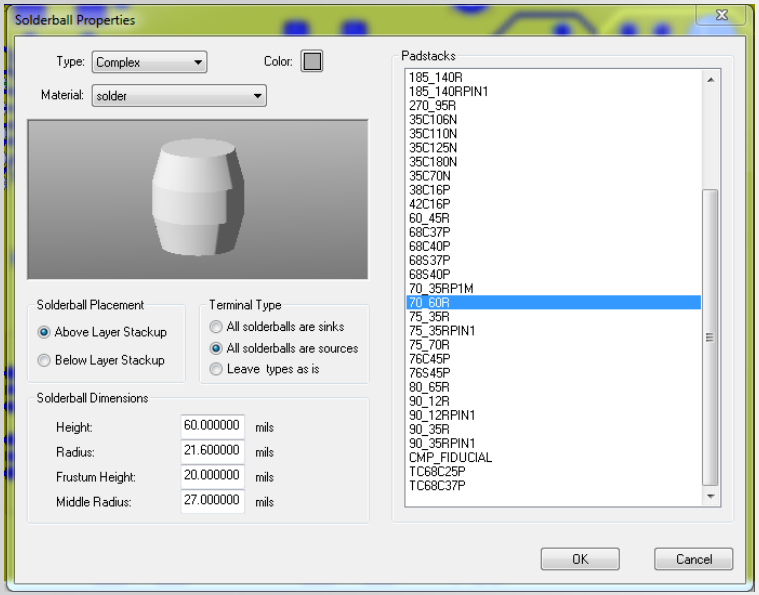
- **Home > Edit Padstacks**
- **Select a padstack to view its properties.** If a via is selected in layout it will automatically be highlighted when the Padstack Editor is launched

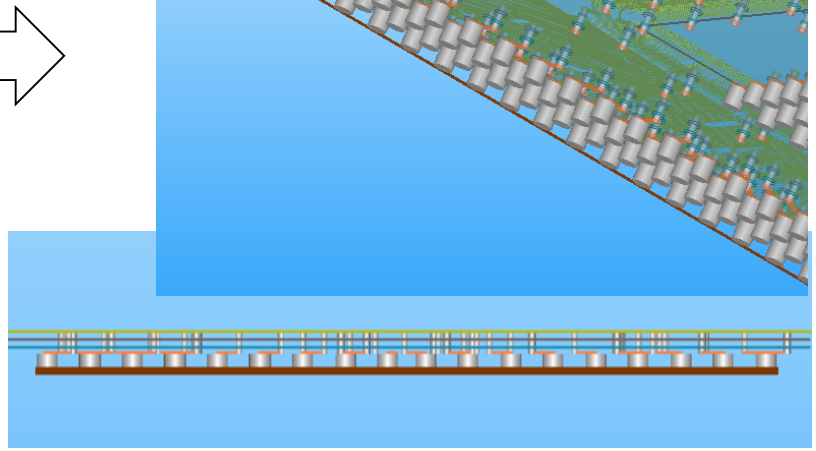


SolderBall Generation

- **Home > Solderball Properties**

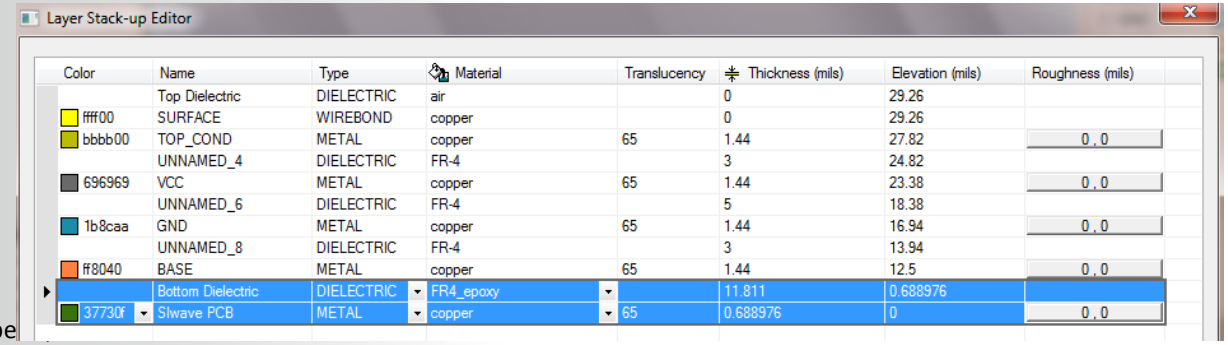
- **Choose padstack and Enter Type, Radius and Height**





Creation of the solderballs and add a PCB layer

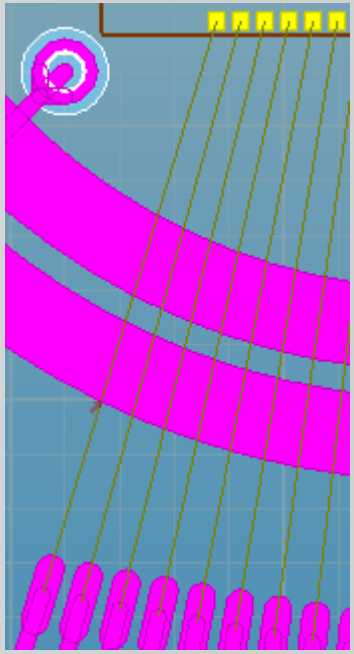
- **Update the stackup (replace FR4 by Air)**

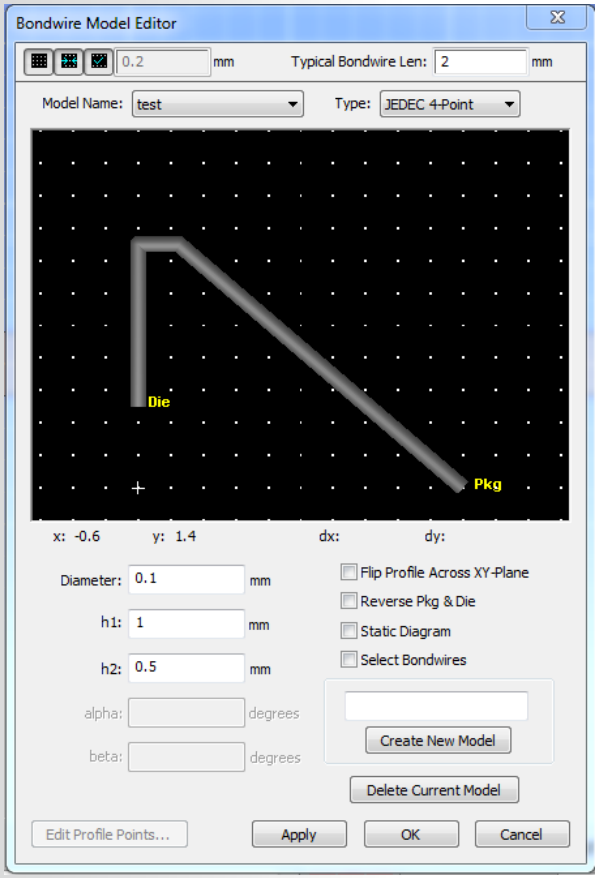


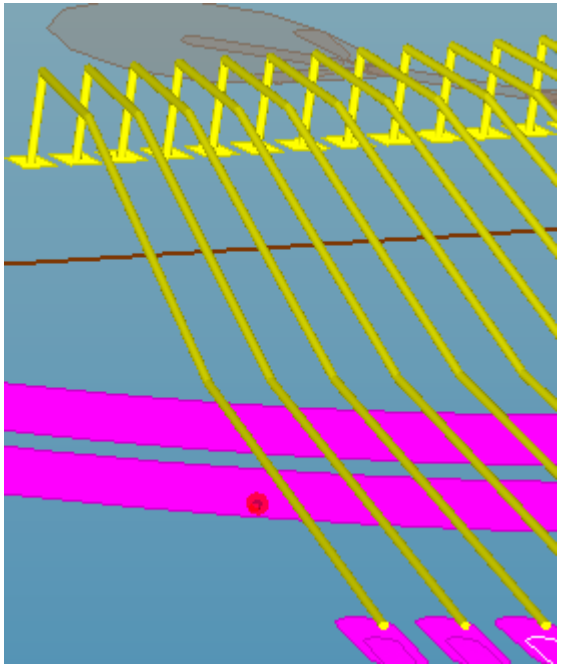
Bondwire Generation

- Bondwire models can be assigned to the layers in the stackup. This command is active only when at least one layer has the type **WIREBOND**. You can edit the layer properties to change the layer type.
- Because bondwires are modeled as traces, you first need to draw a trace before creating a bondwire**.**

- **Edit > Bondwire Model**

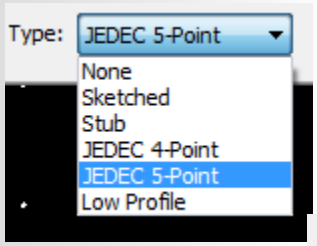






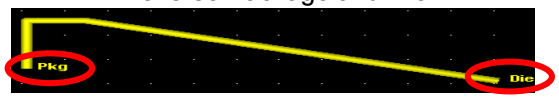
Bondwire Model

- **Bondwire type**
  - Several models are available :

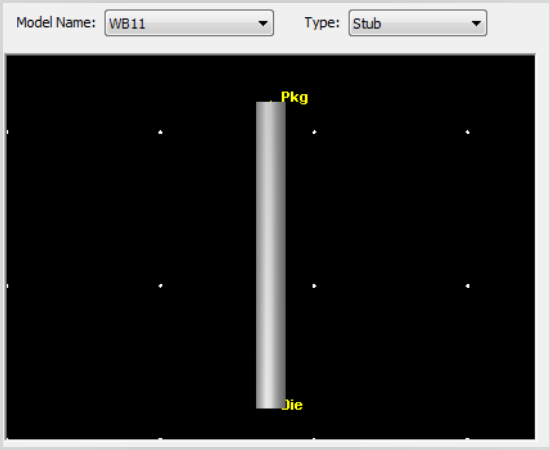


Flip Profile Across XY-Plane

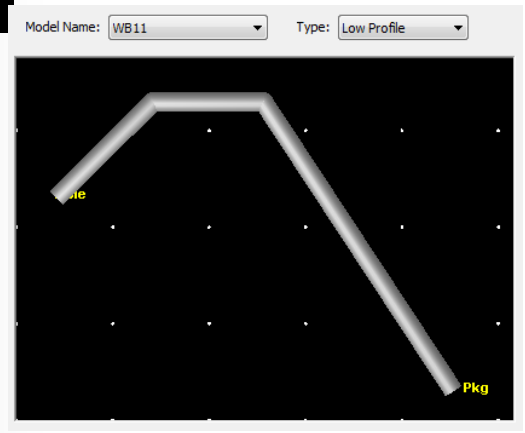
Reverse Package and Die

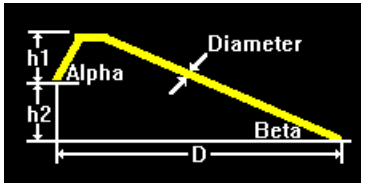


Stub

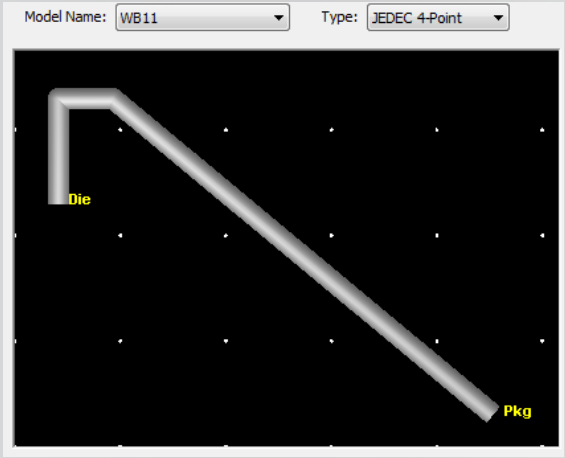


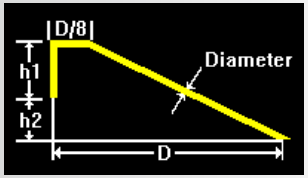
Low Profile



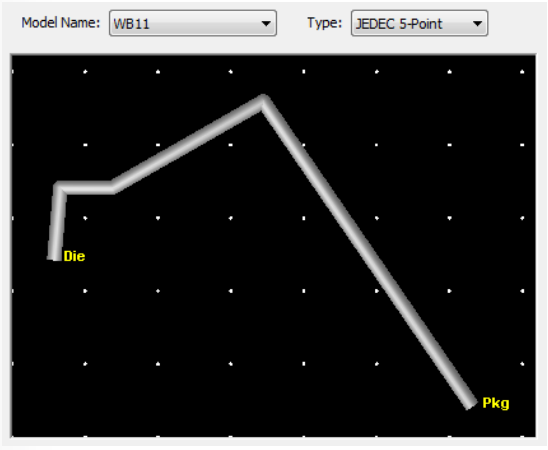


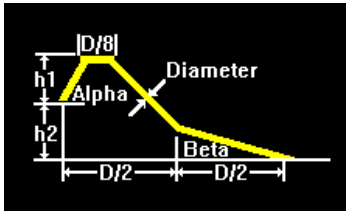
JEDEC 4-Point





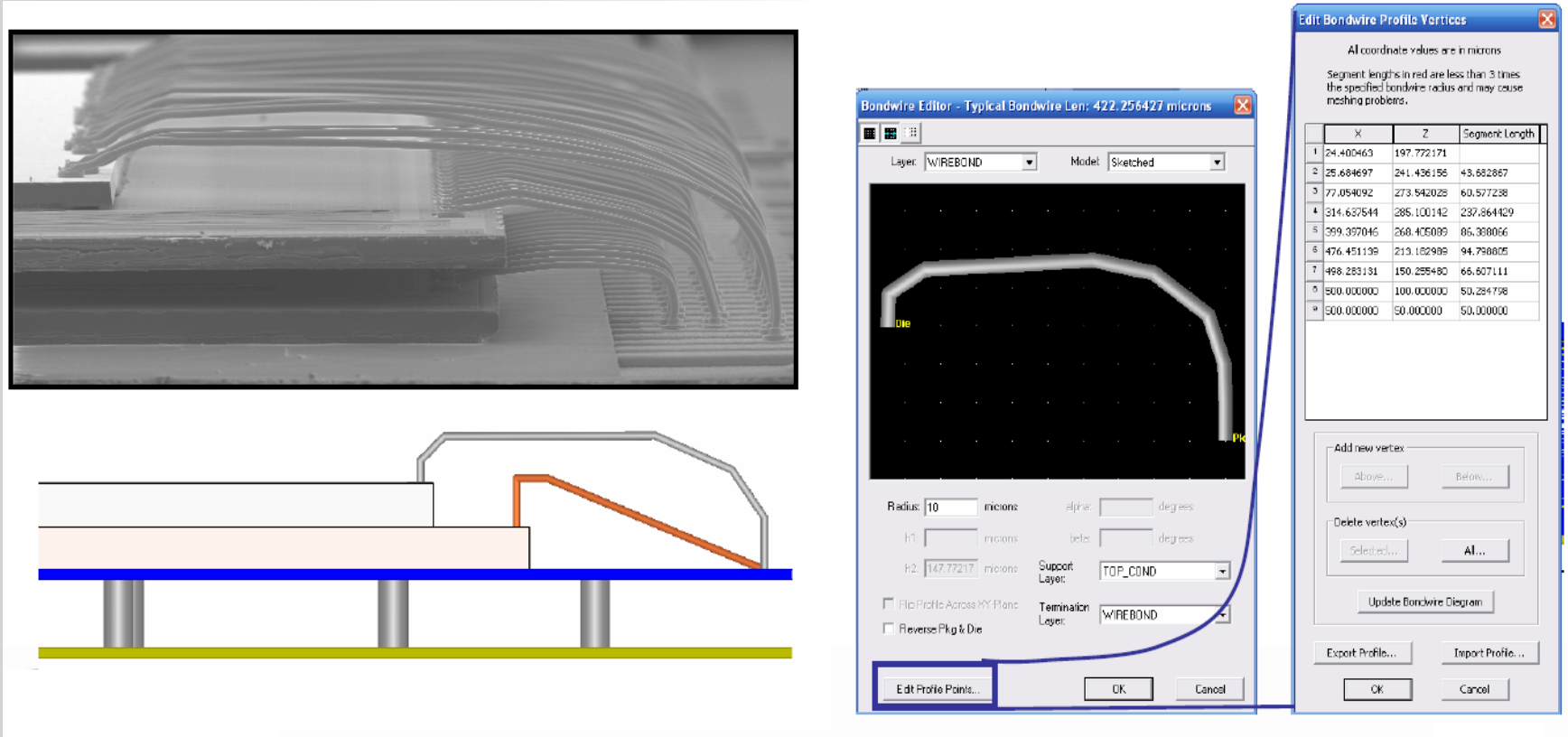
JEDEC 5-Point





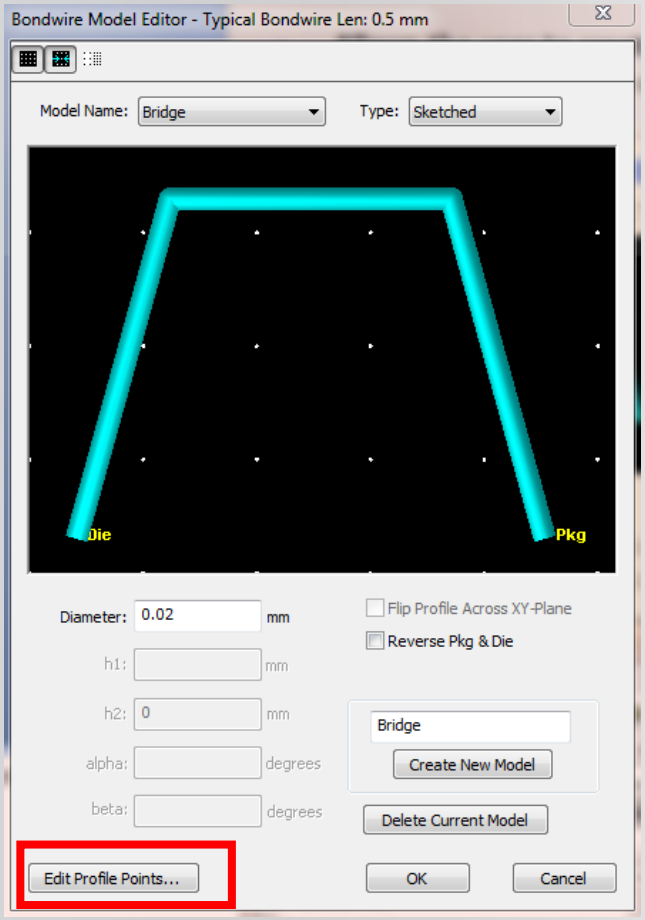
User Defined Bondwire for SiP

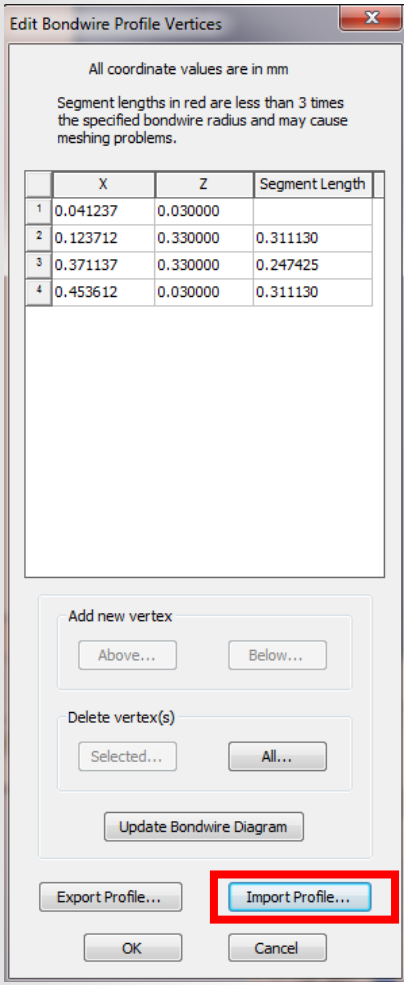
- For Bondwire profile, it is common to use JEDEC 4 or 5 points, but this can cause collision problem for stacked dies in SiP.
- With User Defined Bondwires is it possible to draw every kind of profile from sketch (user can also edit, save or import his own profile)



Custom Bondwire Profile

- **Edit > Bondwire Model…**
- Create a custom bondwire profile by entering points or importing coordinates from a file. The .bwp (bondwire profile) can be imported for use in other projects. Click the **Update Bondwire Diagram** button to refresh the sketch

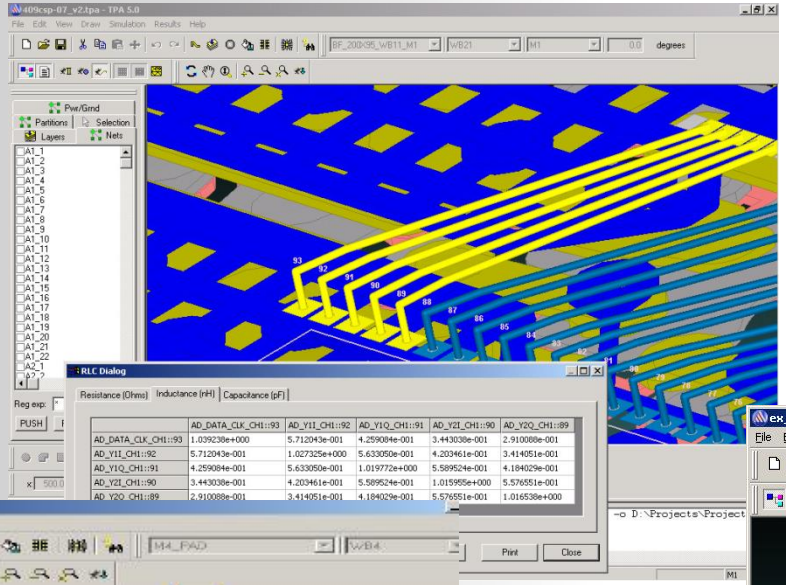




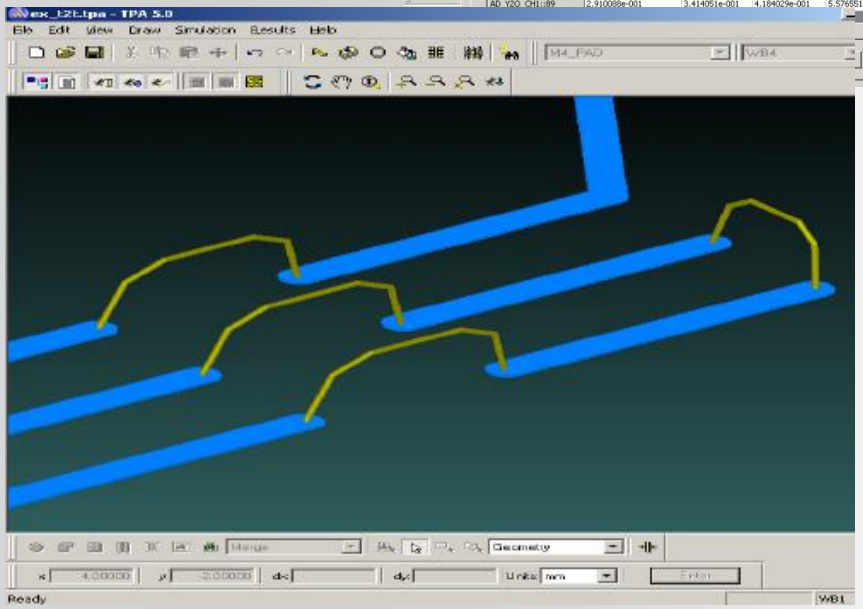

```
# File created by Ansoft TPA
#  Sketched bondwire profile point data
#  Project: GSG_model.tpa
#  Bondwire layer: Bridge

UNITS mm
0.041237 0.030000
0.123712 0.330000
0.371137 0.330000
0.453612 0.030000
```


Expanded Bondwire Options

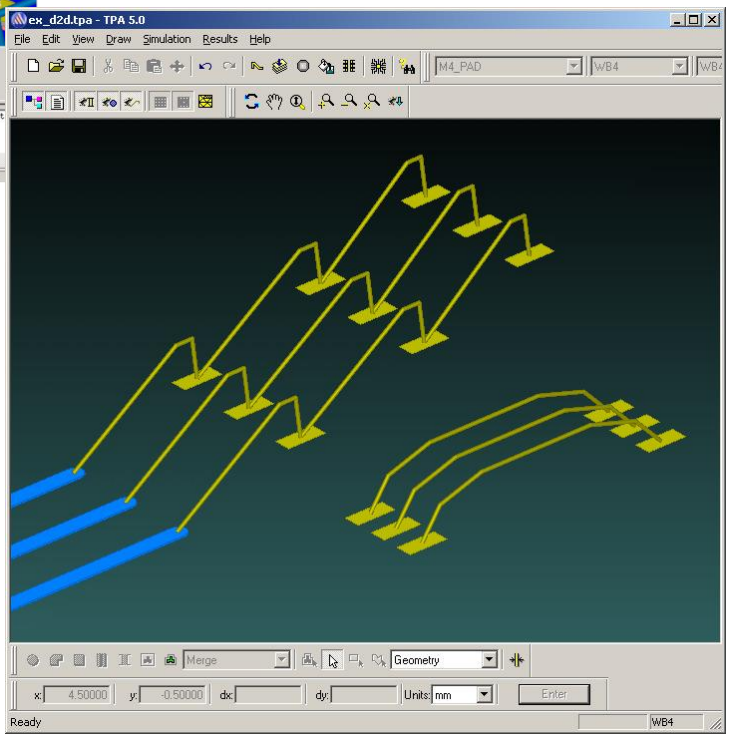
- Die-to-die



- Trace-to-trace

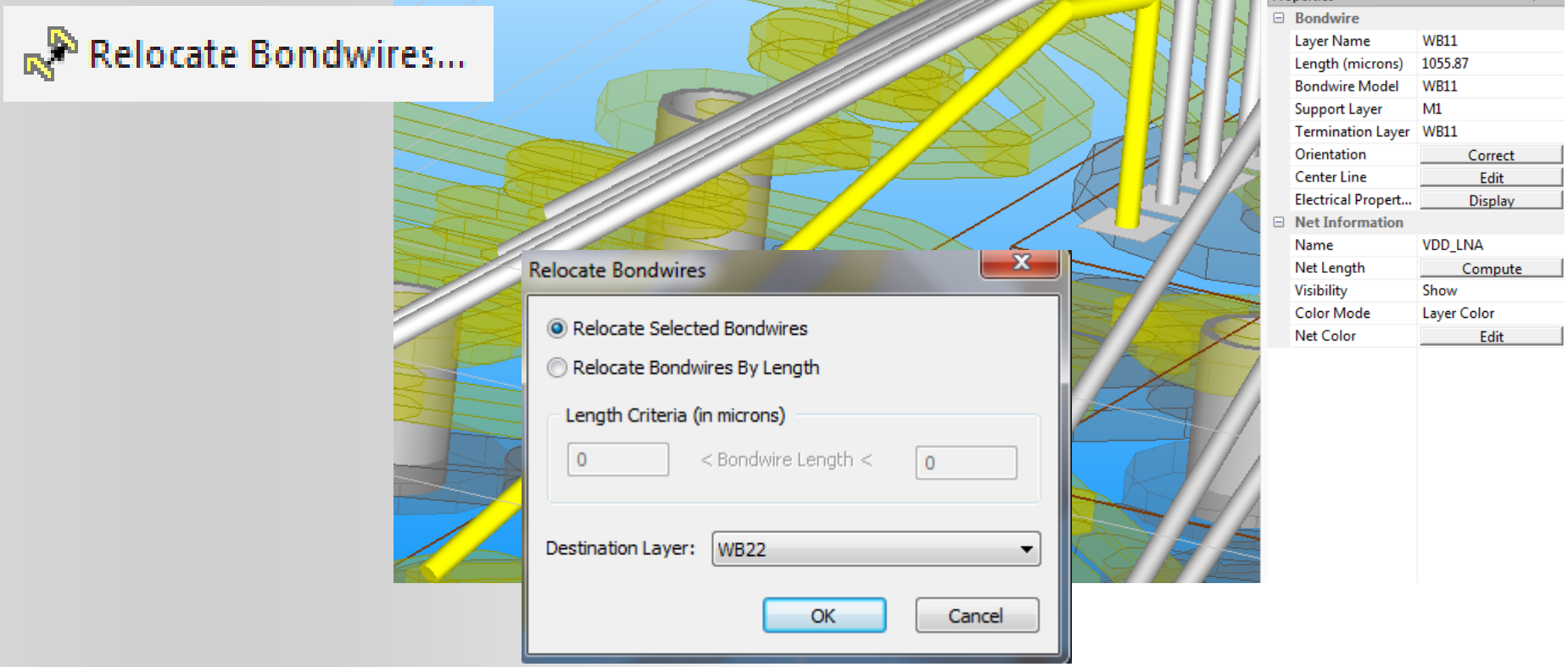


- Cascaded



Relocate Bondwires

- Tools > Relocate Bondwires…
- One isolated Bondwire « VDD_LNA » on Layer ‘WB11’
- Relocate it on ‘WB22’ layer using « Relocate Bondwires » utility



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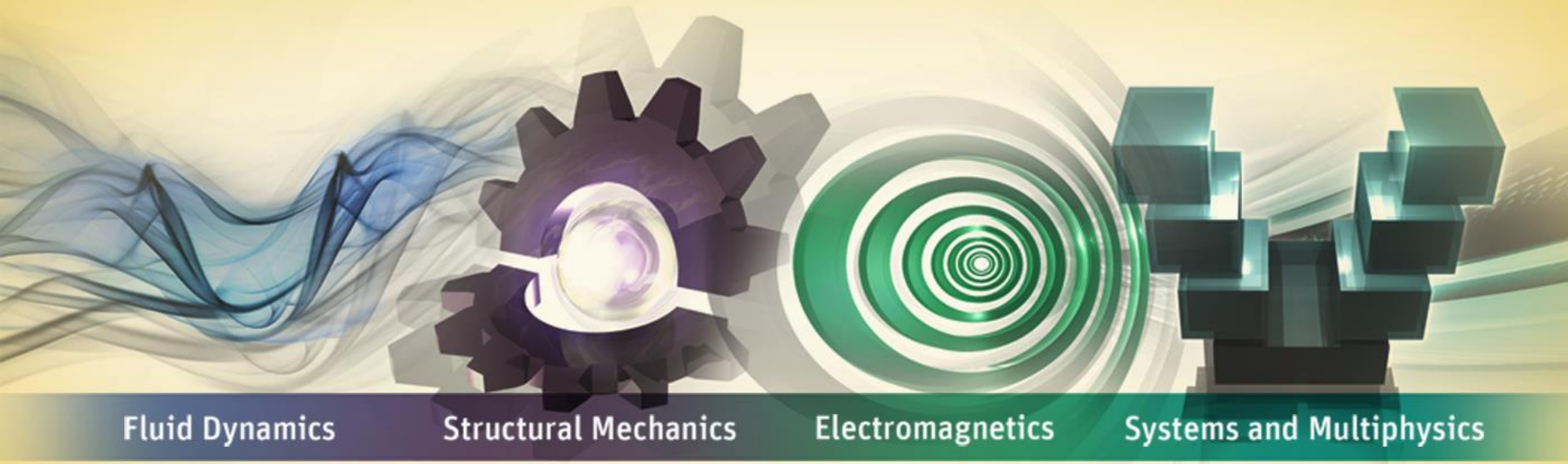
Drawing Mode

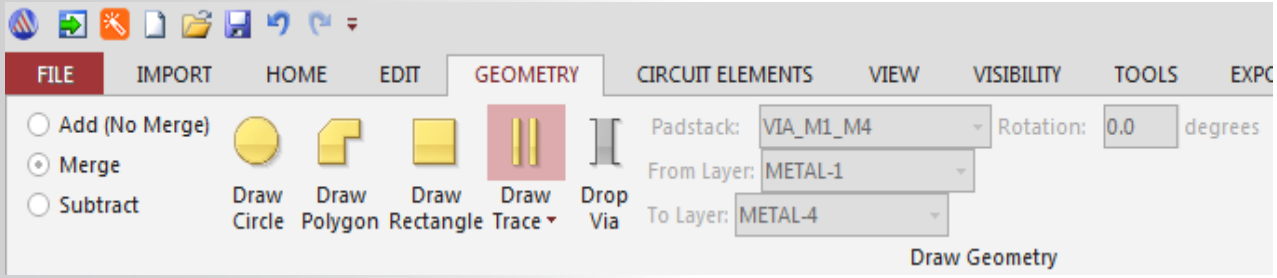


Drawing Mode (1/2)

To modify the layout, you can specify various options for drawing two or more geometric shapes. The shapes can be either added without merging, or merged, or subtracted.

Select one of the three mode

- Draw > Drawing Mode
  - Add (No Merge) : To draw and display multiple objects together. No union between each shape primitive and different “net name”.
  - Merge : To draw and display multiple objects as one merged object. Same “net name”.
  - Subtract : An existing geometry can be modified by drilling holes in it or by removing some elements from it. The area of the geometrical shape is cut out from the main Drawing Area.

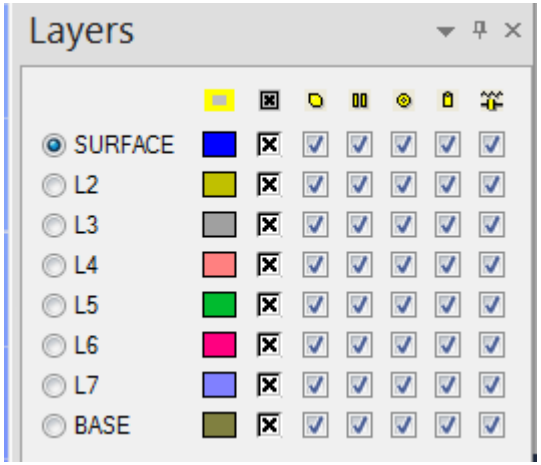


Drawing Mode (2/2)

Select the drawing layer in the Layers Workspace

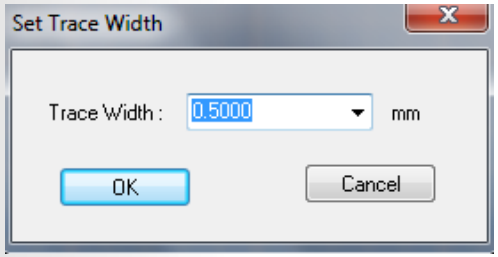
Select a primitive :

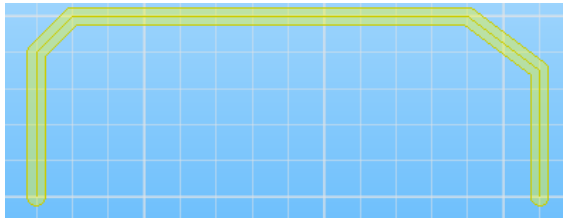
- **Circle (Shortcut Key: F5)**
- **Polygon (Shortcut Key: F6)**
- **Rectangle (Shortcut Key: F7)**
- **Trace (Shortcut Key: F8)**
- **Via (Shortcut Key: F9)**



<u>Note 1 :</u> To draw a Trace

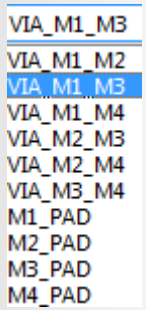
- **Specify the width before**
  - **Draw > Set Trace Width…**

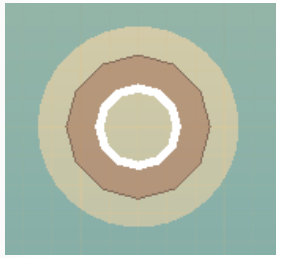


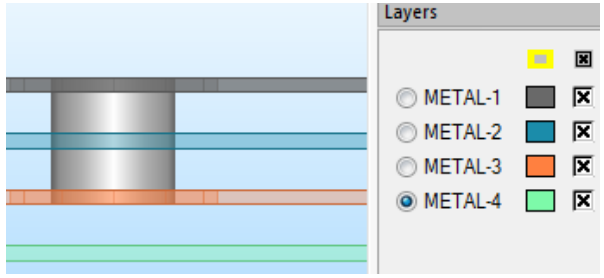


<u>Note 2 :</u> To draw a Via

- **Select a Padstack before**







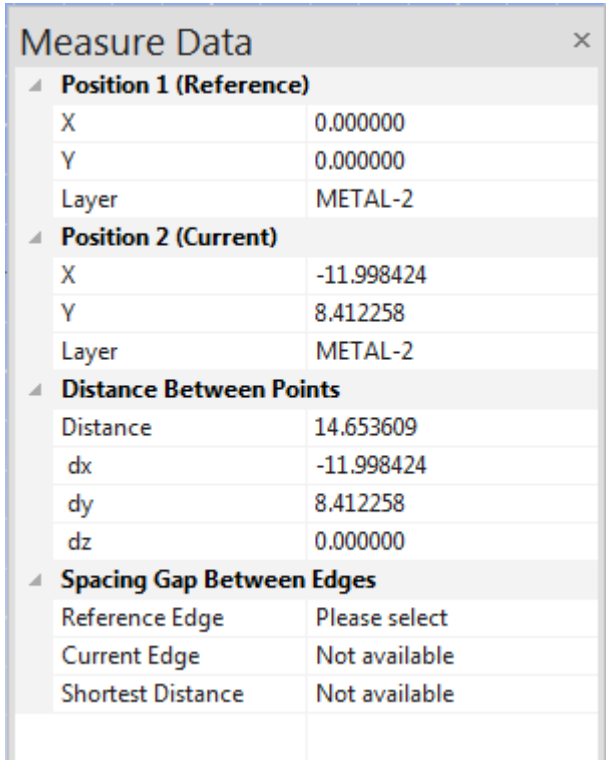
Measuring Data

- **SIwave allows you to measure the distance between points and spacing between edges.**

- **To measure data :**
  - Click Tools>Measure. The Measure Data dockable window appears.

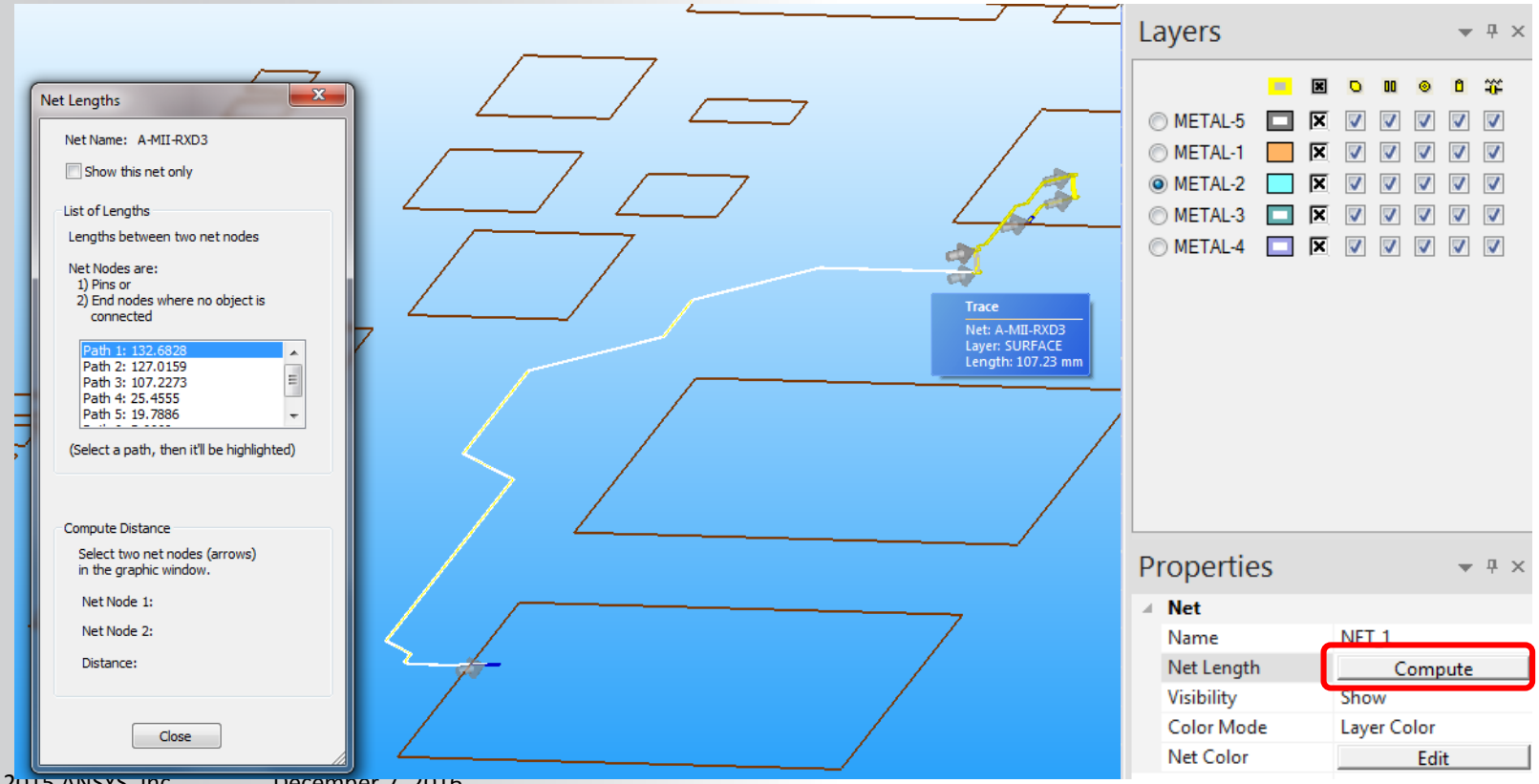
- **To measure the distance between two points:** Click any point for a reference coordinate. This is displayed as Position 1. Move the cursor in the Drawing Area to see the values for Position 2 and Distance between Points. The data updates as the cursor is moved. The shape of the cursor changes when it is snapped to a corner or mid-point.

- **To measure the shortest distance between two edges:** Select an edge in the Drawing Area. This is displayed as the Reference Edge. Move the cursor over another edge to see the values for Current Edge and Shortest Distance.



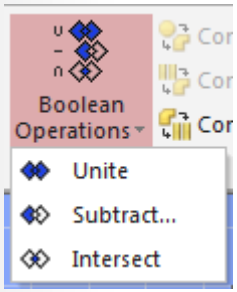
Computing Net Length

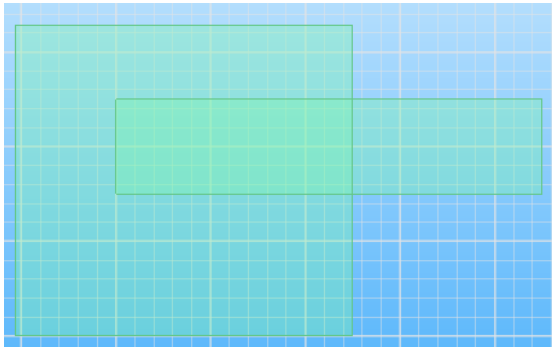
- You can compute the lengths of all possible paths in a net, and also calculate the distance between any two net nodes.
- Tools > Compute Net Lengths or « Compute » button in the properties window



Operations on Plane

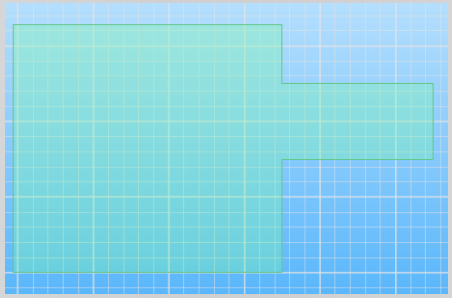
- **Boolean operations can be performed on planes. You can unite, intersect or subtract planes.**

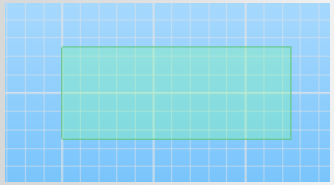


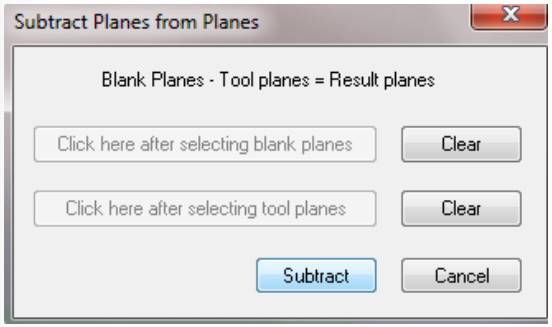


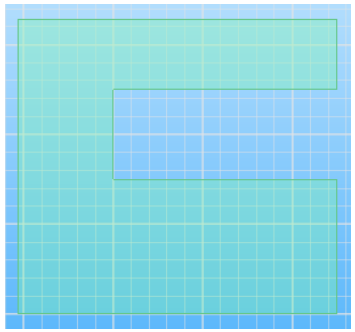
Eg : Uniting Planes

- **Select the two planes that you want to unite.**
- **Click Edit>Boolean Operations>Unite.**



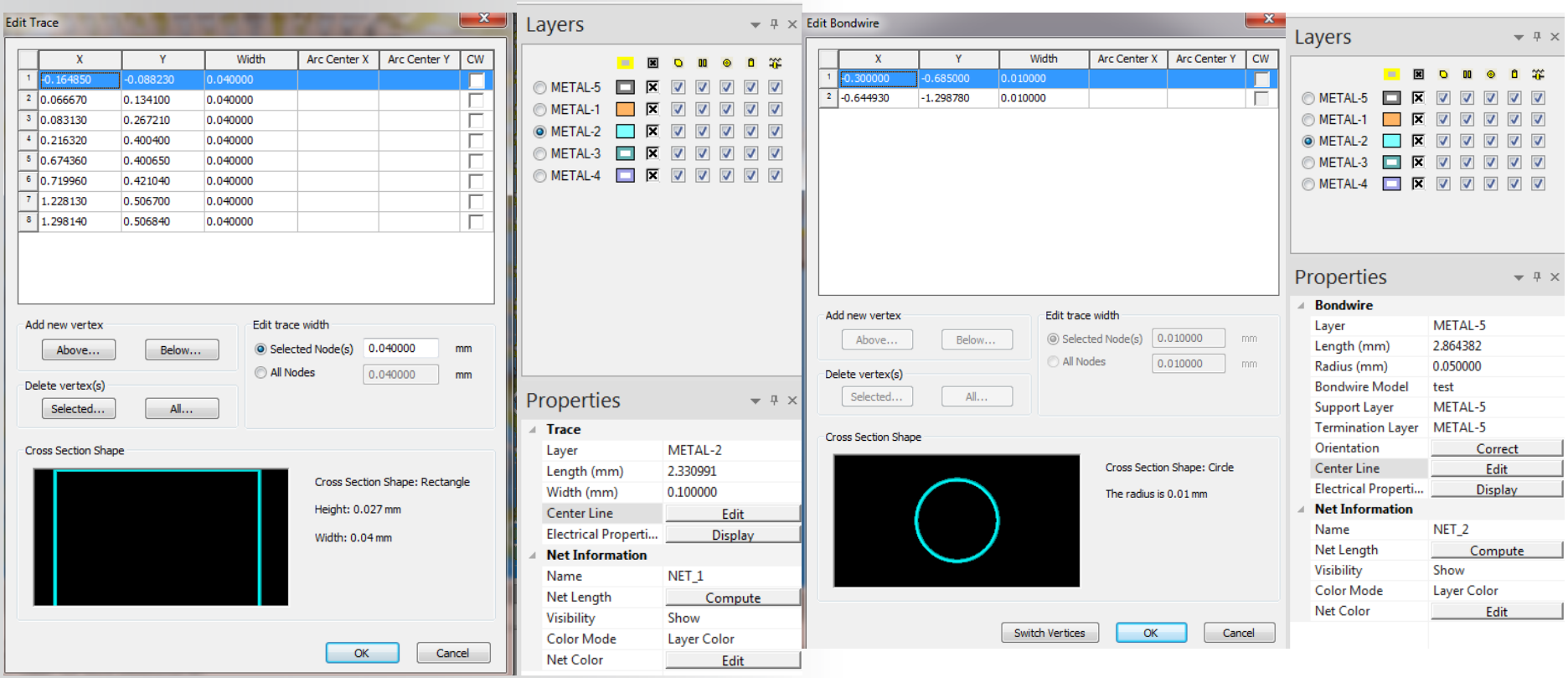






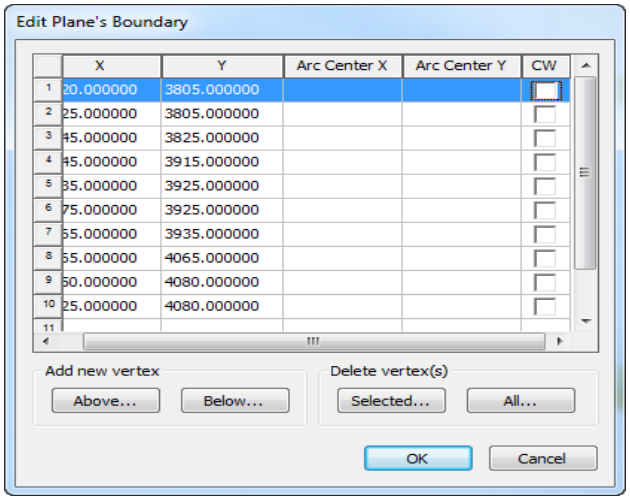
Edit Trace/Bondwire center line properties

- **Trace/Bondwire**
  - To edit a bondwire first graphically select a bondwire in the layout. Bondwire coordinates can be edited. The bondwire radius is also displayed

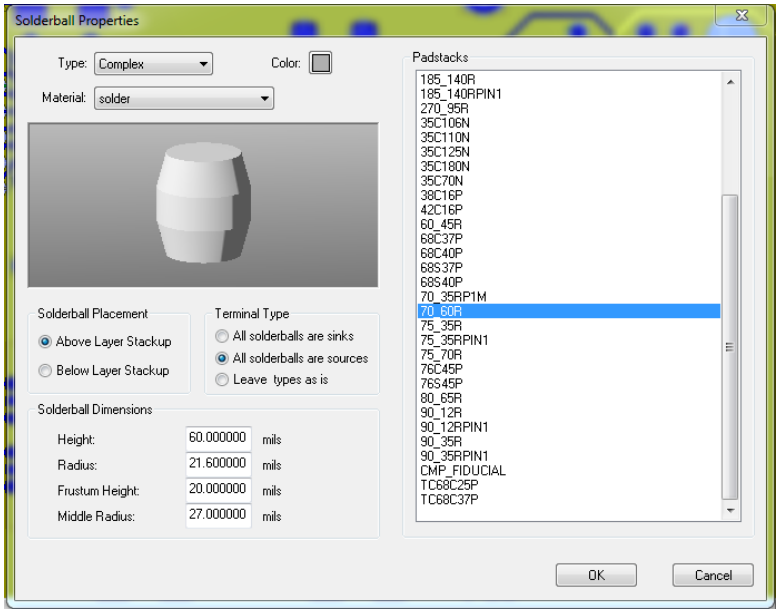


Edit Plane / Solderball properties

- **Plane (Boundary/Cutout)**
  - Manually edit plane boundaries. To activate this option graphically select a plane

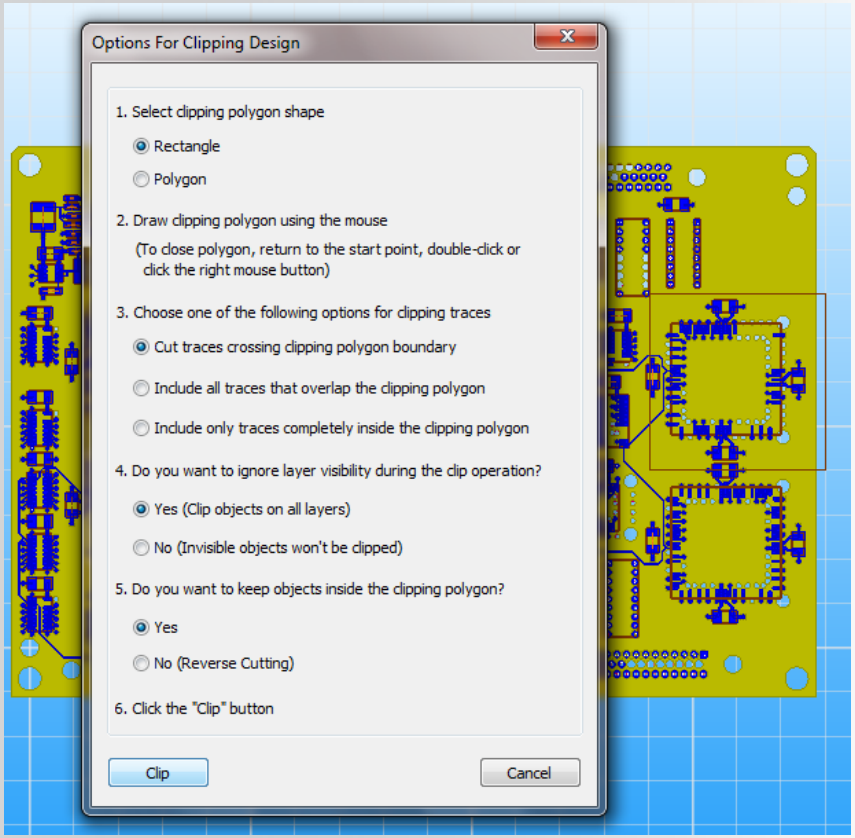


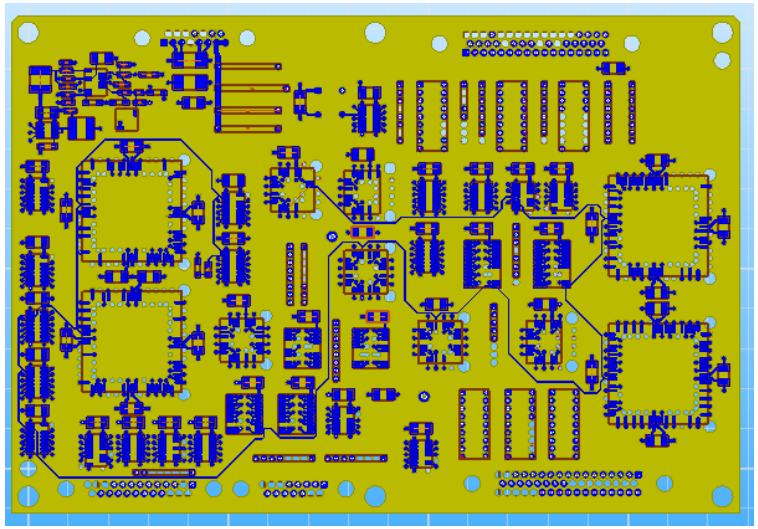
- **Solderballs**
  - Create solderballs and/or solderbumps on packages. Choose the Padstack on which to create the balls and the radius and height

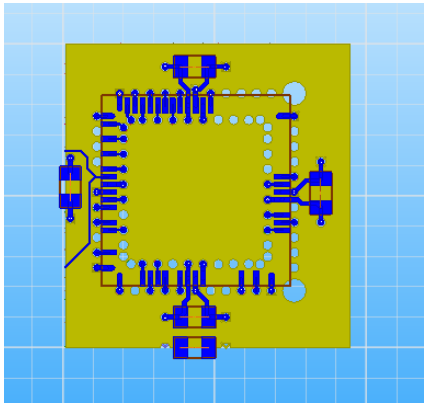


Clipping the Design

- **SIwave provides you with the option to cut out and view a particular region of the design, and ignore the rest of the geometry .**
- Edit > Clip Design
- Follow the 6 steps > Clip

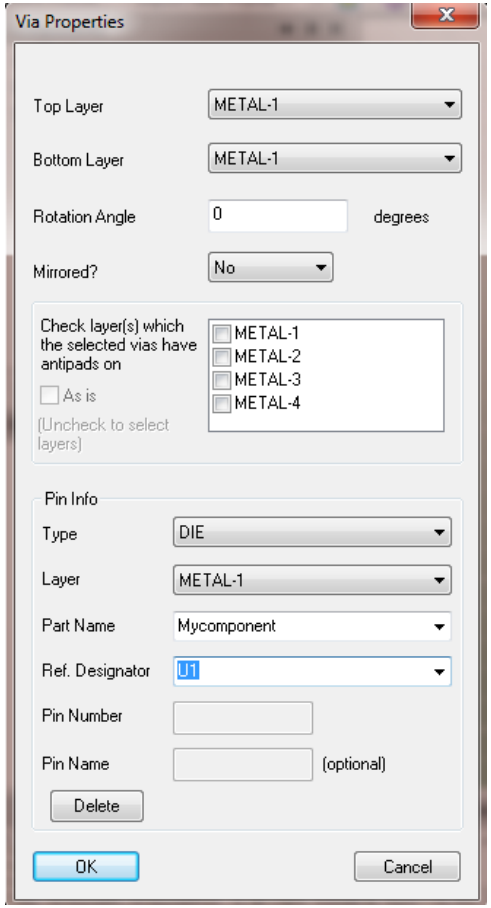






Create a custom Reference Designator

- How to create your own reference designator inside SIwave UI ?
  1. Select via(s)/pad(s) of interest (those you wish to classify as belonging to a part/ref des.).
  2. Right-click and select "Properties" in the pop-up menu.
  3. In the "Via Properties" dialog set the following under the "Pin Info" section:
     - Type (either BGA or DIE)
     - Part name (any reasonable string)
     - Reference designator (any reasonable string)
     - Pin name (any reasonable string).
       -This field is disabled if more than one pad/via has been selected; in this case, pin names are automatically generated (“1", “1", ...)



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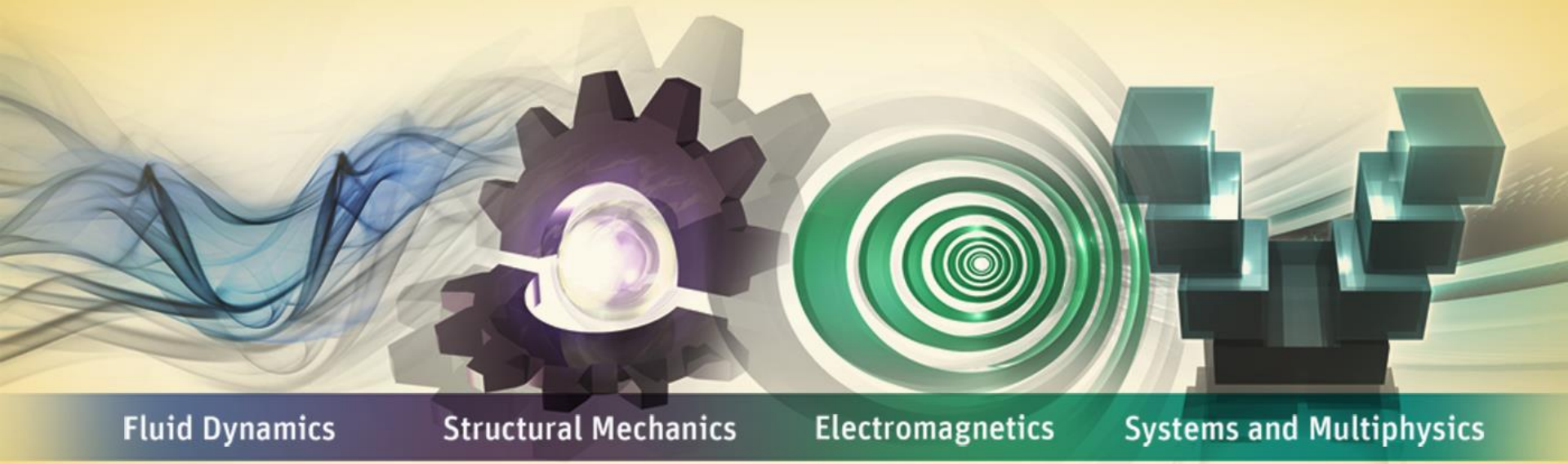
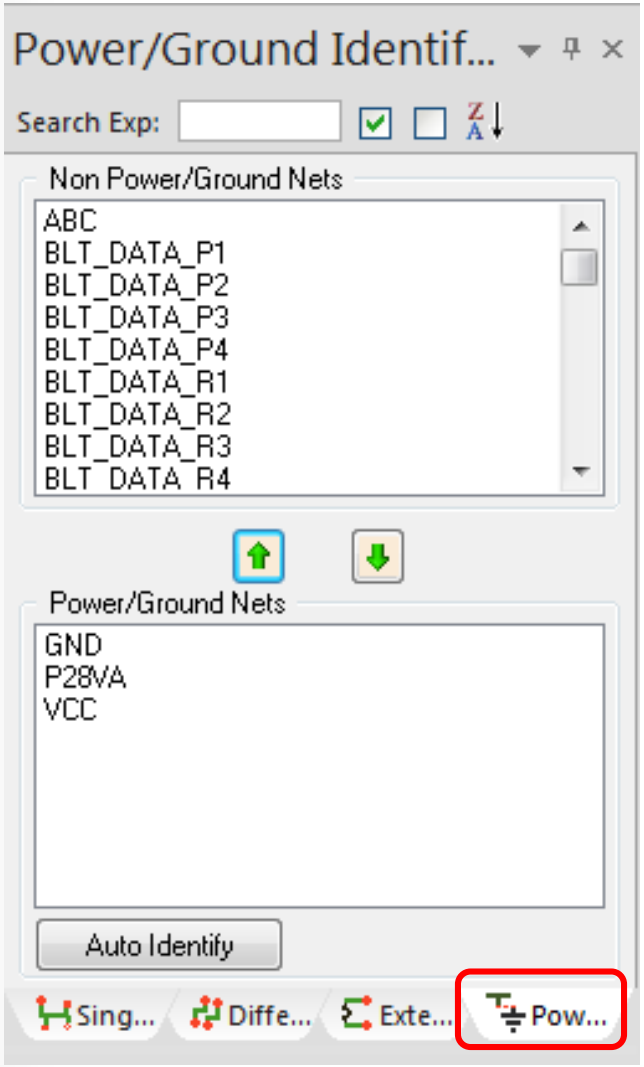
3D Export



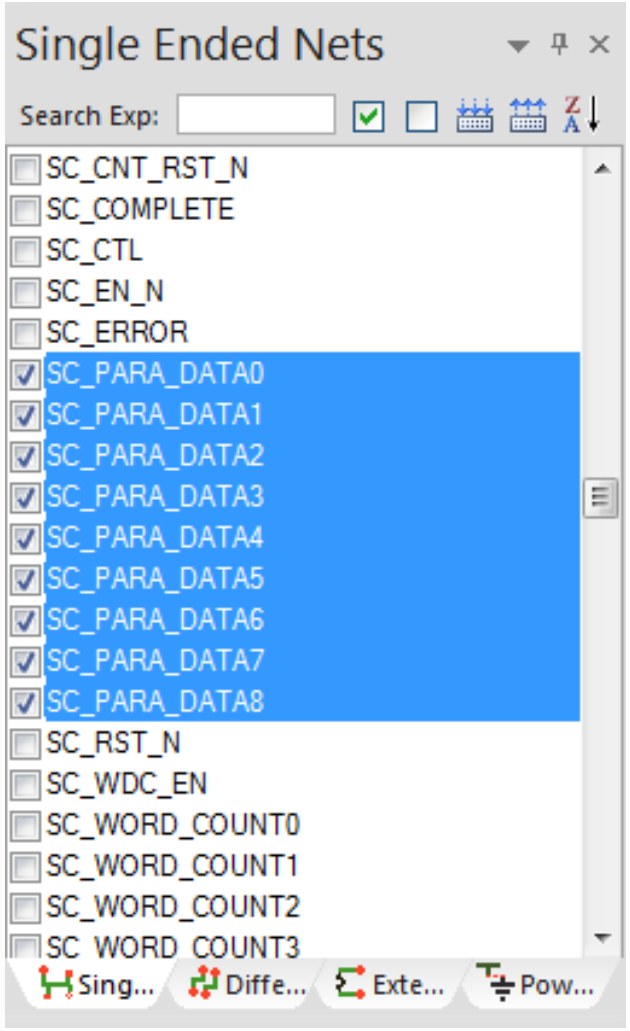
How to do a 3D export?

1. Identify Power and Ground nets



How to do a 3D export?

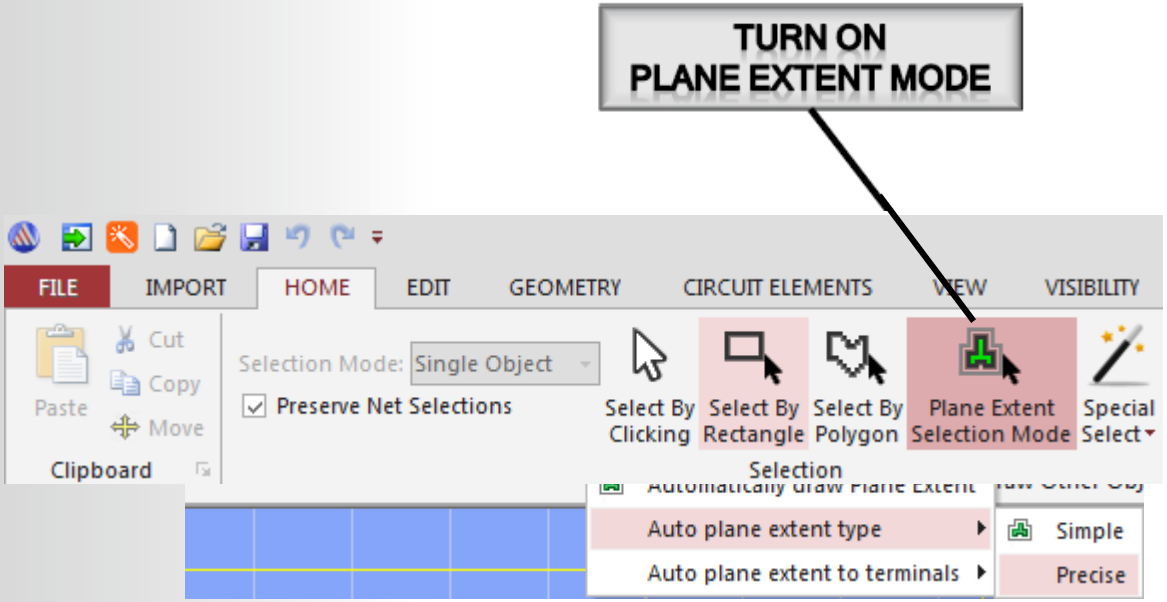
2. Select Nets you wish to simulate

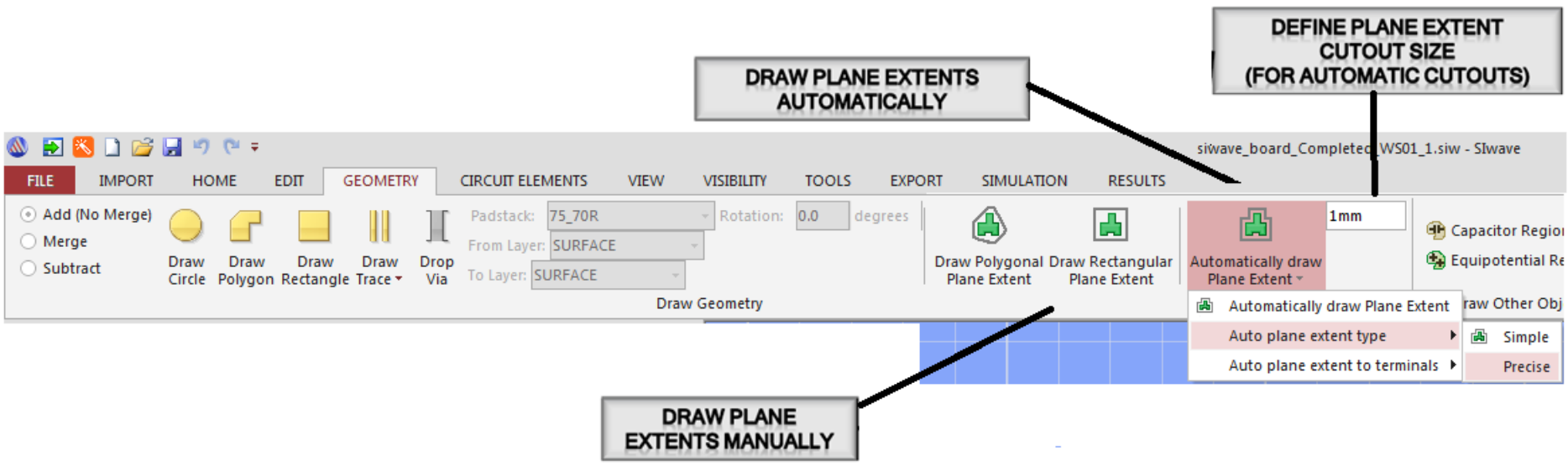


How to do a 3D export?

3. Define Plane Extents

- **Automatic**
  - Simple
  - Precise
  - Type a clip distance
- **Manual**
  - Draw Polygon
  - Draw Rectangle





What is a Plane Extent?

– Plane extents define the region that will be cutout when exporting to HFSS, Q3D Extractor, ANSYS Workbench, or Designer.

– Plane extents define the region that will be cutout for inclusion within an HFSS solve

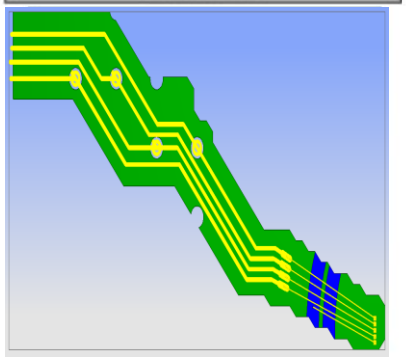
– Plane extent operations

- Users must first define power and ground nets. This allows a cutout on those nets when trying to simulate signal nets.
  - Plane extents can be created automatically or manually
  - – Automatic Plane Extents
  - Define the extent you want the cutout to extend beyond the signal traces (mm, um, mils, inches, …)
    - Simple: Creates polygon cutout without Arcs
    - Precise: Creates polygon cutout with Arcs
  - – Automatic Plane Extents to Terminals
  - Defines the extents to Wirebond, Solderball/Solderbump
    - Simple: Creates polygon cutout without Arcs
    - Precise: Creates polygon cutout with Arcs
  - – Manual Plane Extents
  - User draws a plane extent in the layout editor window
    - Rectangle: Creates rectangular cutouts
    - Polygon: Creates polygon cutouts

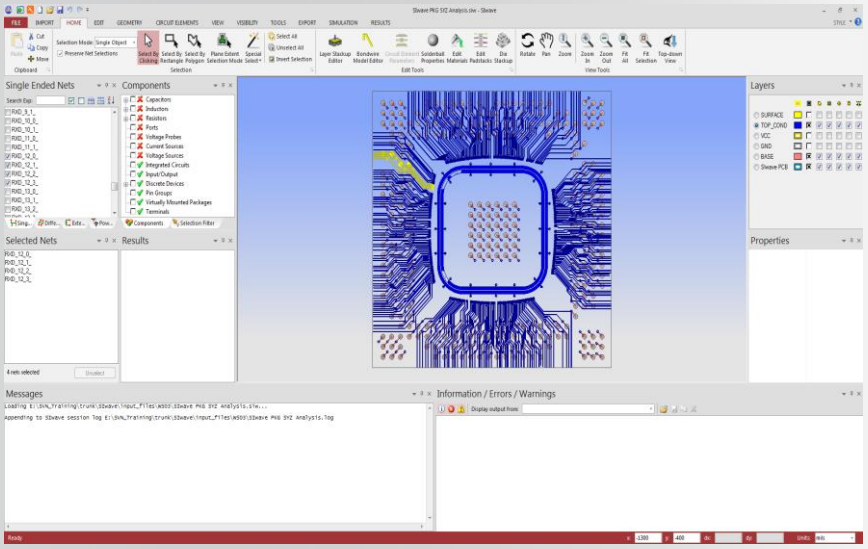
How to do a 3D export?

3D EXPORT PREVIEWS FOR DIFFERENT PLANE EXTENTS

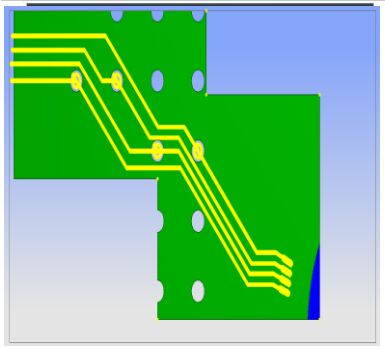
AUTOMATIC PLANE EXTENT AT 0.2 MM



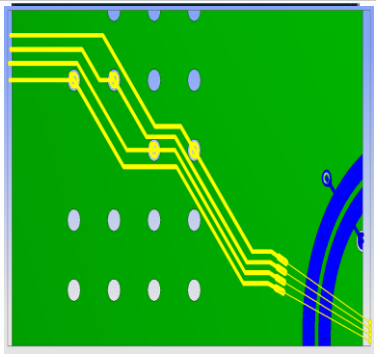
4. Go to Export > Preview Export (Clipped PWR/GND)



MANUAL PLANE EXTENT POLYGON

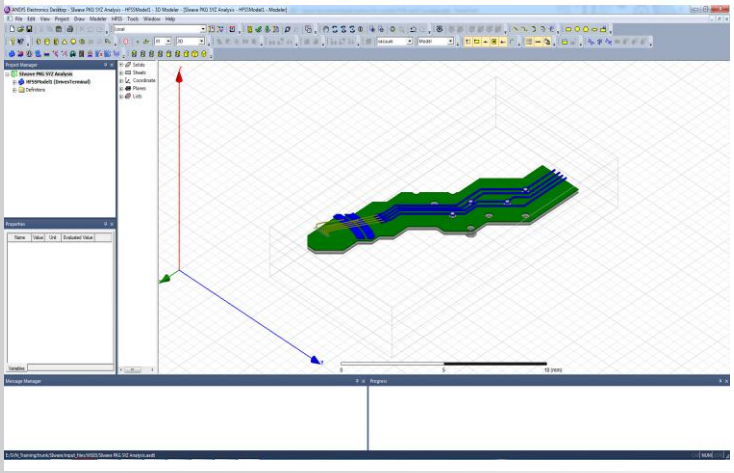


MANUAL PLANE EXTENT RECTANGLE

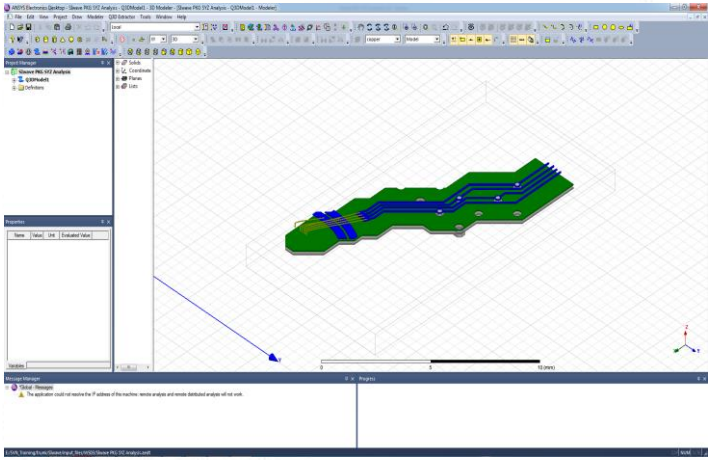


How to do a 3D export?

HFSS

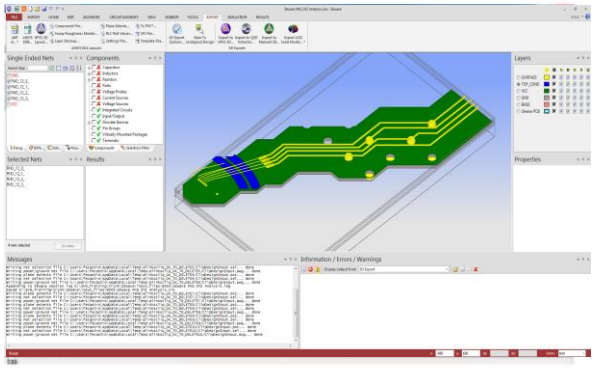


Q3D EXTRACTOR

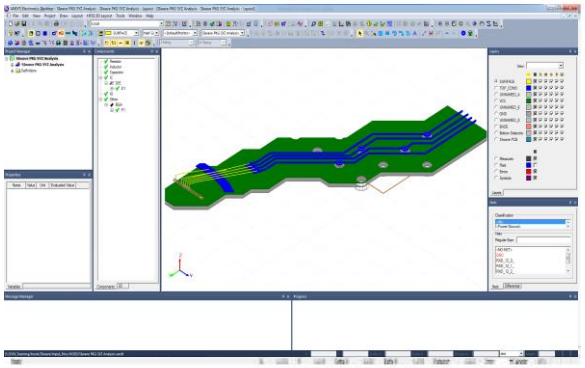


5. Export to HFSS, Q3D Extractor, Designer or ANSYS Workbench

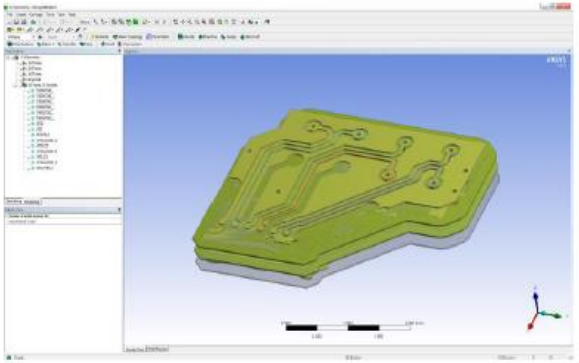
SIWAVE WITH ALINKS



HFSS 3D LAYOUT



ANSYS WORKBENCH



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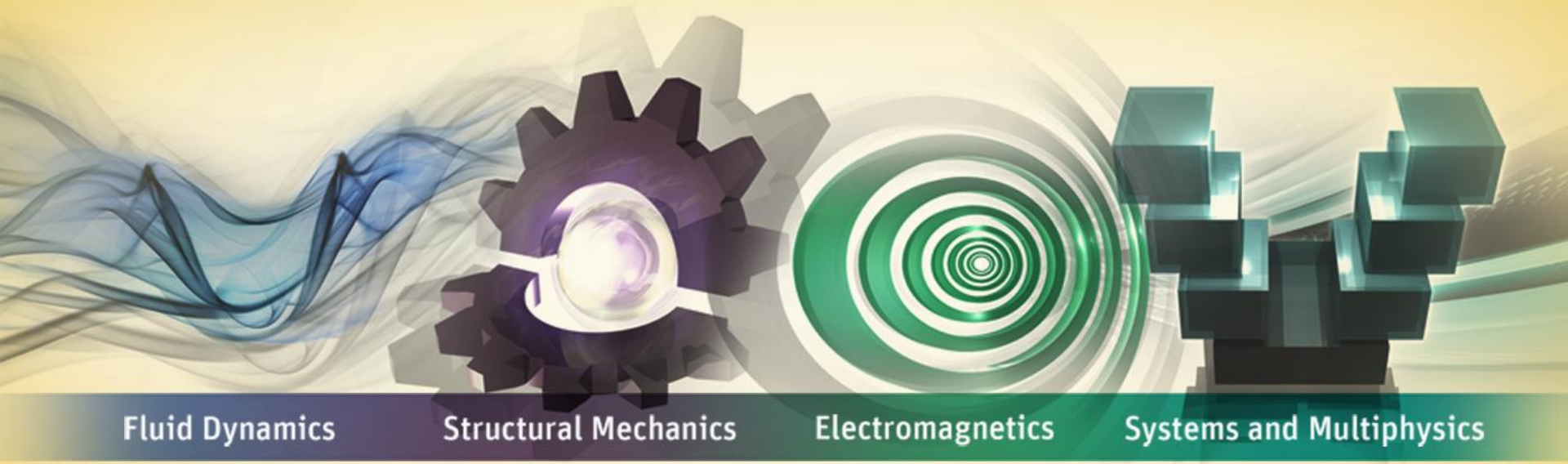
Validation check



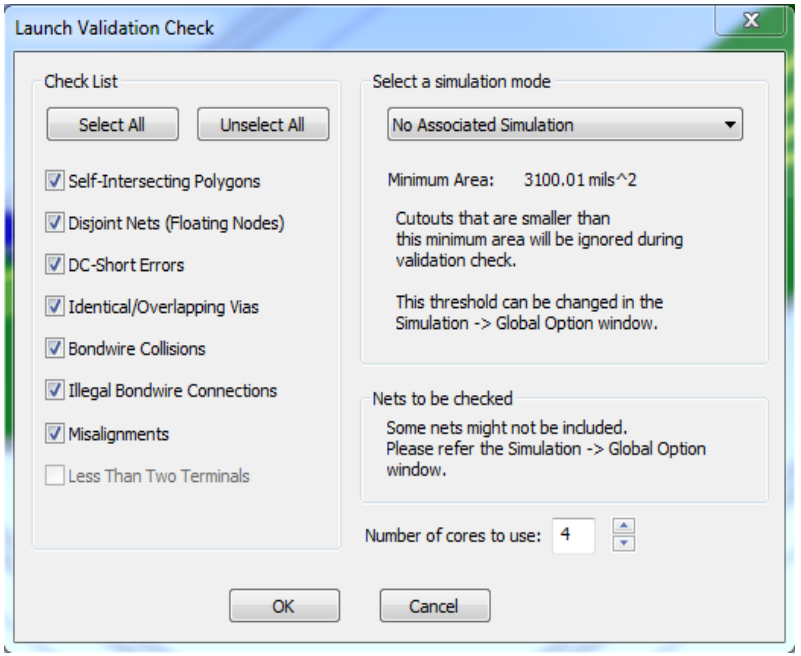
SIwave : Validation check

- **Before you run an analysis on a model, it is very important that you first perform a validation check on the project. When you perform a validation check on a project, SIwave runs a check on all the setup details of the active project to verify that all the necessary steps have been completed and their parameters are reasonable.**

Performing a Validation Check

- **Tools > Validation Check.**

- **Self-Intersecting Polygons**
  - Check for duplicating planes, intersecting edges, and check if voids intersect the plane boundaries.
- **Disjoint Nets**
  - Check if there are any nets that are not completely connected.
- **DC-Shorted Errors**
  - Check if any nets overlap.
- **Identical/Overlapping Vias**
  - Check if any vias are identical or overlap on the same nets.



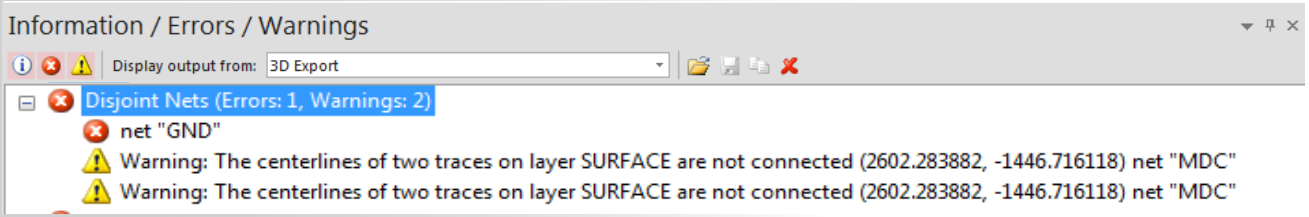
SIwave : Validation check

- **Bondwire Collisions**
  - Check for duplicate or overlapping bondwires.
- **Illegal Connections of Bondwires**
  - Check if the inner radius of the via is more than the bondwire, or if the bondwire extends through the pad.
- **Misalignments**
  - Check for all misalignments, in the following cases:
    - to flag and auto-correct areas where the centerline of a trace is not contained within a plane.
    - if a trace overlaps with a plane, but the centerline of a trace doses not intersect with a plane.
    - if a trace overlaps with other trace, but the centerline of a trace does not intersect with the centerline of other trace.
    - if the boundary of a pad/via intersect with the boundary of a trace, but the center of a via/pad is not located on the centerline of a trace (in other words, the pad/via is not snapped to the centerline of a trace).
    - if the boundary of a plane intersect with the boundary of a pad/via, but the center of the pad/via is not contained in the boundary of the plane.
- **Unreferenced Trace Segments**
  - Check for traces with no reference plane above or below it.

Validation Check : Disjoint Nets

- **Definition of a Net : A 'net' is a continues piece of metal. If two pieces of metal that are defined to be the same net are not DC shorted an error can occur .**
- **Disjoint Nets**
  - Check if there are any nets that are not completely connected and highlights trouble with electrical connections.
  - A very common problem that arises sometimes is that piece of metal that have been added as shield are not physically connected to ground. These floating pieces of ground pour can actually serve as a radiating structure rather than provide effective shielding as the engineer was intending. Any floating pieces of metal should be connected through vias/additional metal or removed from layout.

- **To fix the disjoint nets**
  - Expand the Disjoint Nets error message

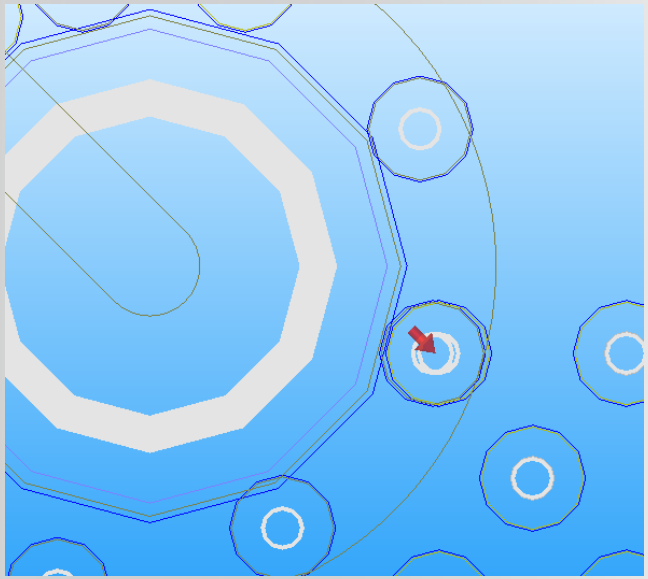


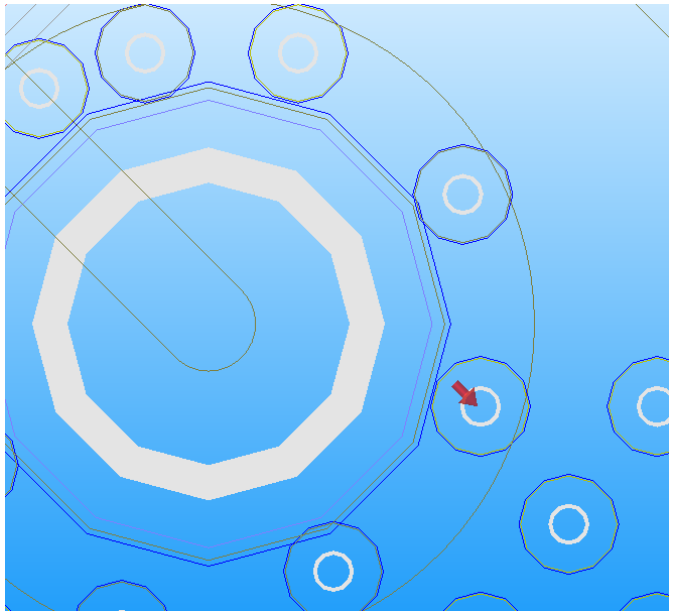
  - The net GND has been identified as having disjoint geometry. Select this net from the nets listing
  - Select Edit -> Nets -> Separate Disjoint Parts
  - Click OK to the resultant message window.
  - Scroll down the nets window and notice that additional nets were created from the disjoint pieces, net-1, net—2,….

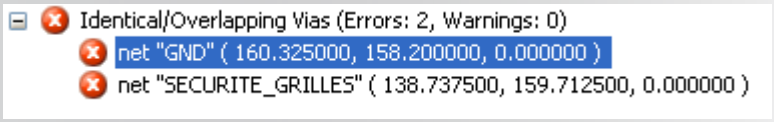
Validation check : Identical / Overlapping Vias

Identical/Overlapping Vias

- **Check if any vias are identical or overlap on the same nets.**

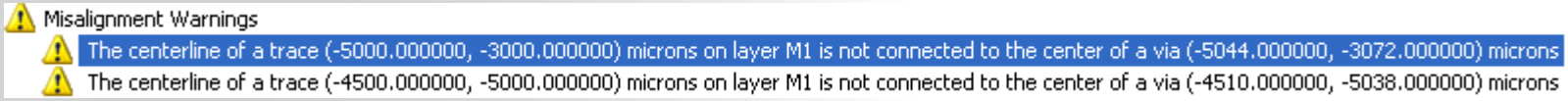


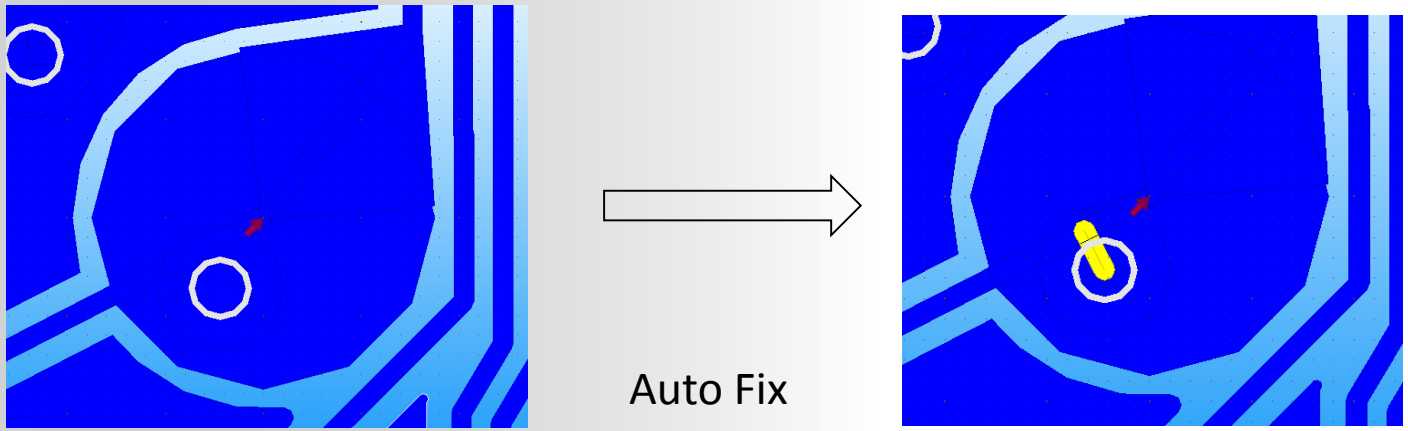




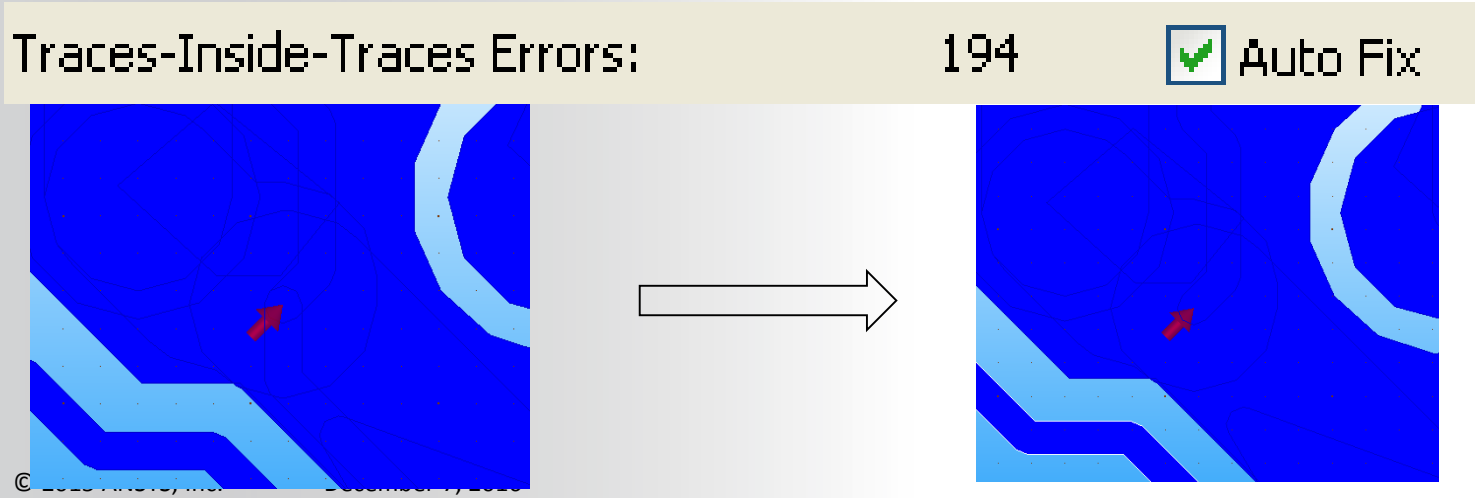
Validation Check : Misalignments

Misalignments :



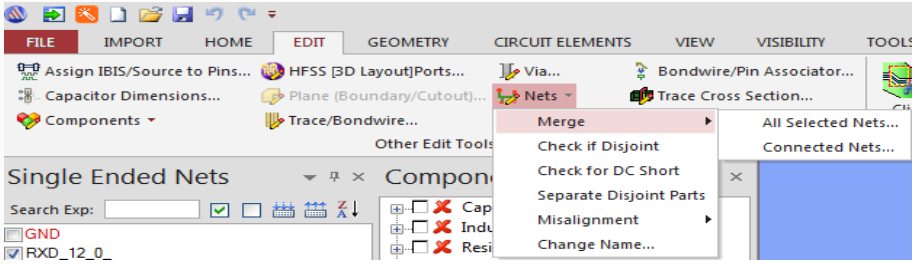


- **Traces-Inside-Traces Errors :**



Nets options

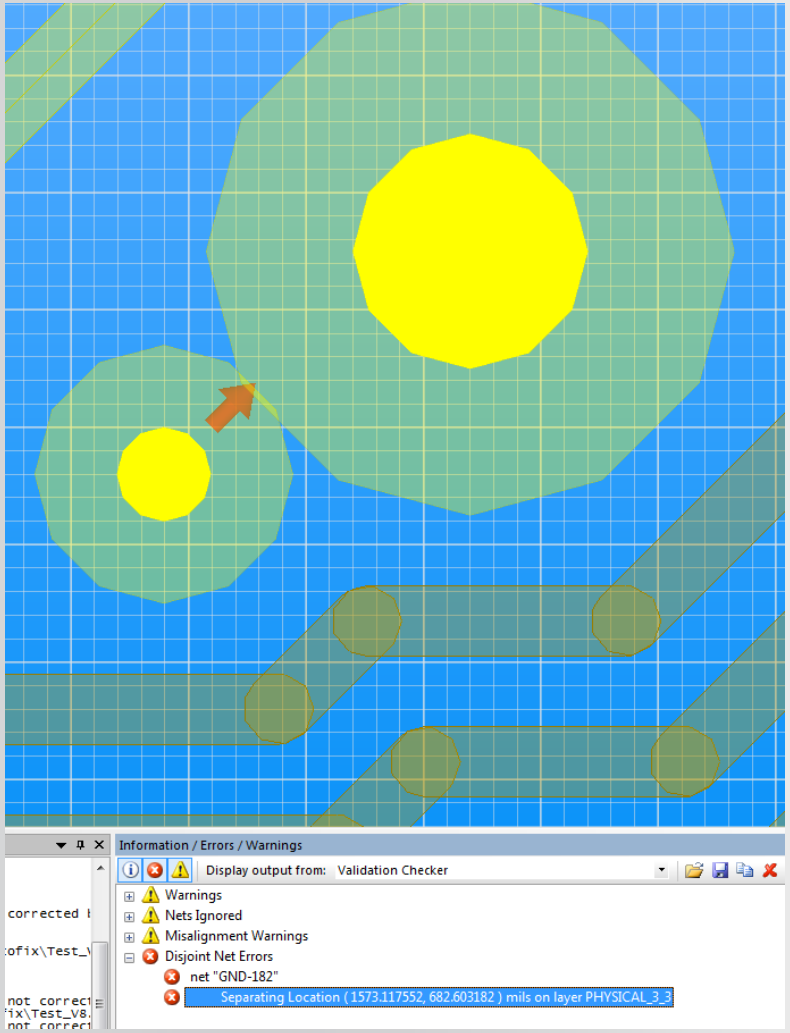
- **Edit > Nets**
  - Most of the Nets options are used to correct geometry that has been imported from a third-party layout tool. It is useful to first run a Validation Check (which will be described later in this section) to detect potential issues



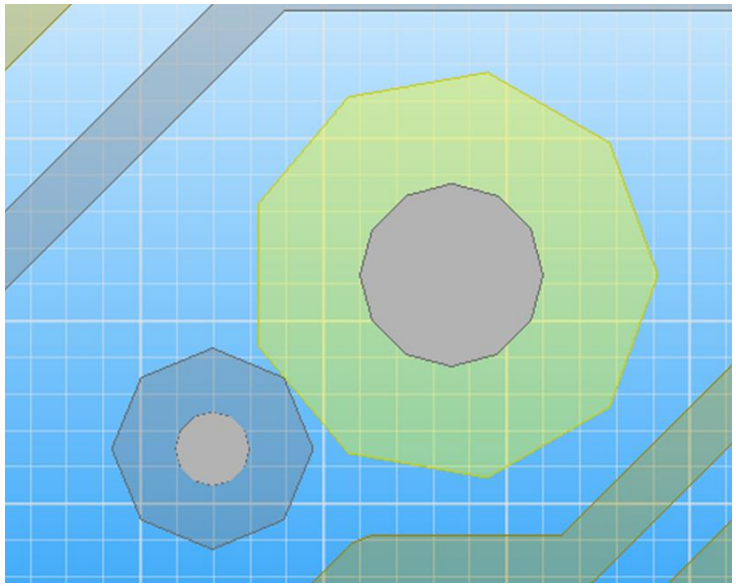
  - **Merge**
    - **All Selected Nets**
      - Merges all electrically connected nets that have been selected
    - **Connected Nets**
      - Merges all electrically connected nets in the set into a single net. It is not necessary to manually select these nets
  - **Check if Disjoint**
    - Only checks the selected nets. The complete layout can be checked during the Validation Check
  - **Check for DC Short**
    - Only checks the selected nets. The complete layout can be checked during the Validation Check
  - **Separate Disjoint Parts**
    - If all parts of a net are not electrically connected this operation will allow these parts to be separated into different nets
  - **Misalignment**
    - Select and View
      - No operation is performed, this is a visualization only
    - Correct
      - SIwave will try to correct the alignment. The misalignment will be detected in the Validation check. This occurs when a design has traces whose center lines are not connected to any planes or pads or the center lines of other traces
  - **Change Name**
    - Enter a new name

Disjoint Nets

Original : The two pads look to be connected



For solver setup, the arcs are discretized and so they are not connected.

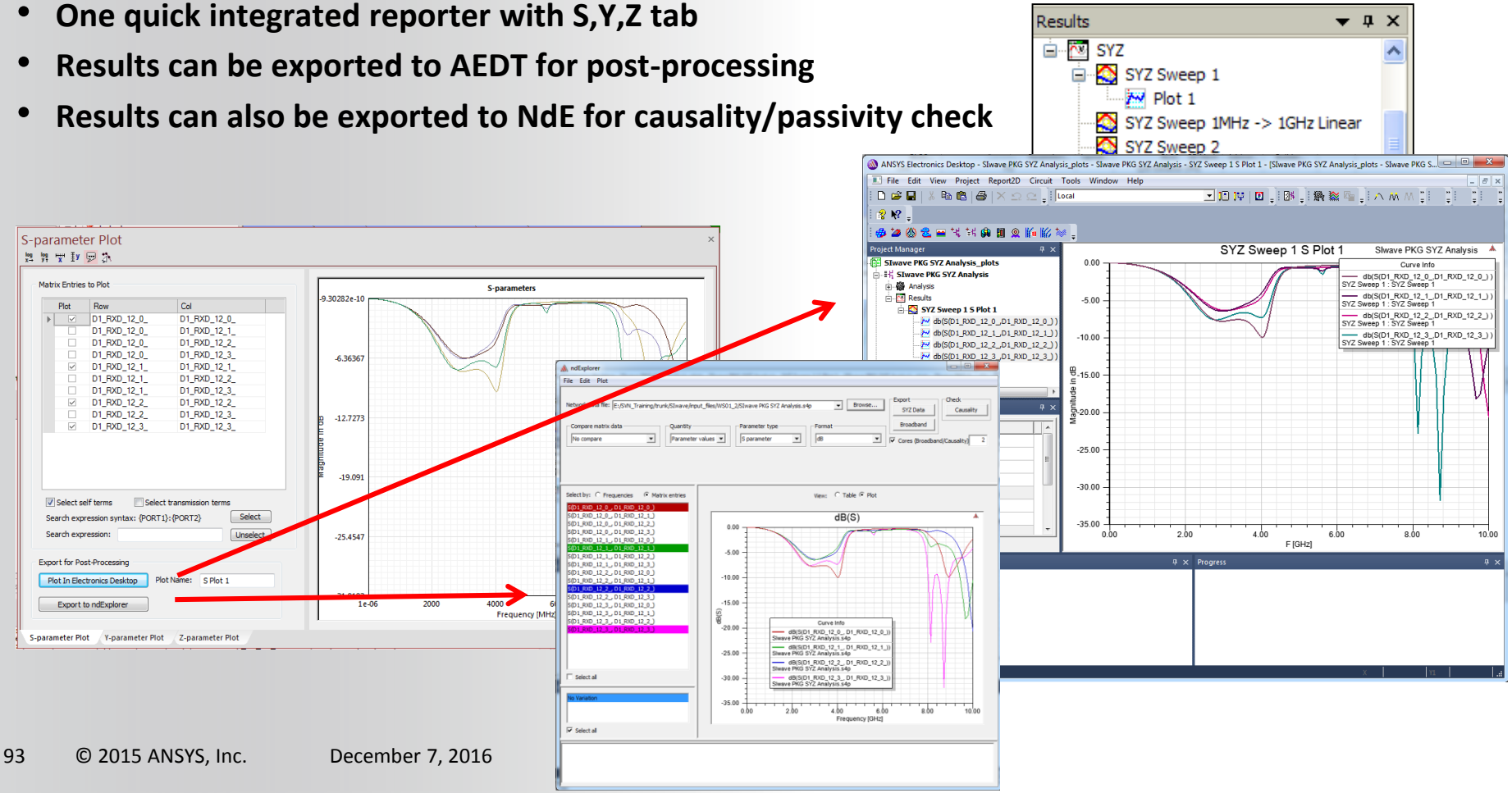


The auto fix can't separate the disjoint nets, but the validation check will point the separating locations of disjoint nets
If a trace connecting two pads in the design is added manually, the net gets well-connected.

SIwave GUI Controls – Results

SIwave Desktop : Results Window

- Users can define solve, and post-process multiple resonant mode, frequency, SYZ, etc., simulations
- Simulation results are no longer stored in the *.siw file but rather are stored in the *.siwaveresults subdirectory. Far-field results and network parameters are accessed from the desktop
- One quick integrated reporter with S,Y,Z tab
- Results can be exported to AEDT for post-processing
- Results can also be exported to NdE for causality/passivity check



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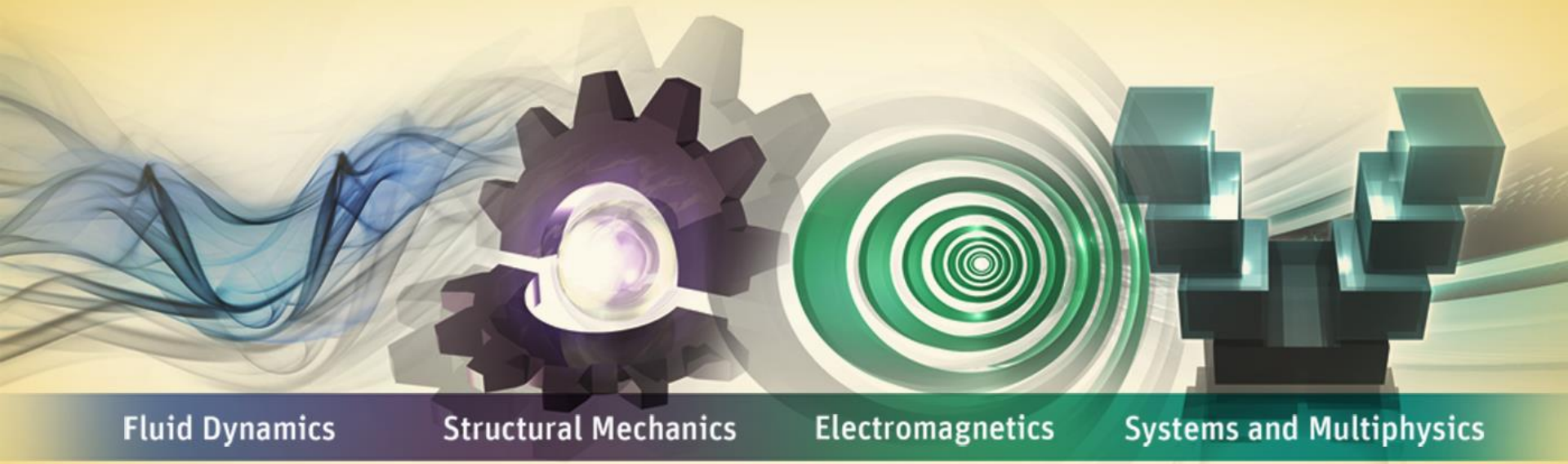
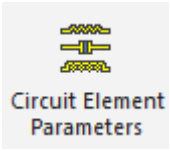
Circuit Element



SIwave Circuit Element Parameters

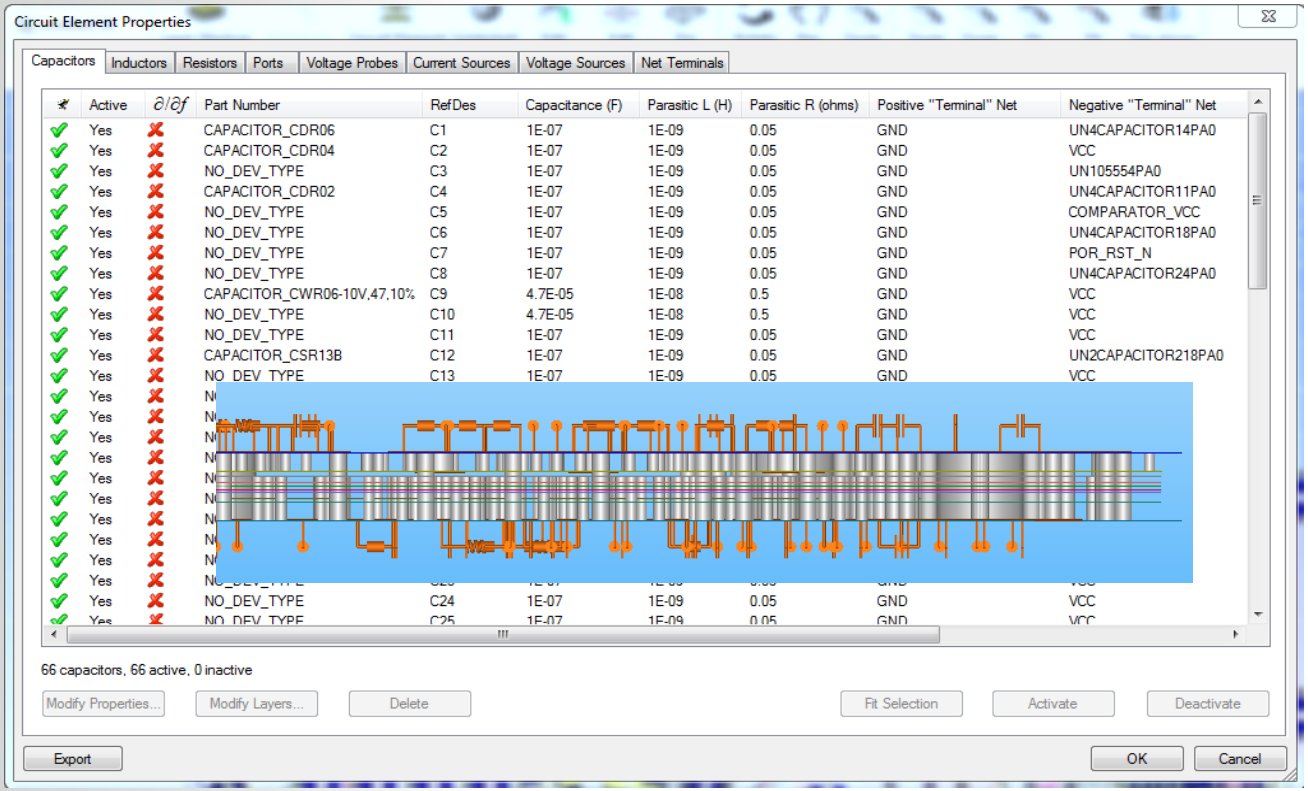


Home > Circuit Element Parameters

- For manufacturer supplied components: you can see the manufacturer name, series number, global parts, circuit elements, and pins.
- For local components (created and placed by you): you can see the part name, circuit elements and pins.
  - **Next to each pin number, you can see the net to which it is attached.**

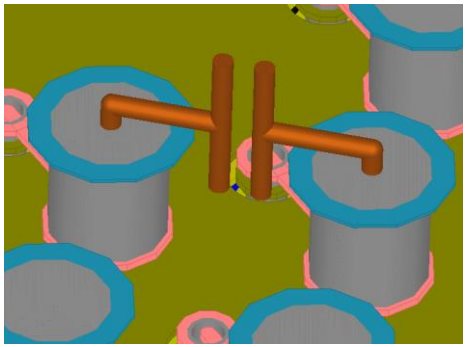
Set Active or **Set Not Active**

A green check mark in front of the element shows that it is active and will be included in the analysis. A red cross shows that is inactive.



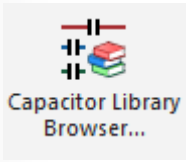
Passive components

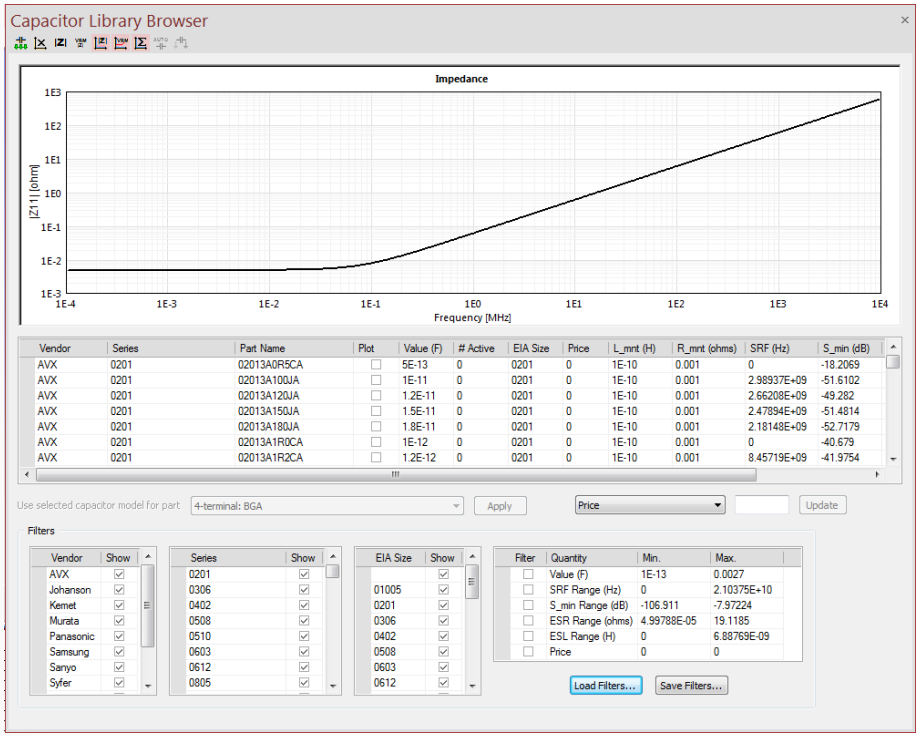
- Direct import of passive component

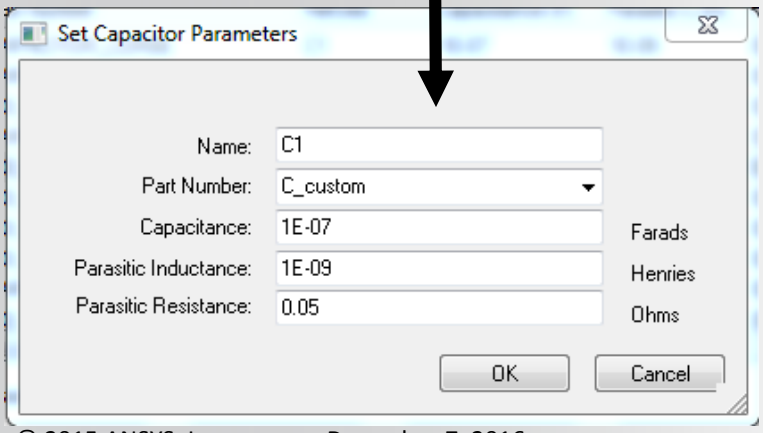


Choosing appropriate model

- Three methodologies :
- Ideal resistor, inductors and capacitors
- TouchStone representation of Capacitors, Inductors, Resistors, and ICs
  - Vendor libraries of commonly used components (ESR, ESL included)
- Equation based RLC parasitics
  - User defines parasitics at specific frequency

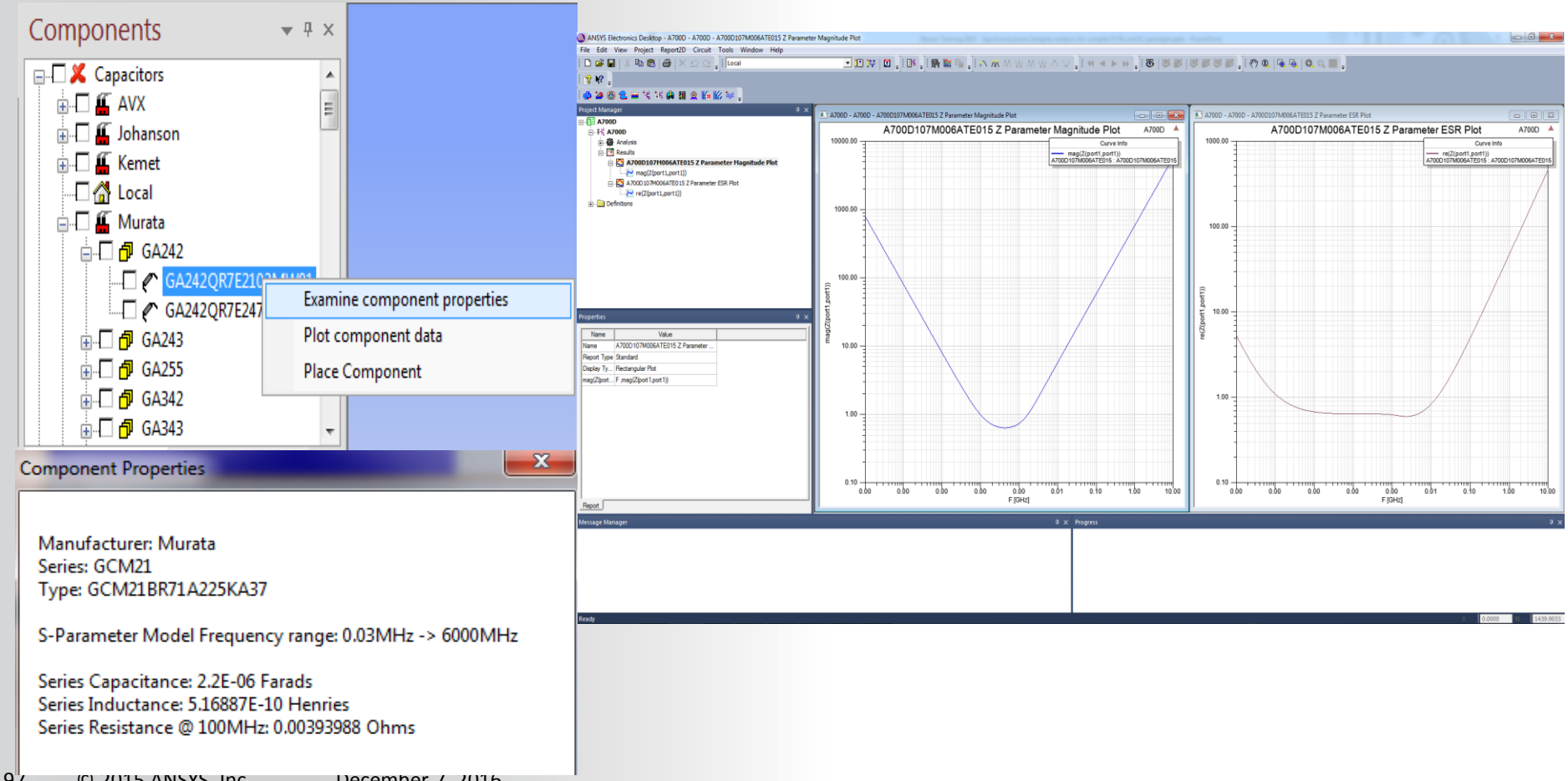






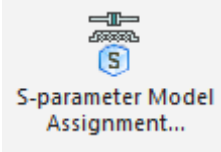
Examine Component Properties

- **If you have a global part name selected: you can examine component properties, plot the component's impedance vs. frequency graph, or place a component either on the top layer or bottom layer**

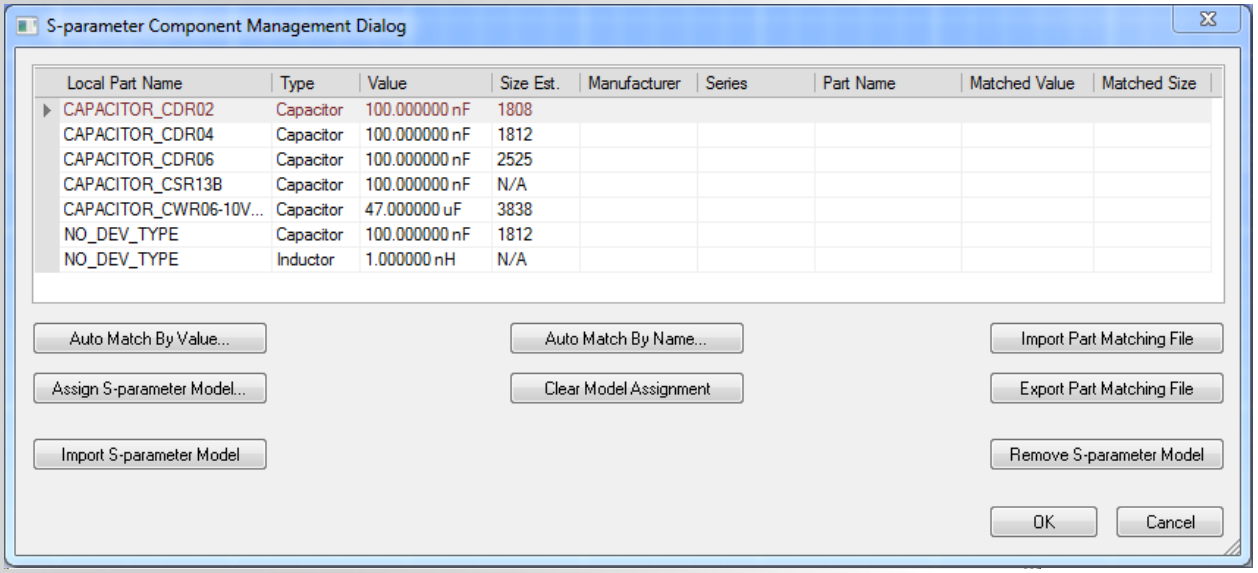


SIwave : Component Management

To launch the Component Management dialog



- **Tools > S-Parameter Model Assignment…**

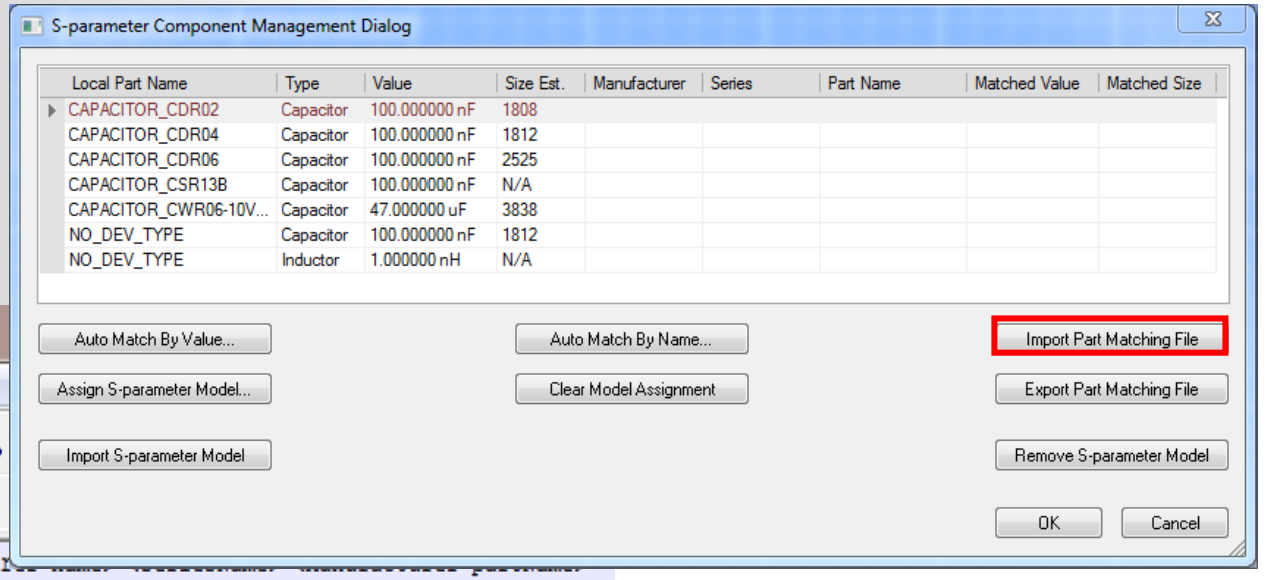


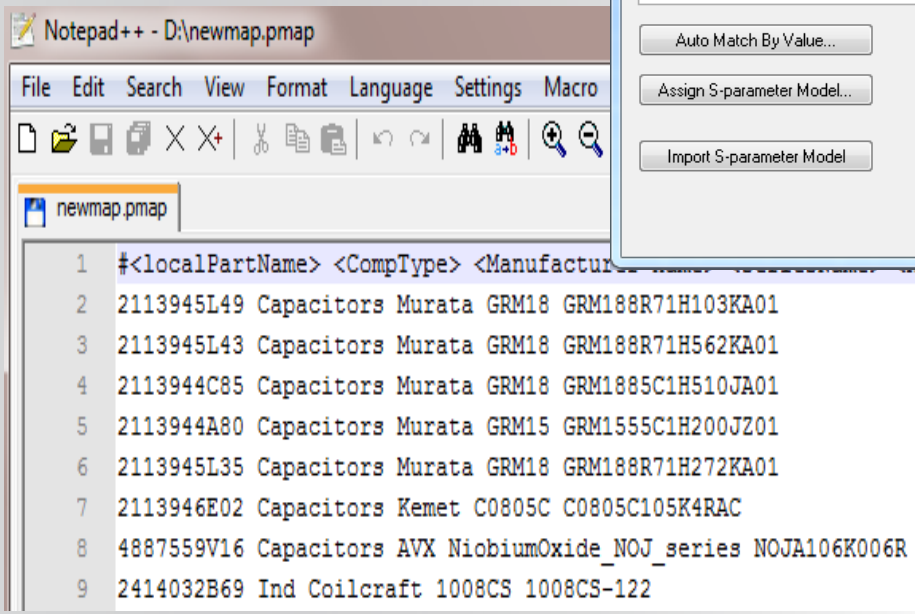
- **Matching can be done :**
  - Automatically by Matching part names or values
    - Click **Auto Match By Value...** or **Auto Match By Name...**
  - Using a matching File :
    - Click **Import Part Matching File …**

SIwave : Part Matching File

In the Component Management dialog

- **Import Part Matching File**

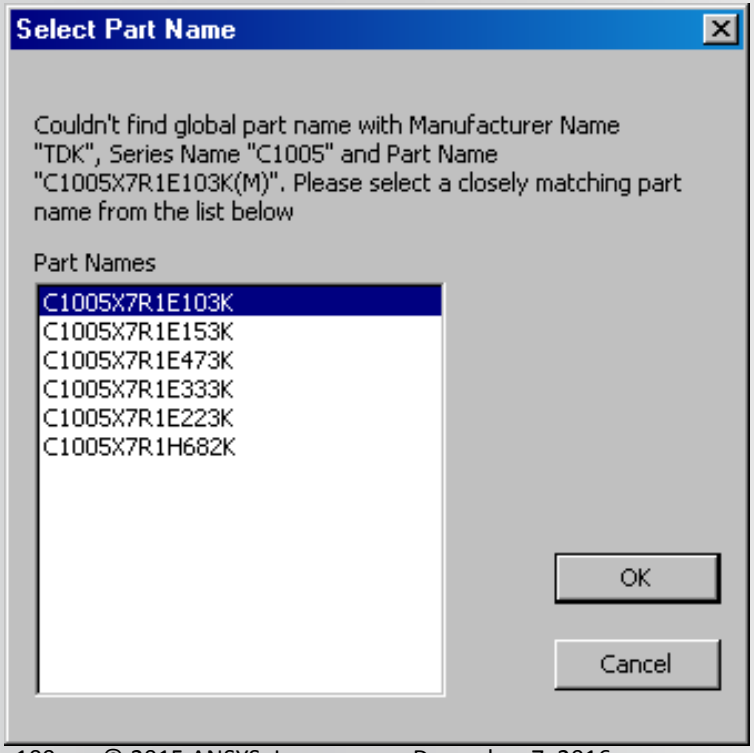


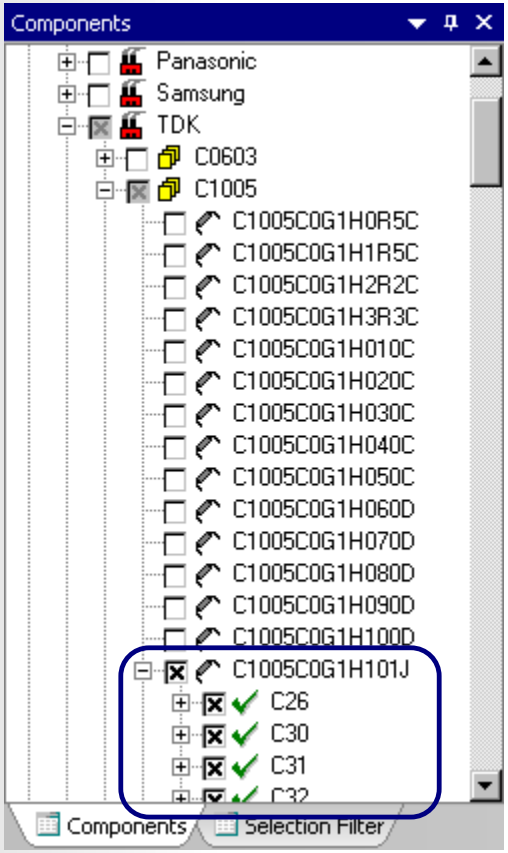


SIwave : Part mapping file

Part Matching from Part Number

The vendor part number in the BOM may not be an exact match to a value in the library.





Wide-band scattering-parameter models are automatically assigned from the SIwave library.

SIwave : part mapping file

*** Syntax for specifying parts:**

<part name> <type> <val> <pin order>

which gives little clue as to supported strings for the <type>, <val>, & < pin order> fields

There is a component mapping file that has the format like this:

```
# <partname> <ParasiticCap> <ParasiticInd> <ParasiticRes>
R_PAK_0402X4-15,5%,31.25MW,N/AA     Res     1.500000e+01
R_0603-750,1%,1/16W,N/A-1%,1/1A     Res     7.500000e+02
R_0603-75,1%,1/16W,N/A-1%,1/16A     Res     7.500000e+01
R_0603-7.5K,5%,1/16W,N/A-1/16WA     Res     7.500000e+03
```

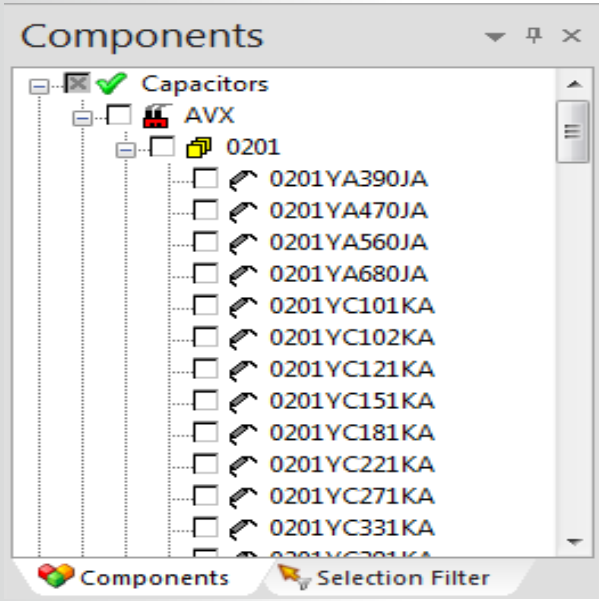
Which can be exported through **File > Export > Component Mapping File**

Then there is a PMAP file which has the format:

<CustomerPartNumber> <Type> <Vendor> <Family> <PartNumber>

Example : part mapping file

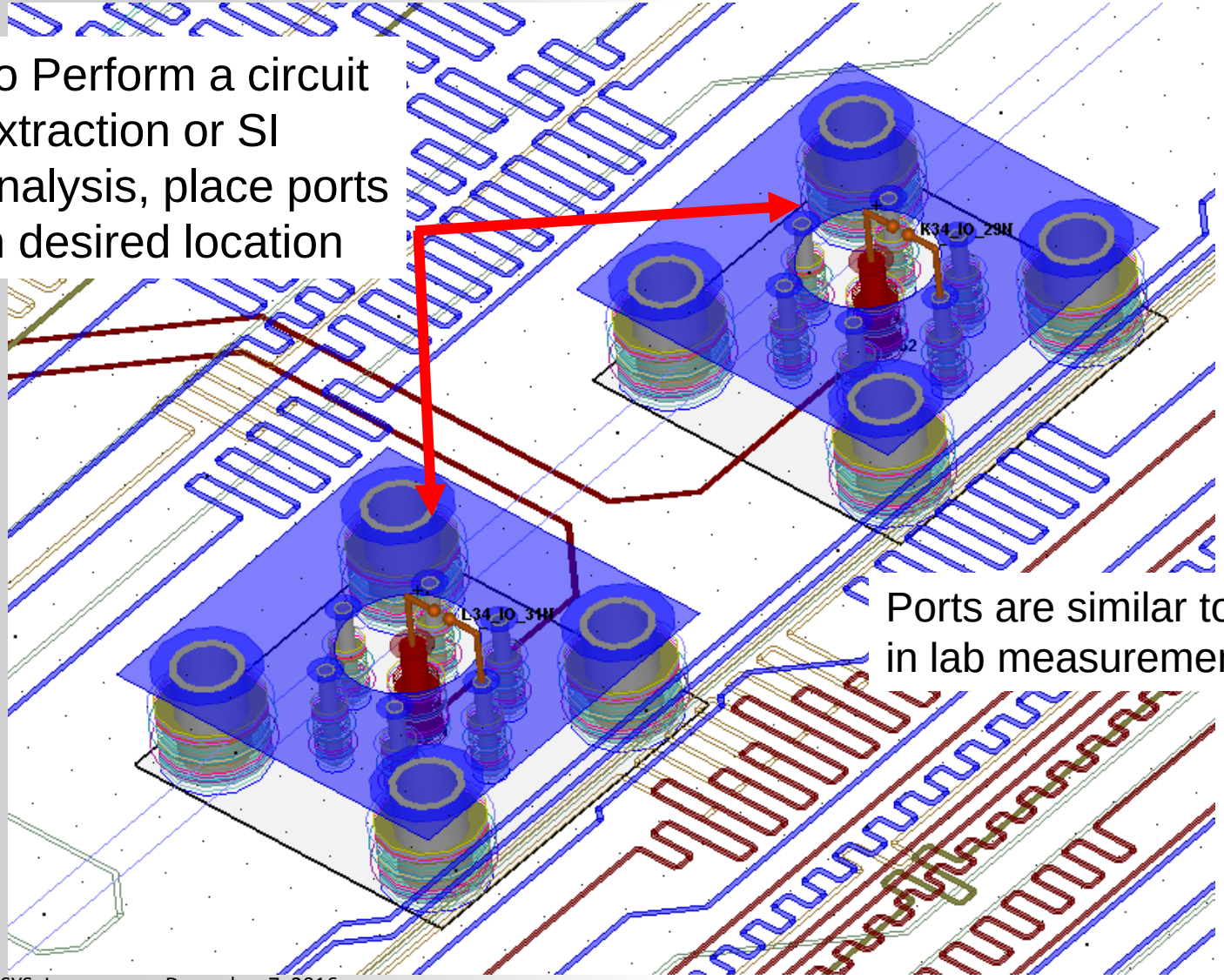
- So if the customer has a part number called CUST203204932 which is a 0201 cap that would map to an AVX capacitor family 0201 part number <0201YA390JA>:



- Then the Customer.PMAP file would be a text file that would have then entry:
  - CUST203204932 Capacitors AVX 0201 0201YA390JA
- This file would perform the mapping under the Tools à Component Database à Part Matching File

SIwave : Port Assignment

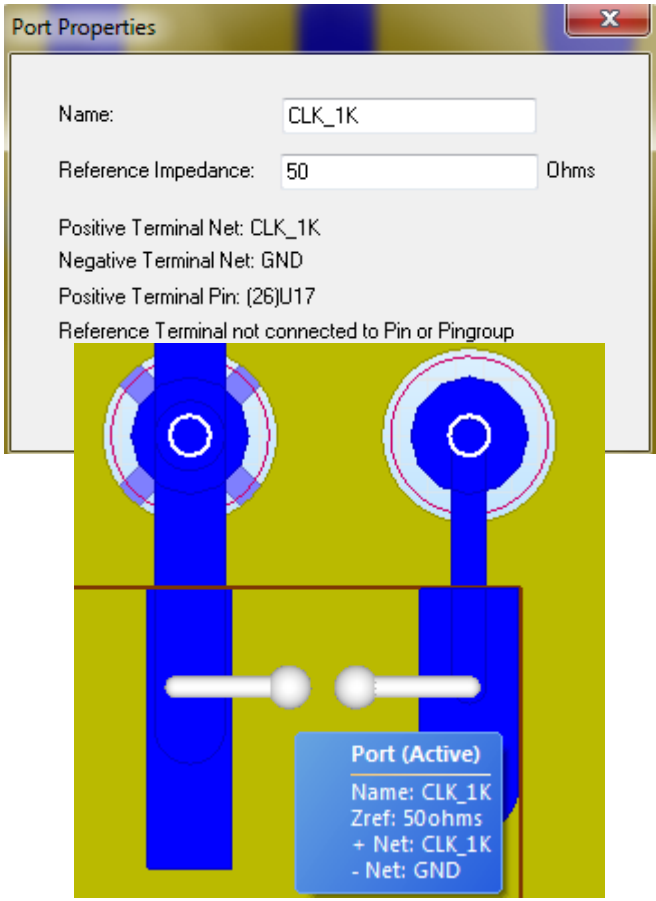
To Perform a circuit extraction or SI analysis, place ports in desired location

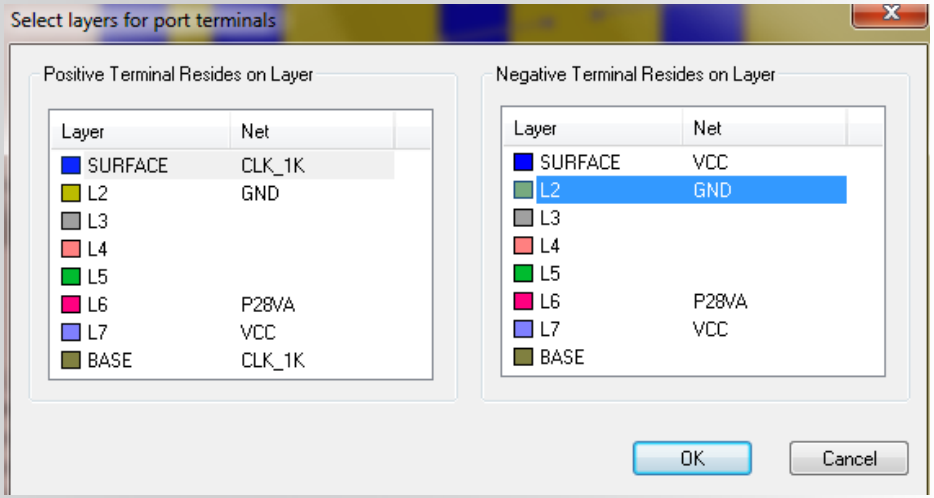


Ports are similar to probes in lab measurements

SIwave : Manually draw a Port

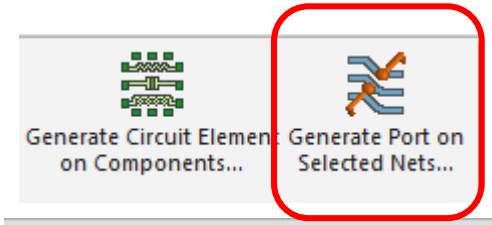
- Top-Down view must be activated
- Circuit Elements > Add Port
- Click 2 times to define the positive and negative pin.
- Define the Positive and Negative Terminals by choosing a layer
- A port can be placed everywhere

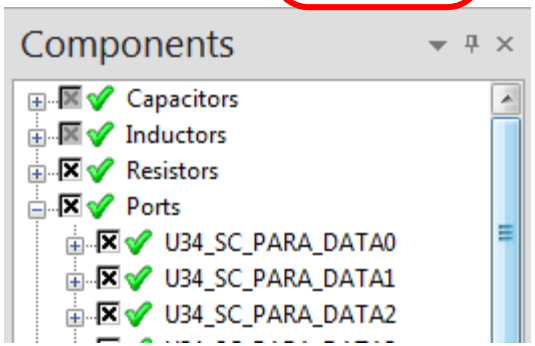


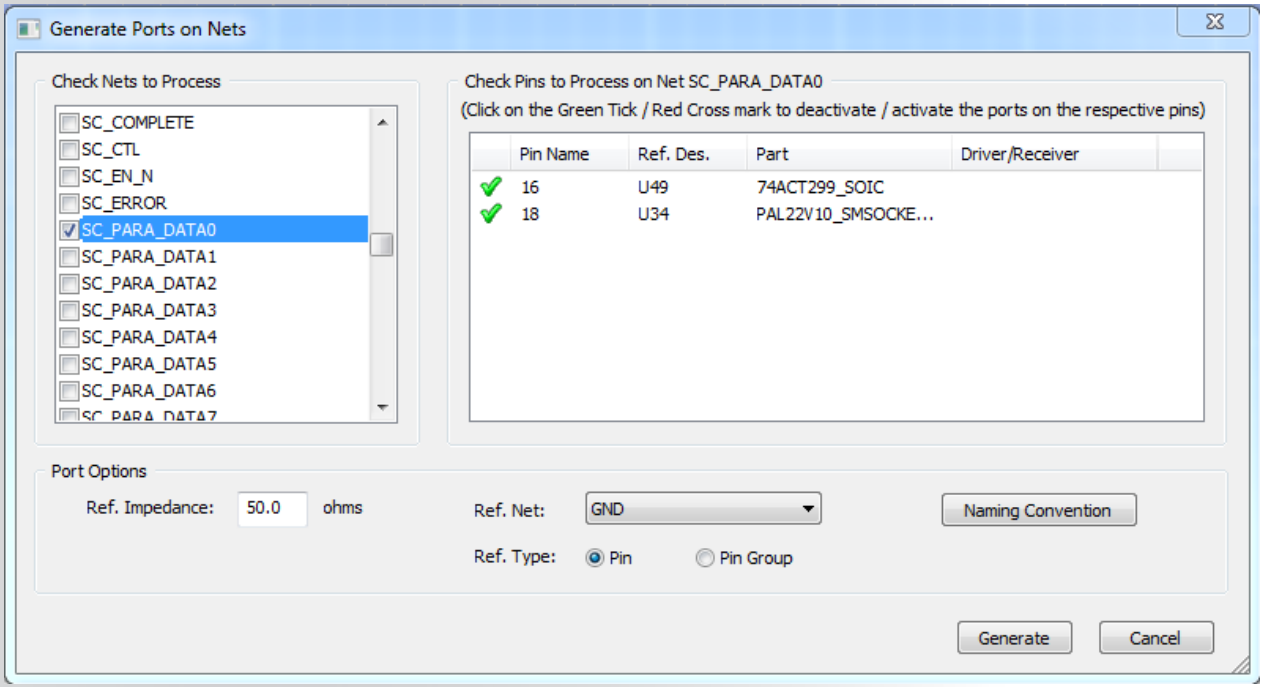


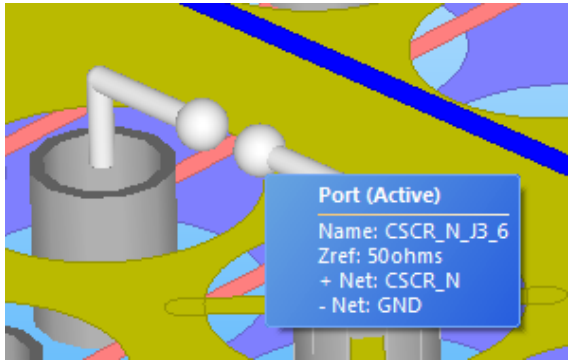
SIwave : Generate on selected net

- Generate the port on the selected net
  - Select the net(s)
  - Tools > Generate on Selected net…



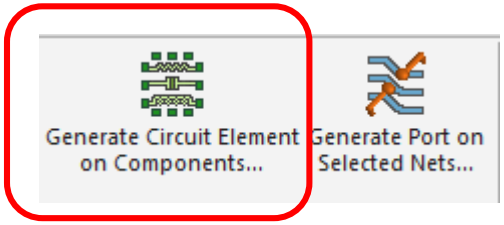


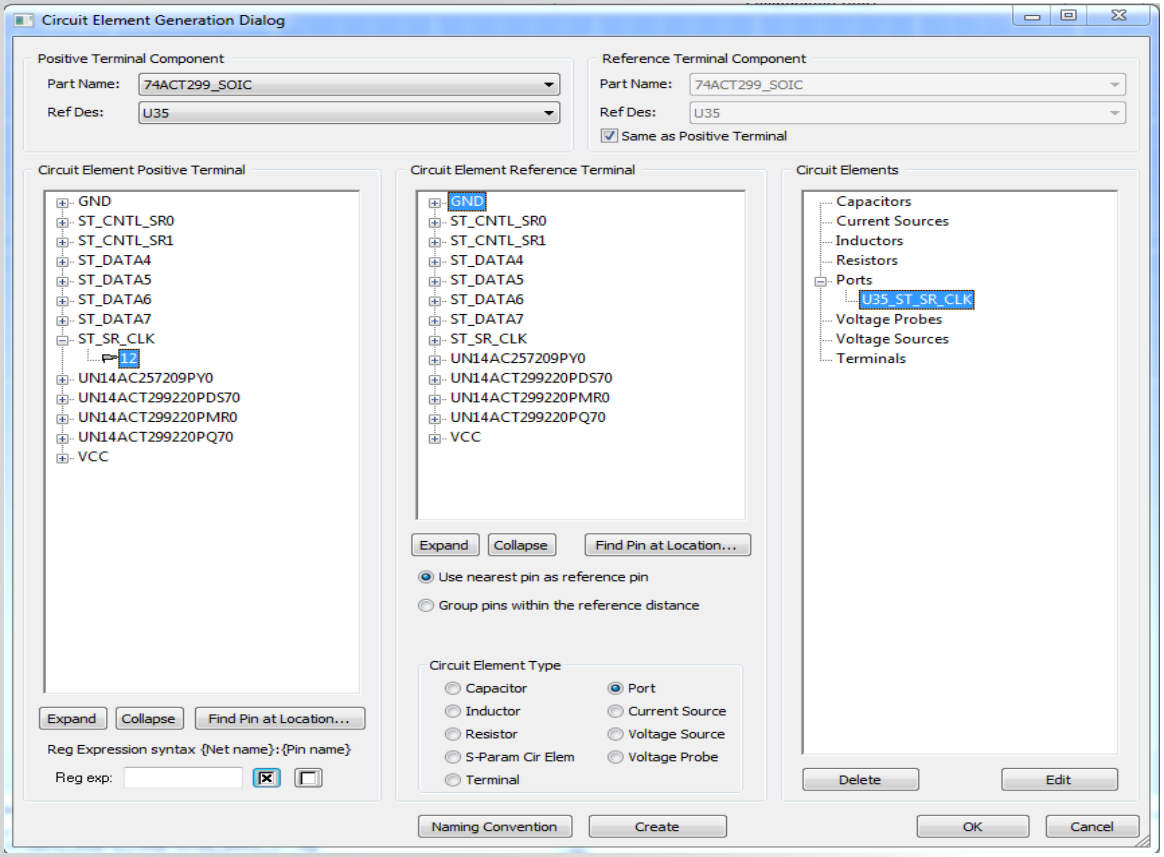


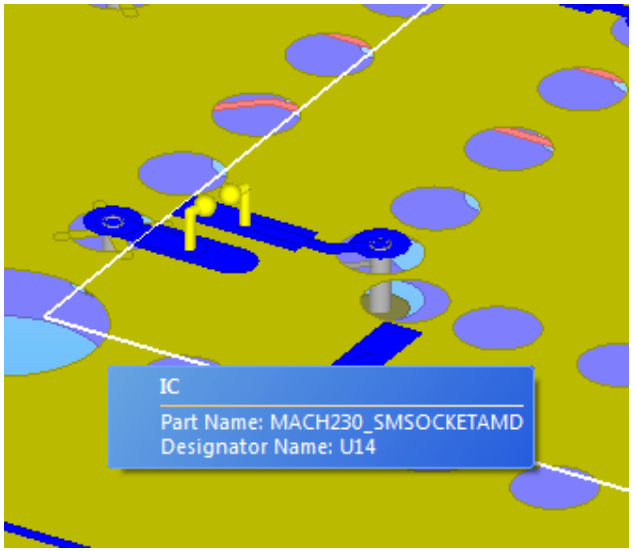


SIwave : Generate on Component

- Generate port on component
  - Select a component
  - Tools > Generate on Component…
  - Define Positive and Reference terminal

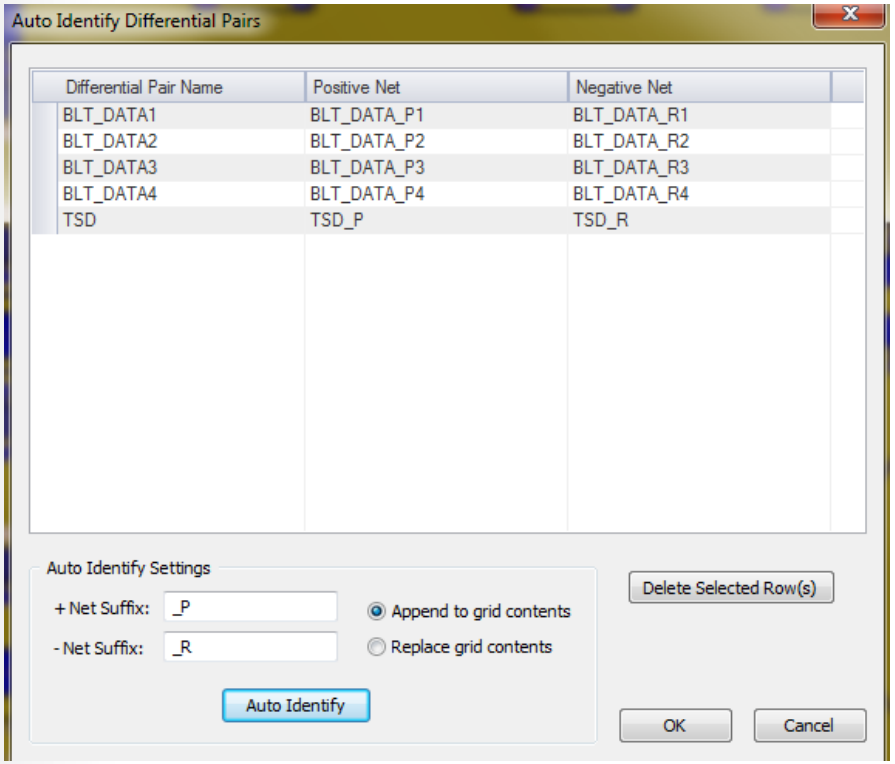






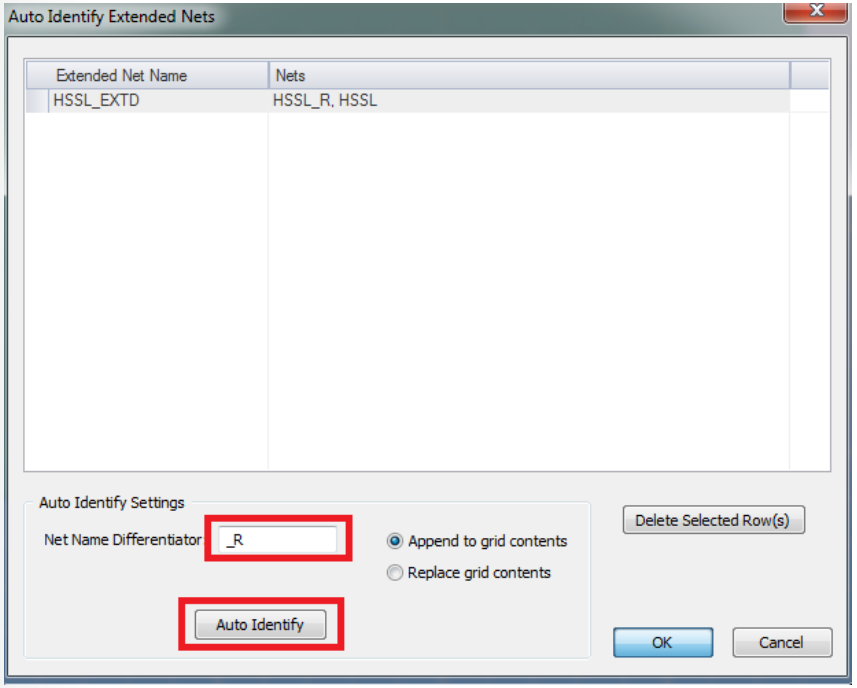
SIwave : Create Differential Pairs

- **Make sure that the Differential workspace is checked :**
  - Visibility > Workspaces > Differential Nets
- **This area allows you to define, search, sort and remove the differential pairs.**
- **An Auto Identify feature find differential pairs using the positive and neagtive net suffix.**
  - Define + & - net suffix
  - Auto Identify



SIwave : Create Extented Nets (E Net)

- **Make sure that the Enet workspace is checked :**
  - Visibility > Workspaces > Extended Net
- **This area allows you to define, search, sort and remove the Enets.** Most extended nets in real usage consist of only 2 nets with names like “**NET1**” and “**NET1_R**” connected by a resistor.
- **An Auto Identify feature find Extended net using a keyword (i.e. the net name differentiator) should be just “_R”**



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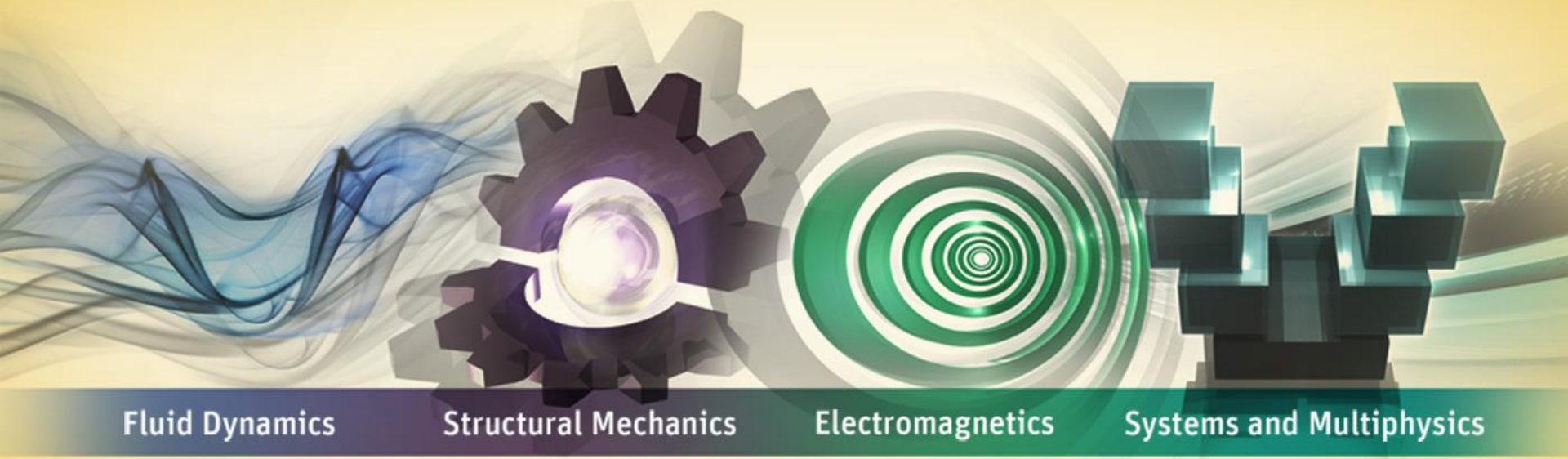
Classic questions about Port Settings



Classic questions about Port Settings

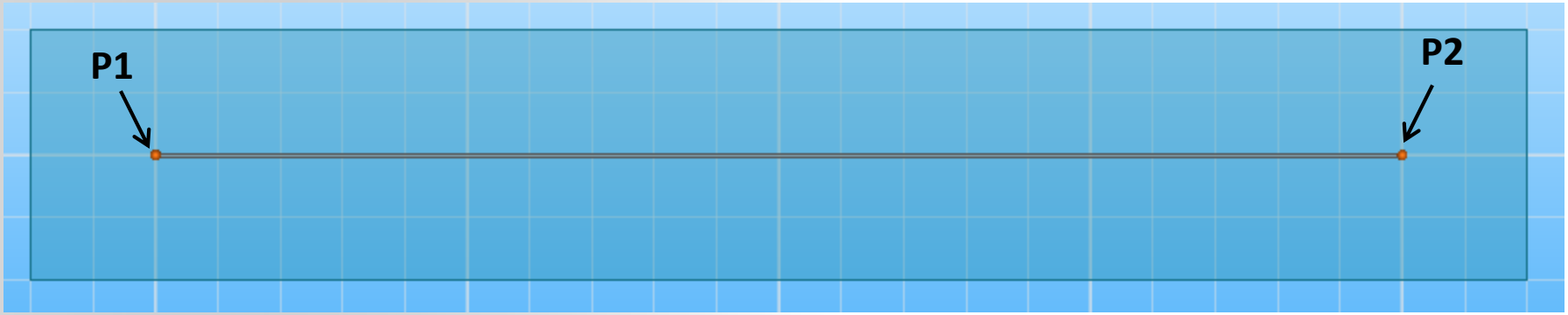
- What if a port in SIwave does not have a connection to a reference plane, but is connected between two signal locations? Does this invalidate the results?

- S-parameter models generally consist of ports referenced to ground.

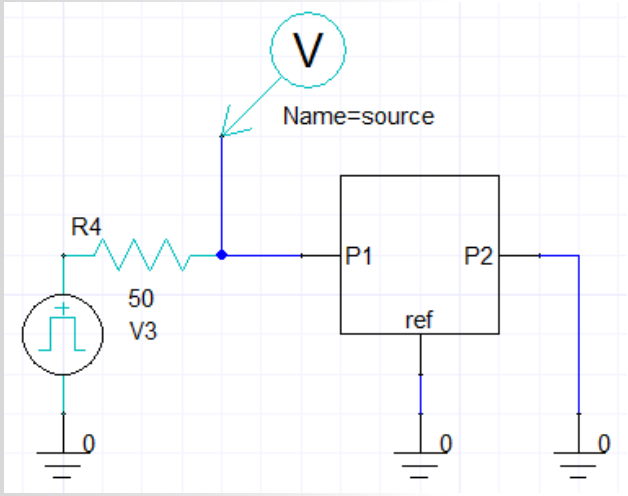
- In DesignerSI, the S-parameter symbol is often in is an “implied reference to ground” format.

A Simple Example

- Consider a 2-inch long trace over a reference plane.
  - Ports P1 and P2 between the trace and plane at each end

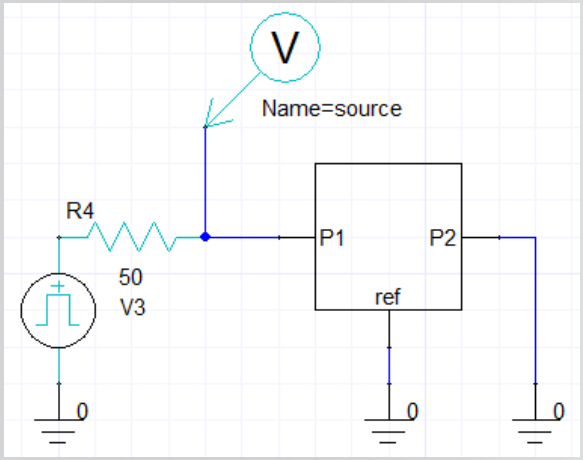


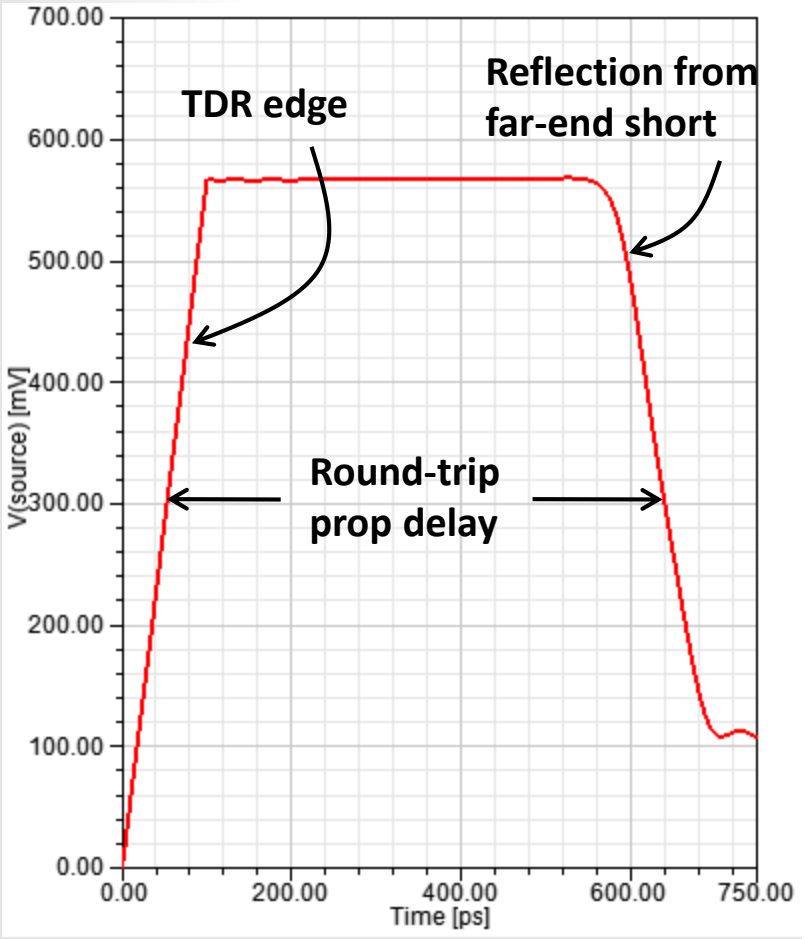
- Model in AEDT, with a source at P1 and P2 shorted to ground:



TDR Results

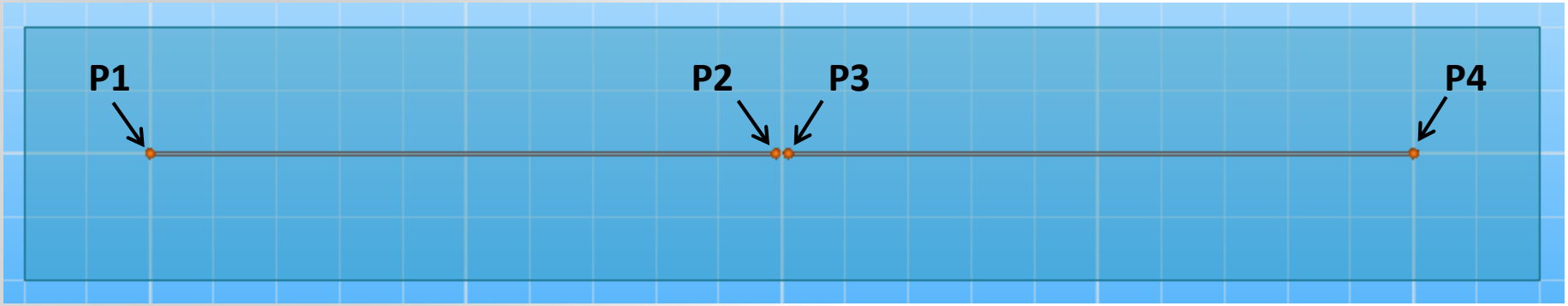
- **Source drives a 100ps edge**

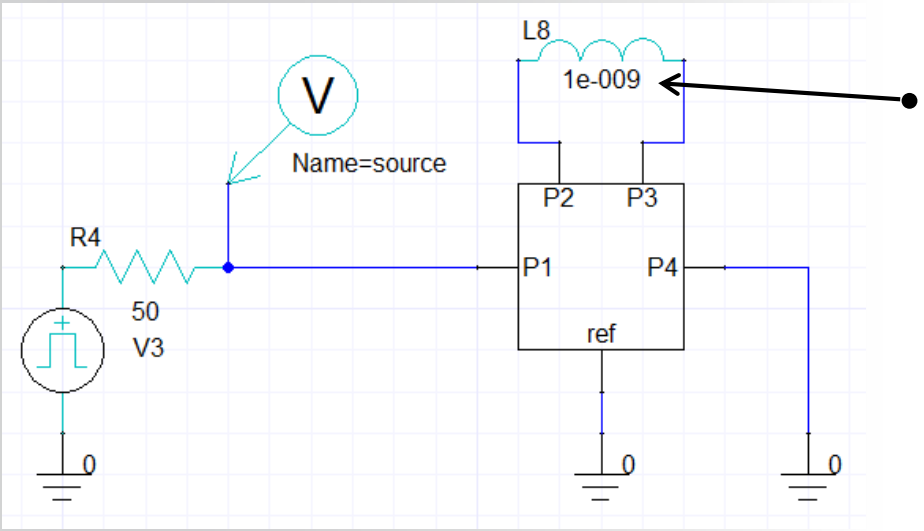




Now Split the Trace In Two…

- Now two traces of roughly 1 inch in length
- Ports to ground at all trace ends

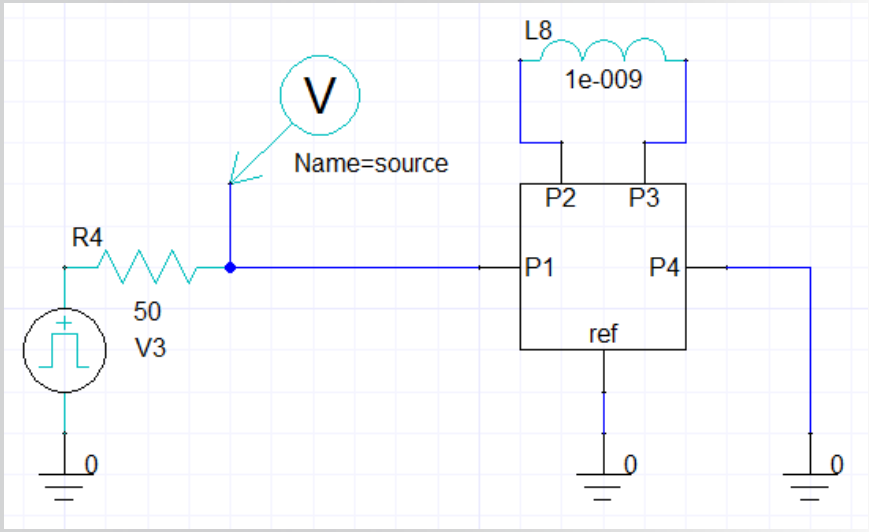


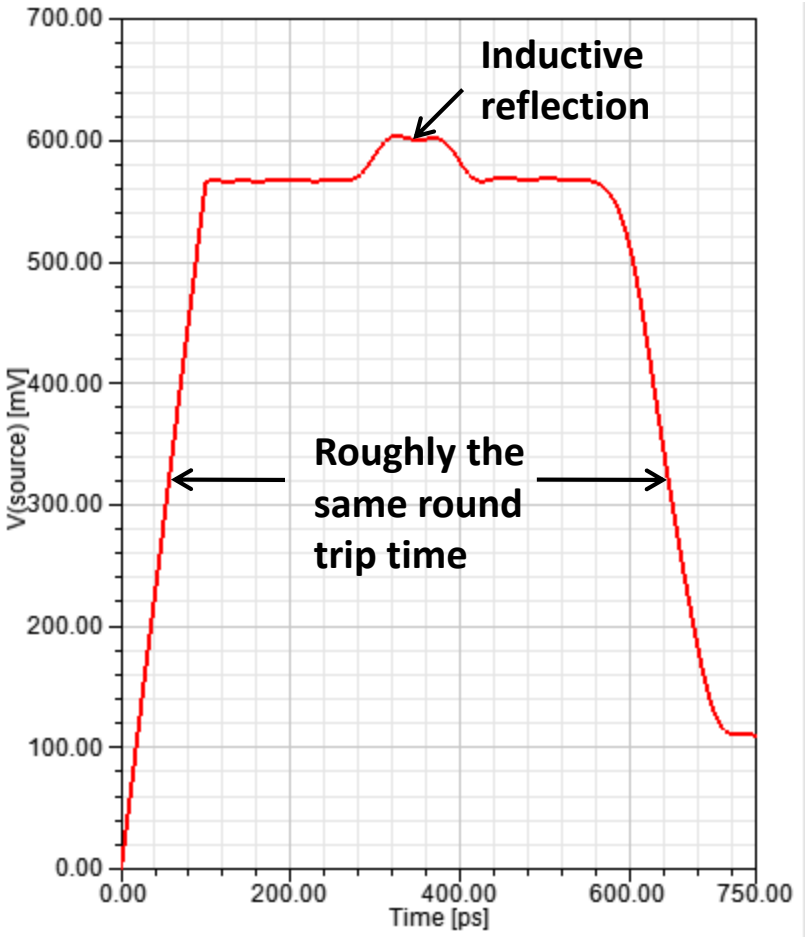


- Connect a series inductor between P2 and P3

Series Inductor Results

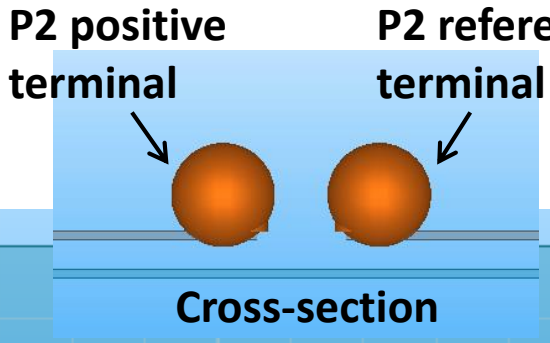
- Inductor causes small positive reflection in the middle of the waveform
- Results still perfectly intuitive

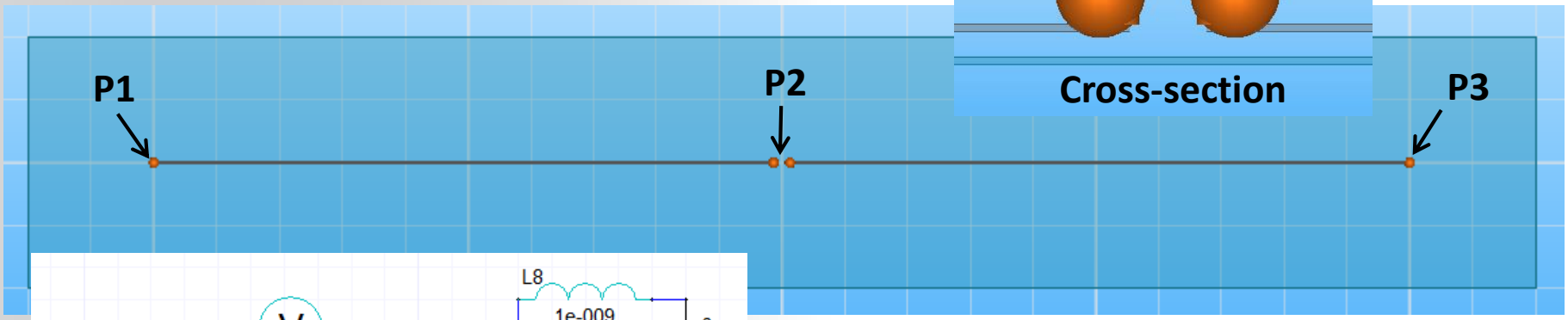


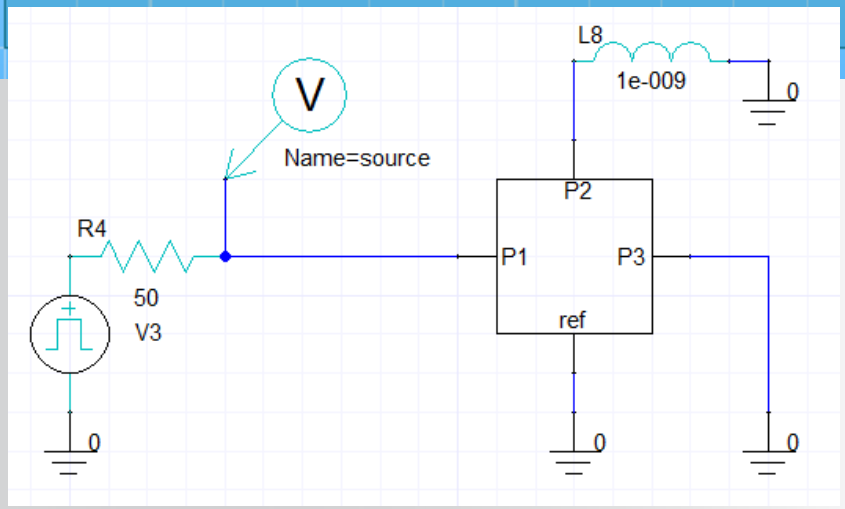


Now Place Just One Port In the Middle

- Same pair of 1-inch traces, but now place a single port P2 across the gap between them.
  - No connection to reference plane at P2





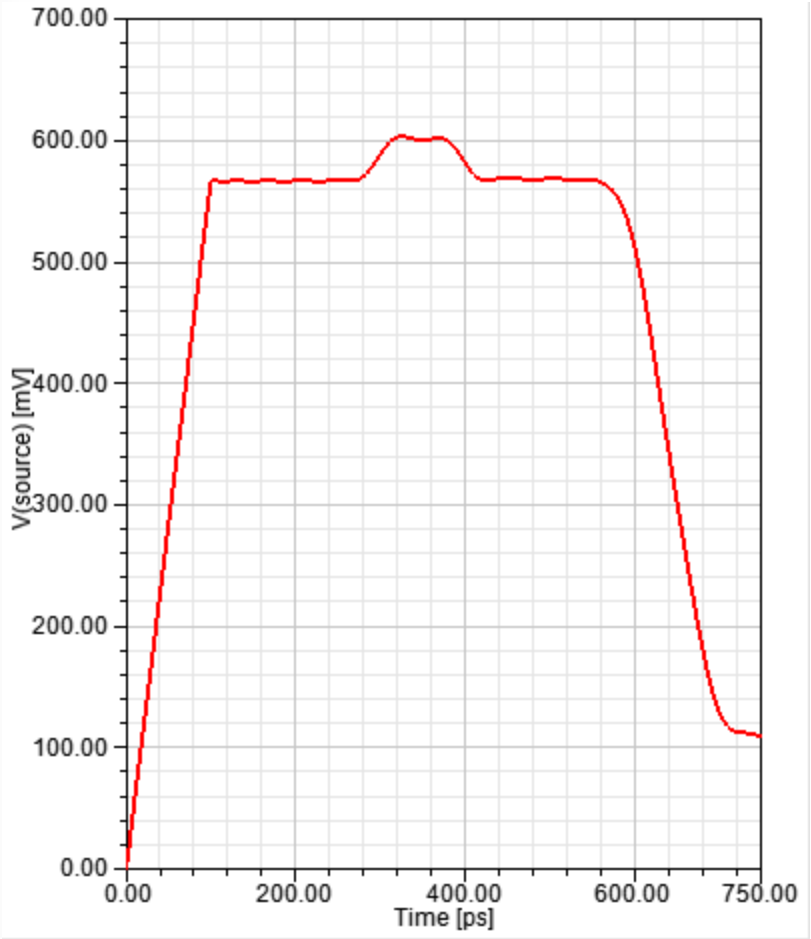


In the circuit schematic, we only have one pin. How do we connect the series inductor?

If we connect it between the P2 terminal and circuit ground, will that short out the second trace?

No. Results Are The Same

- Voltage between node P2 and circuit ground corresponds to voltage across the positive and reference terminals of the SIwave port
- Circuit ground and physical reference plane are completely different things



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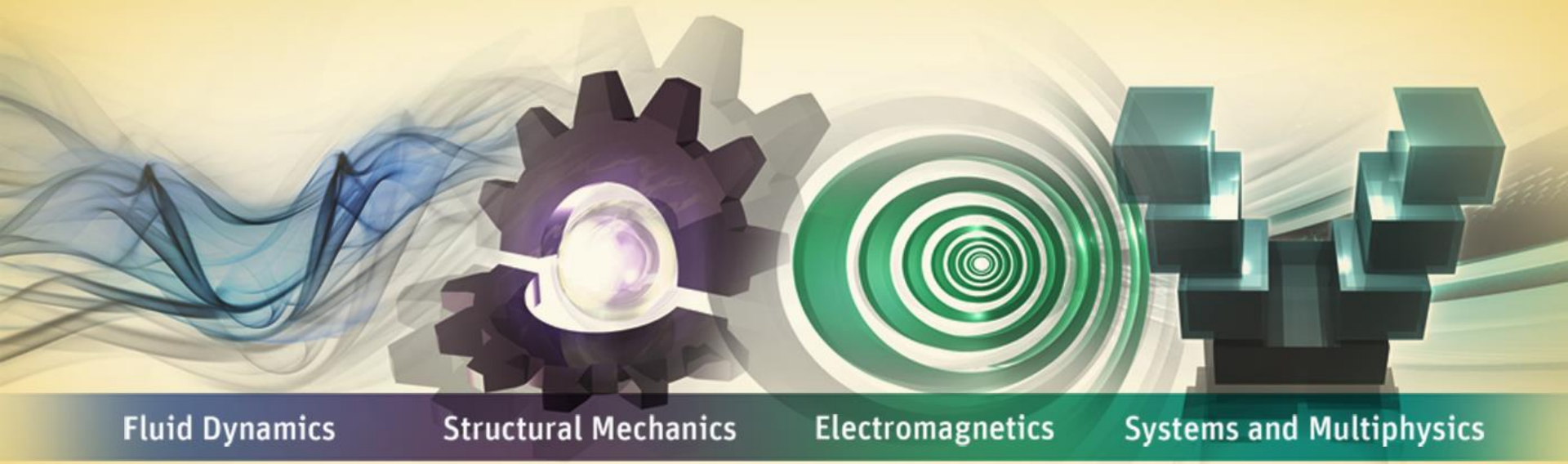
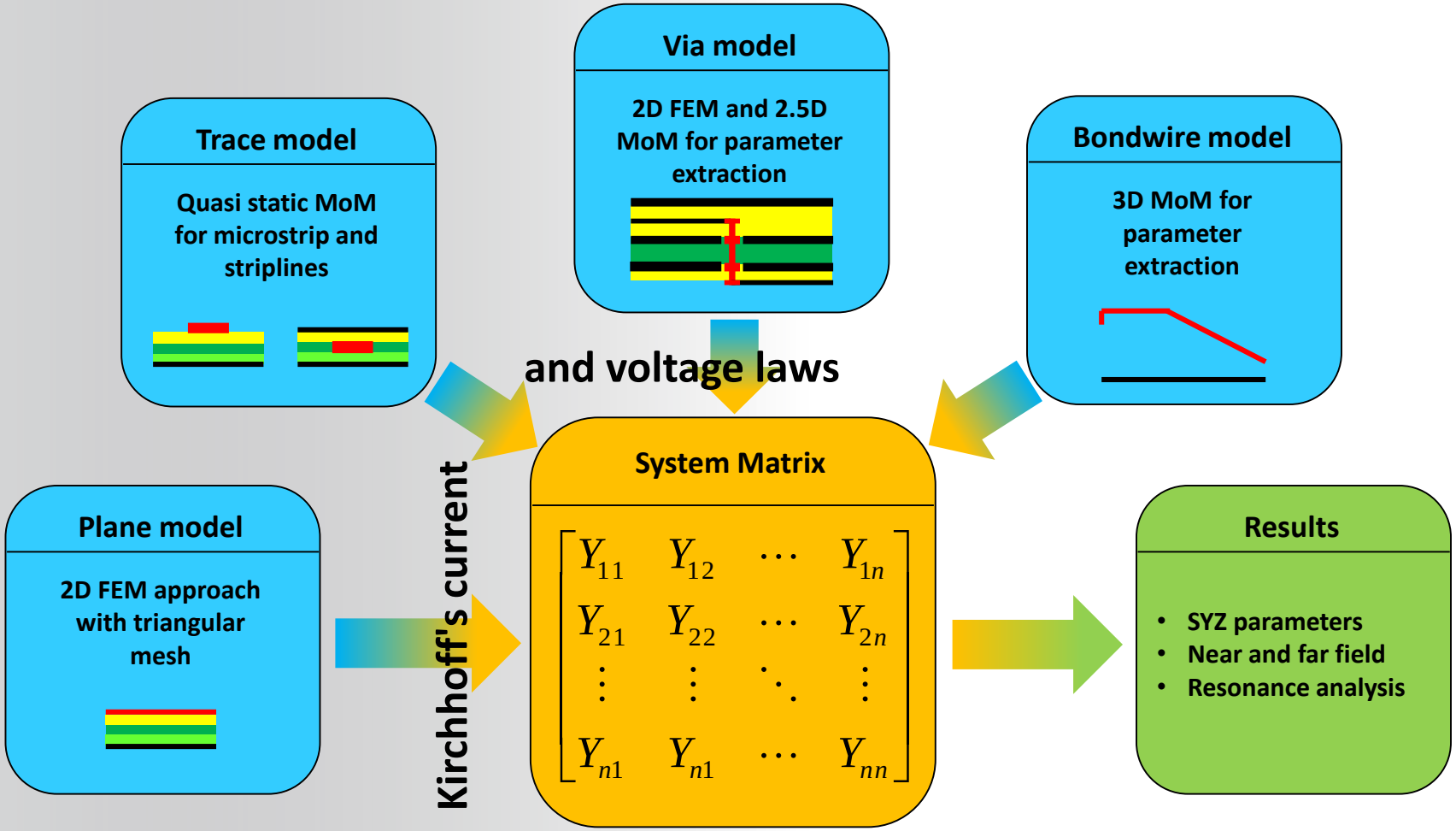
SIwave Solvers



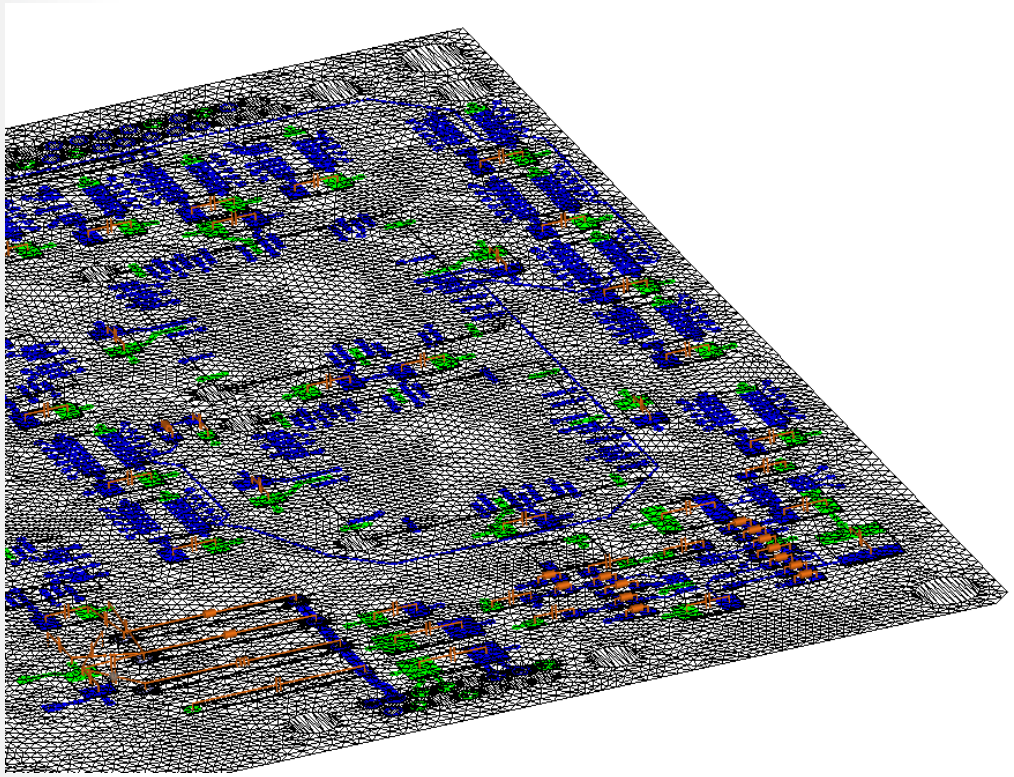
SIwave Solver Technology

SIwave solver components:



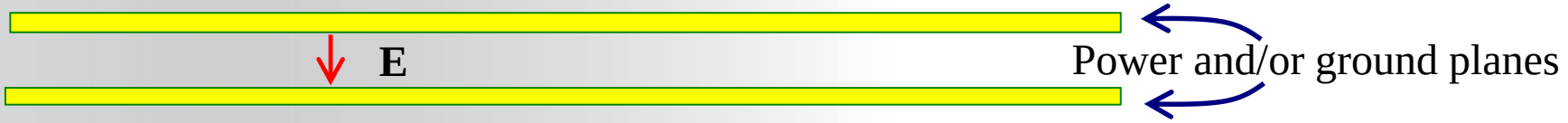
Plane Handling

Same FEM technology as HFSS, but for layered structures, i.e. 2D non-uniform mesh



$$\mathbf{E} = \hat{\mathbf{z}} E_z(x, y)$$

$$\mathbf{H} = \hat{\mathbf{x}} H_x(x, y) + \hat{\mathbf{y}} H_y(x, y)$$



2D restriction offers a major speed and memory advantage

Separation between the metal planes is much less than the wavelength

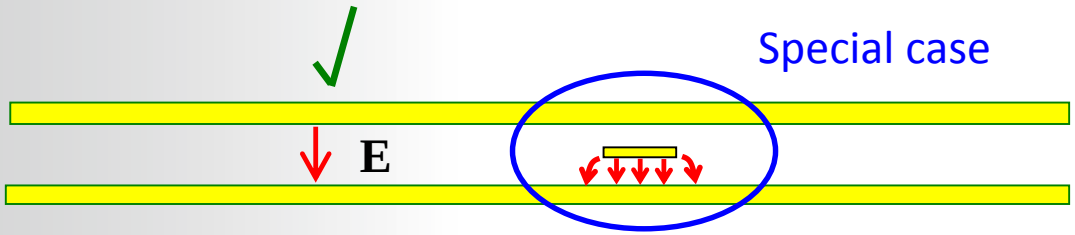
2-D Full-wave FEM continued

- **The Maxwell's equations can be reduced to a wave equation in terms of the voltage difference between planes.**

$$\frac{1}{R+j\omega L}\nabla^2 V(x,y)-(G+j\omega C)V(x,y)=I$$

- **The pre-processor identifies where the assumption is valid**

$$\mathbf{E}=\hat{\mathbf{z}}E_z(x,y)$$



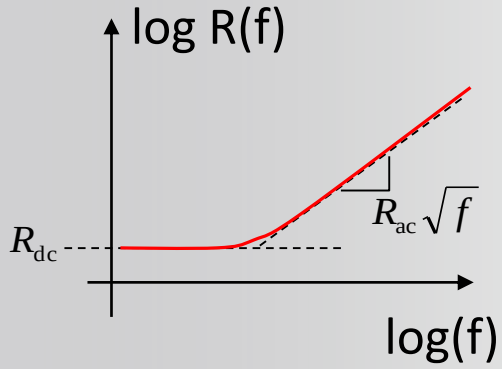
SIwave - Hybrid Solver

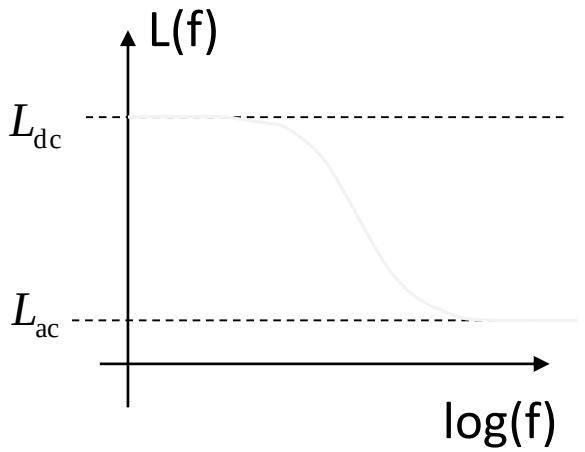
SIwave is a Hybrid Solver

- The pre-processor validates the layout, identifies and categorizes structures, assembles matrix and passes to sparse matrix solver.
- When is $\mathbf{E} = \hat{\mathbf{z}} E_z(x, y)$ not valid?
  - Traces
  - Trace-plane coupling
  - Via transitions
  - Plane edges
  - Bondwires, balls, bumps
  - Coaxial probes

Correct Handling of All Plane Effects and Dielectric Losses

Frequency-dependent plane impedance





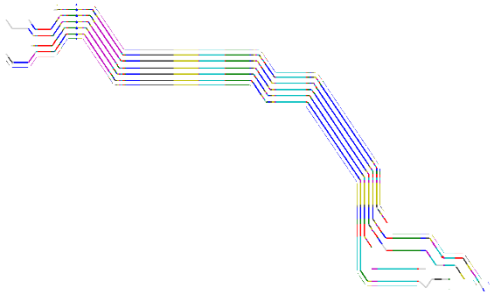
Correct Handling of Dielectric Losses

- Loss tangent and permittivity vary with frequency in a coordinated way
- Djordjević-Sarkar model
  - Satisfies causality laws -> physically realistic behavior

MoM Modeling of Traces

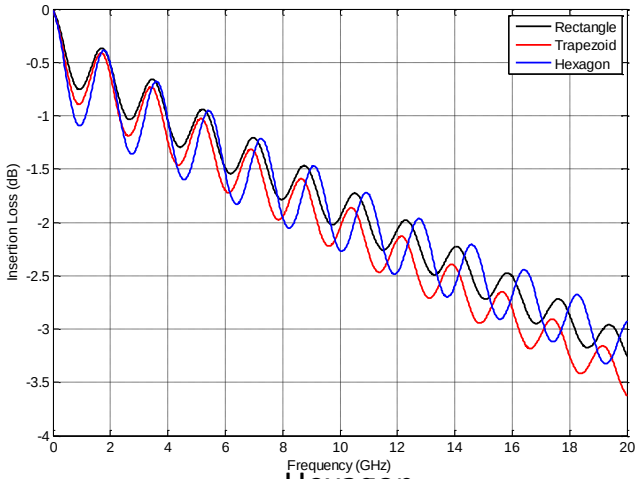
2D MoM RLCG trace extraction

- **Generalized multilayer extraction**
  - **Transmission lines**
  - **CPW**
  - **Split planes**
- **Non-uniform material stackups**
- **Trapezoidal and hexagonal cross-sections**
- **High accuracy and speed**
  - **Adaptive meshing of the trace cross-sections**
  - **Fast frequency sweep acceleration**
- **Multithreaded solve capability with perfect scaling**
- **Automatic coupling based on dB threshold**



SIwave Modeling of Traces

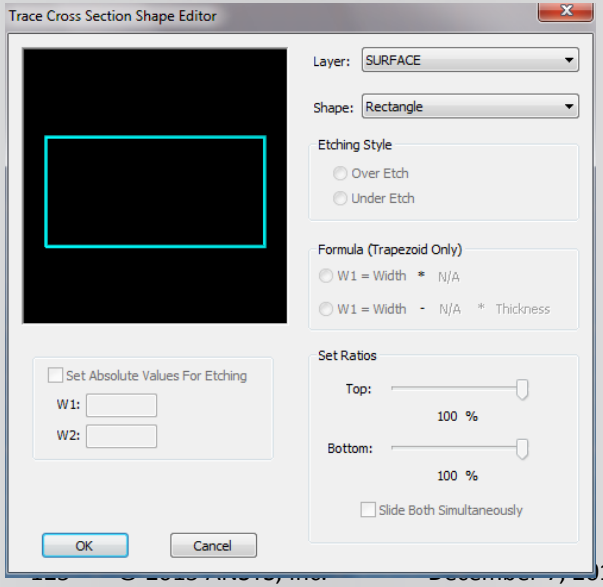
- **Define Trace Cross Section by choosing the appropriate shape by layer:**
  - Rectangular, Trapezoidal and hexagonal
- **Edit > Trace Cross Section…**

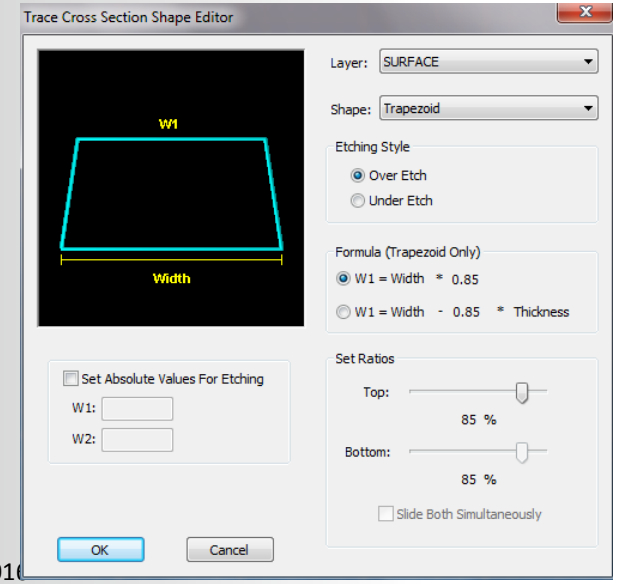


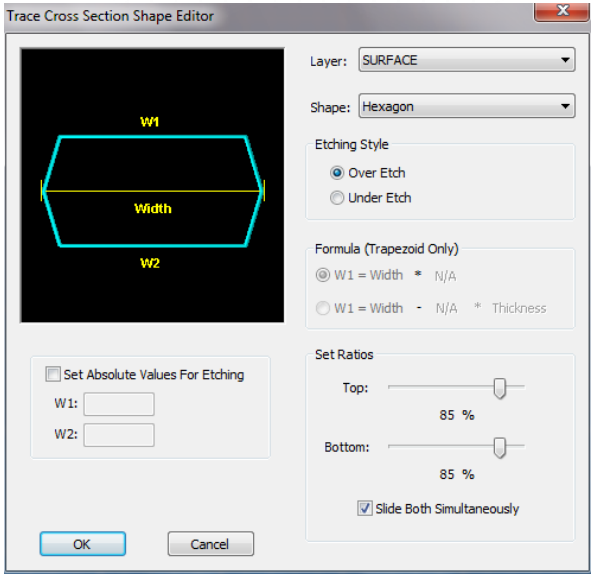
Rectangle

Trapezoid

Hexagon







Additional Solver Capabilities…

Vias

- Quasi-static FEM. Recognize repeated structures and solve only once.

Plane edges: edge-edge coupling

- 2D-MoM. Similar to transmission line modeling

Plane edge to trace coupling

- 2D-MoM

Low frequency plane-plane coupling

Passive components (RLC or s-parameters)

Bondwires & Balls and bumps

- Fast quasi-static 3D MoM (or Boundary Element Method)

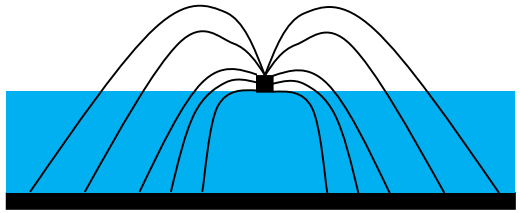
Efficient, accurate full-wave analysis of complex PCB‘s is possible due to

- Sophisticated „pre-processing“ that properly recognizes and categorizes 3D features.
- Multiple EM solvers working in combination.
- Advanced Numerics (Matrix solver)

SIwave Solver Components

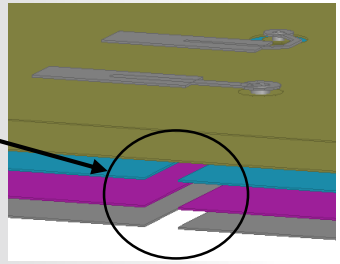
Further models for improved accuracy:

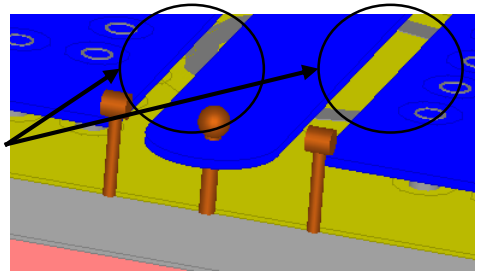
- **Fringe fields: correction for thin planes (very critical for inductance!).**



- **Smart coupling detection: coupling between traces/plane edges and via coupling.**

- **Coplanes, split planes and thin planes: plane – plane and trace plane coupling.**



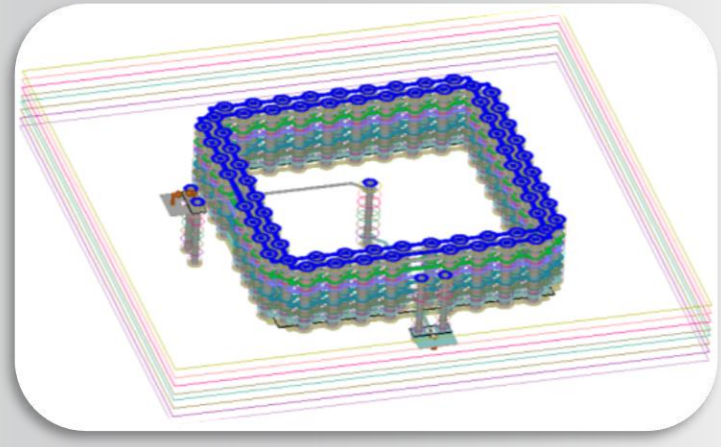


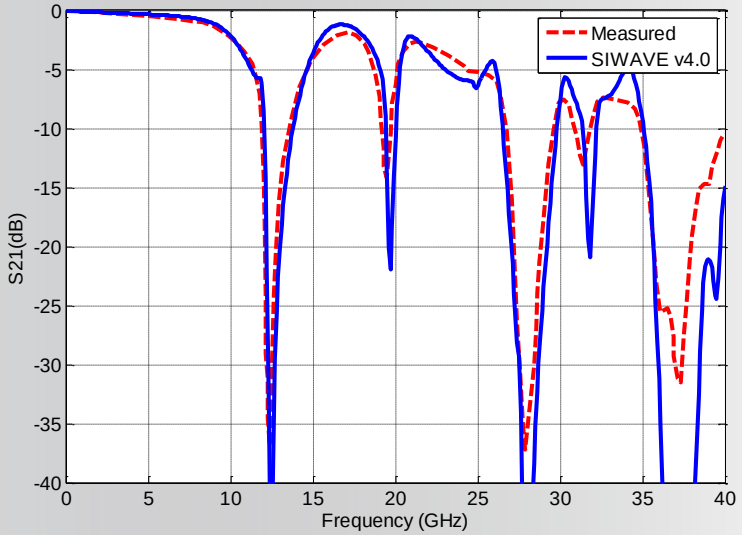
SIwave - Via Modeling

New VIA library - IBM Benchmark Examples

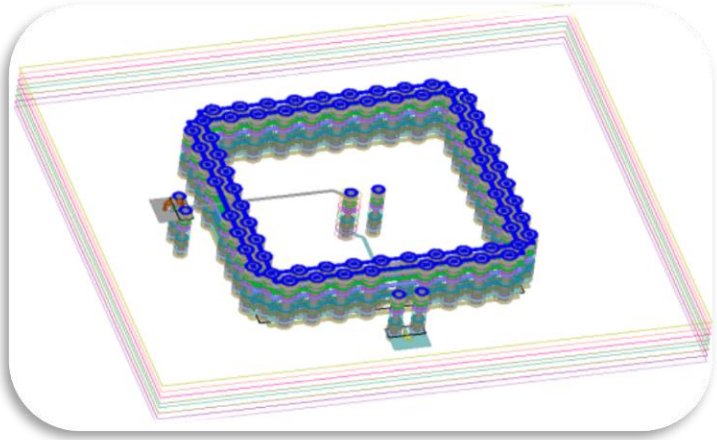
Taken From: Selli, G., et al, "Developing a 'Physical' Model for Vias," DesignCon 2007

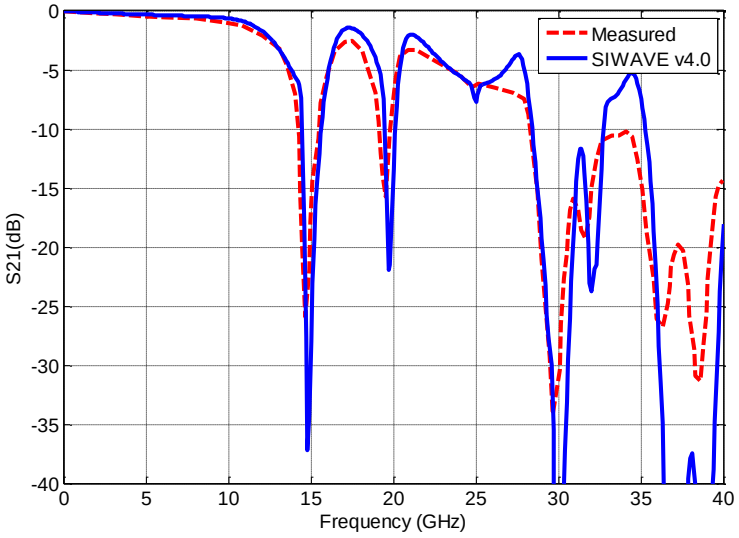
Single Through Via





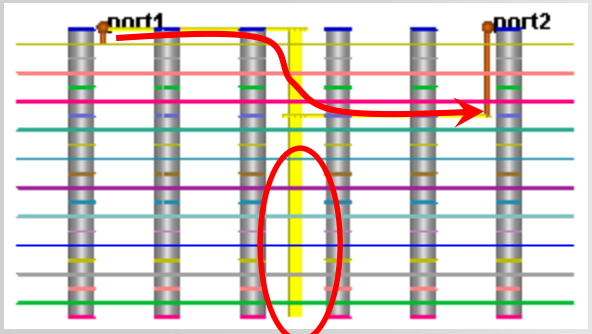
Single Through Via + Ground Via

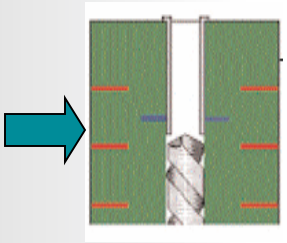


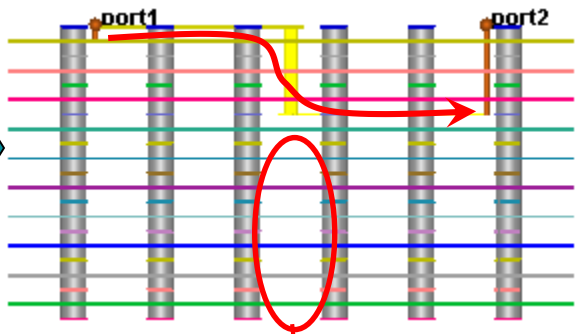


High-Speed Memory System
Design Issues : Via Stub effect

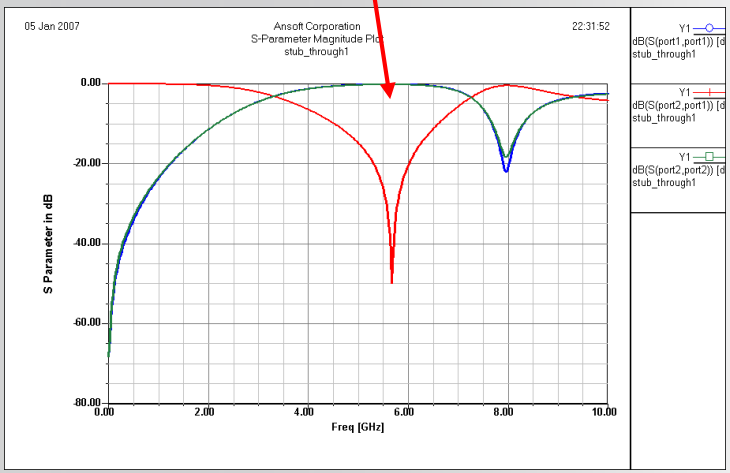
- **Board level - Via Stub effect**

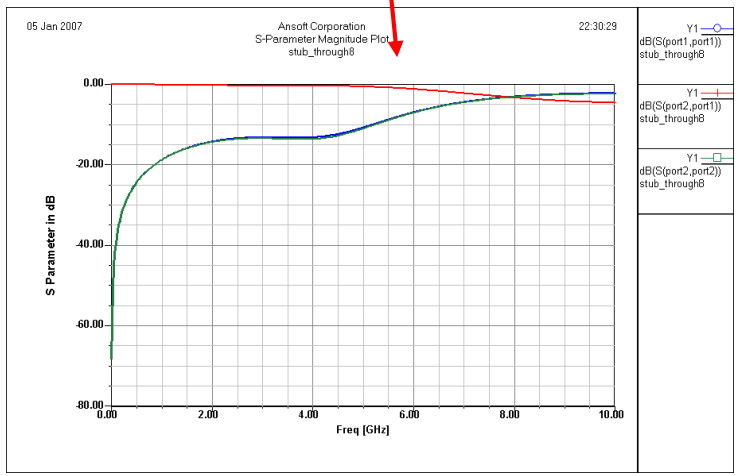






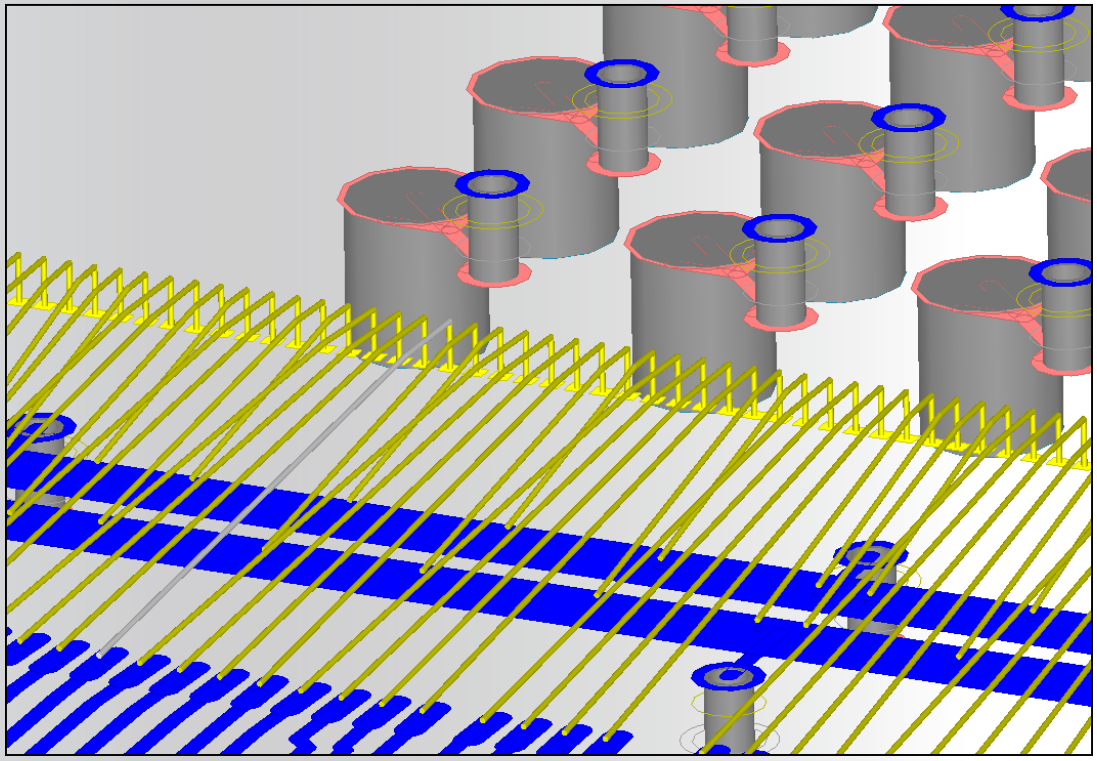
Via Stub Effect

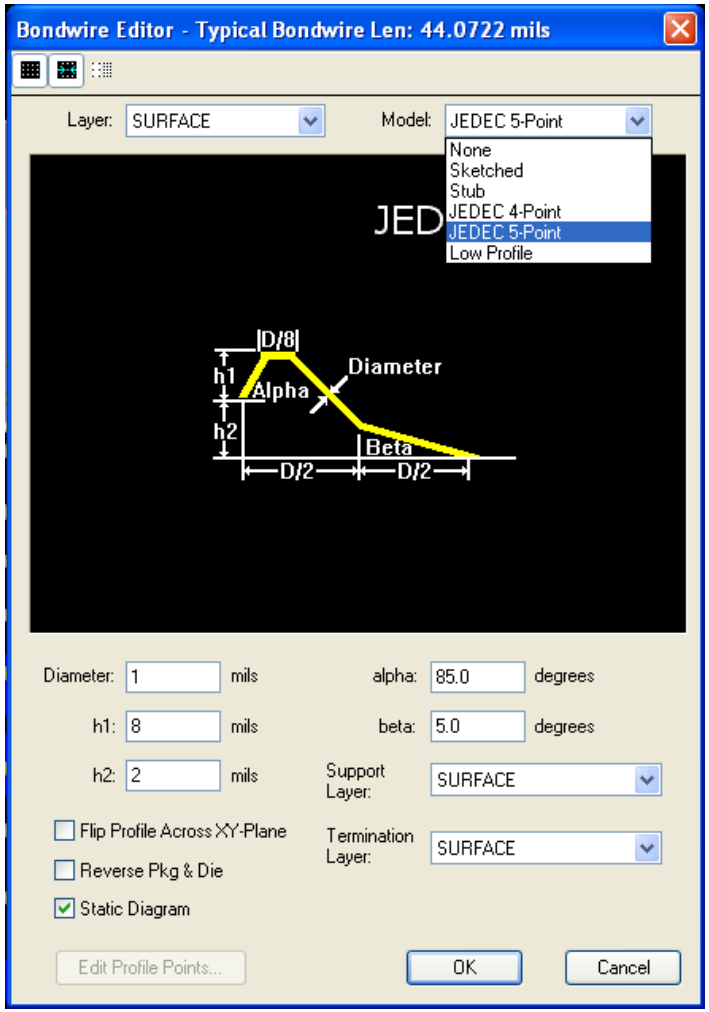




Bondwires

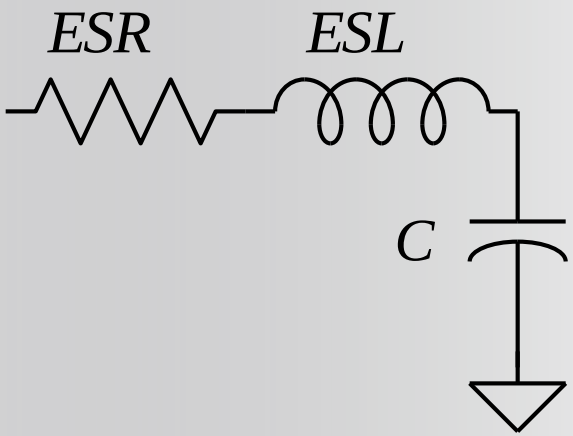
A 3D method of moments solver is used to extract the RLC parasitics, including self and mutual terms



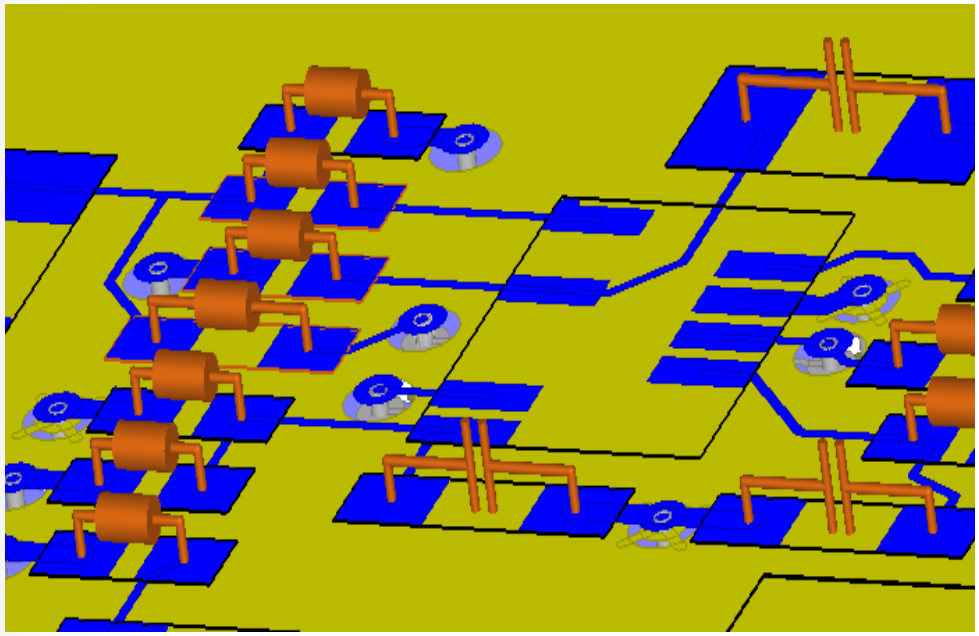


Passive Components

- RLC components can be modeled as:
  - Lumped Element
  - Touchstone file



Ferrites included as a Touchstone model



Component attachment accurately modeled from pad dimensions

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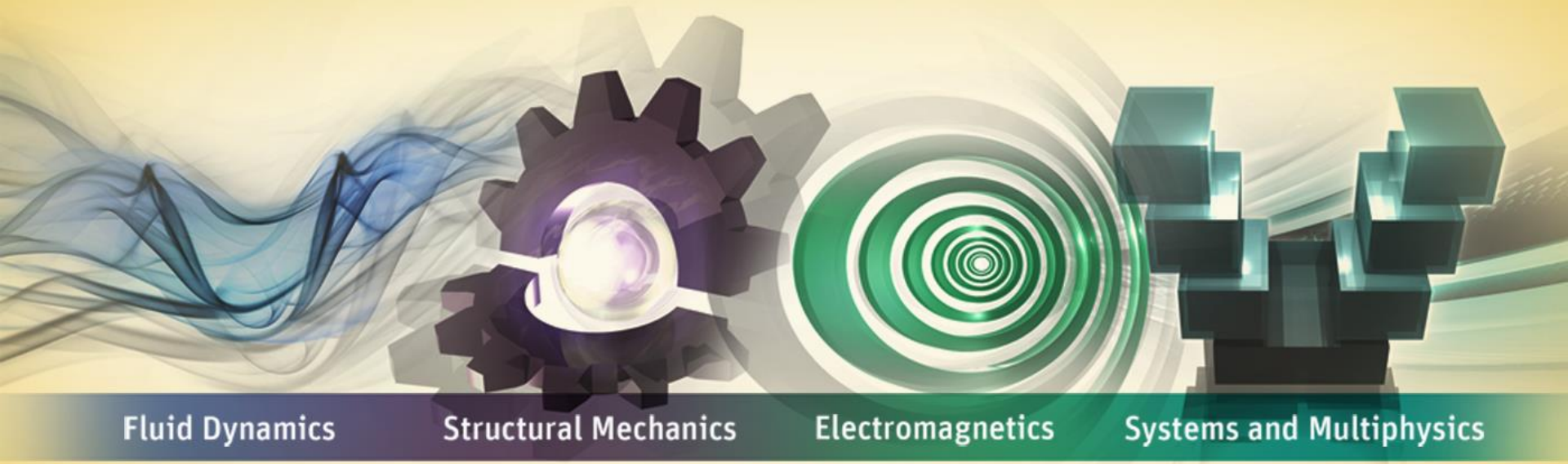
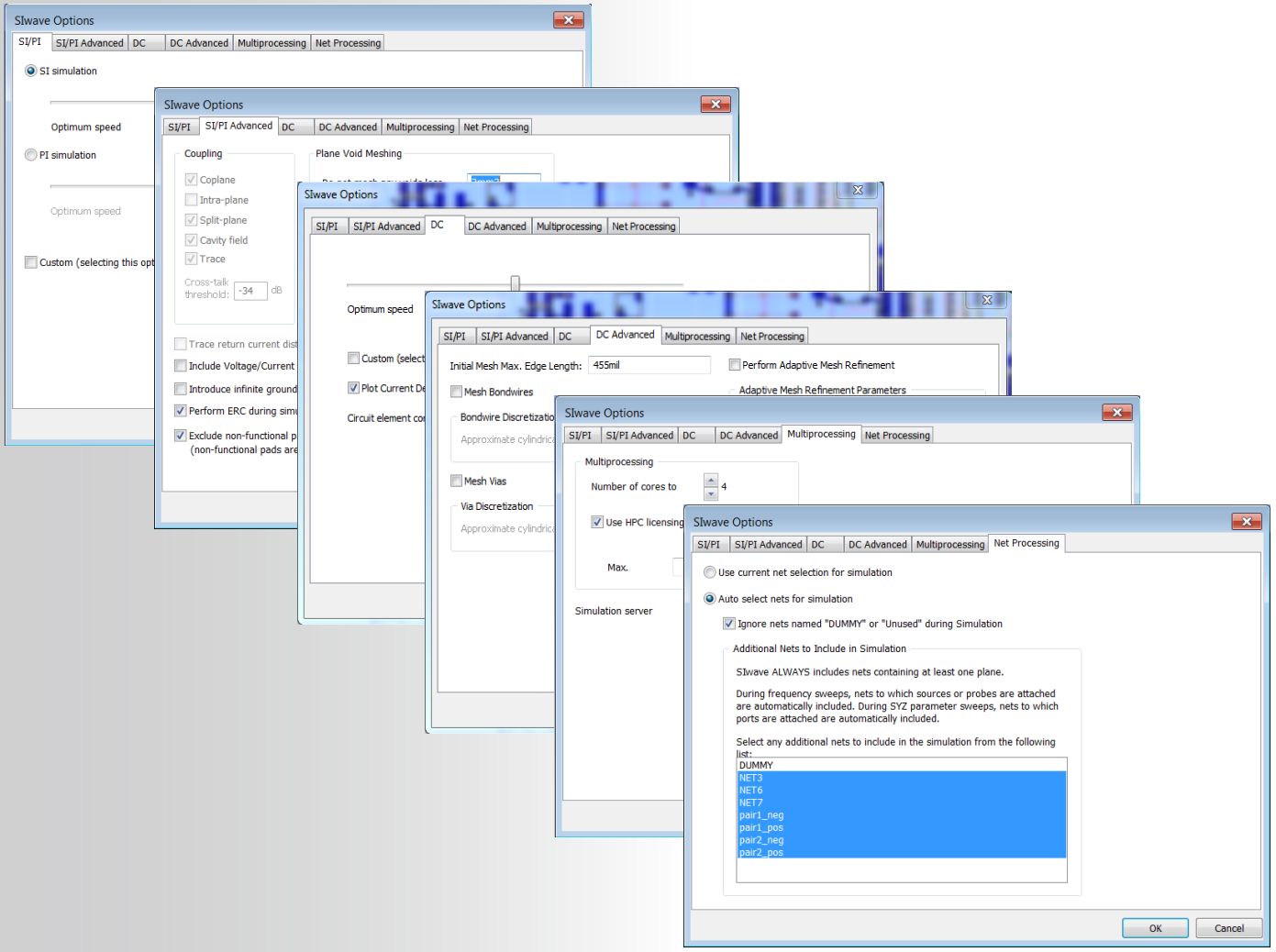
Simulation Options



Global Simulation Options

Simulations > Options…

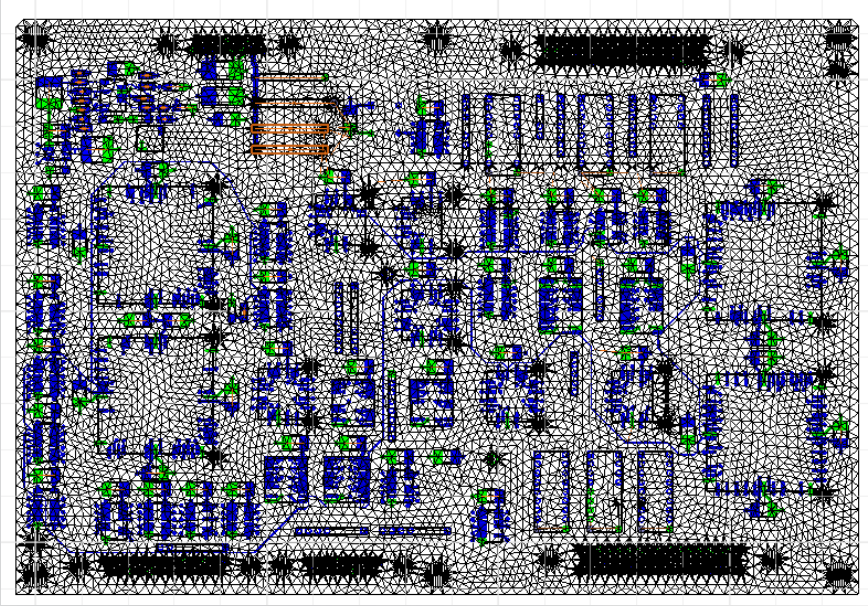


SIwave - Mesh

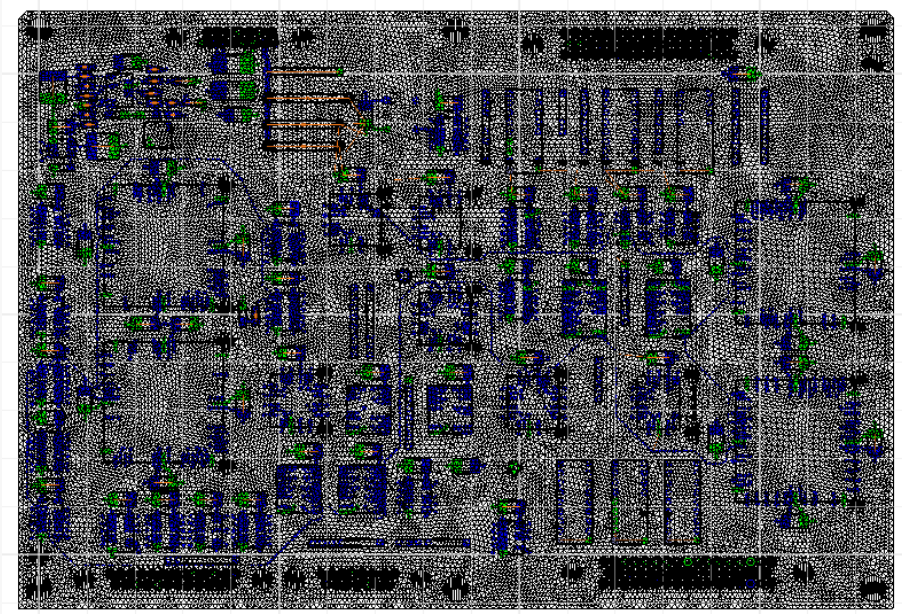
Use FEM Discretization

Mesh Refinement. This parameter controls how the finite element mesh used in SIwave is generated. You can select from the following options:

- **Automatic:** This options automatically picks the suitable mesh refinement frequency. It is dependent on the drawing size, the number of modes, and/or the maximum sweep frequency. This is the recommended option.
- **Frequency:** This option lets you control the mesh size and is based on the effective wavelength of the specified frequency.



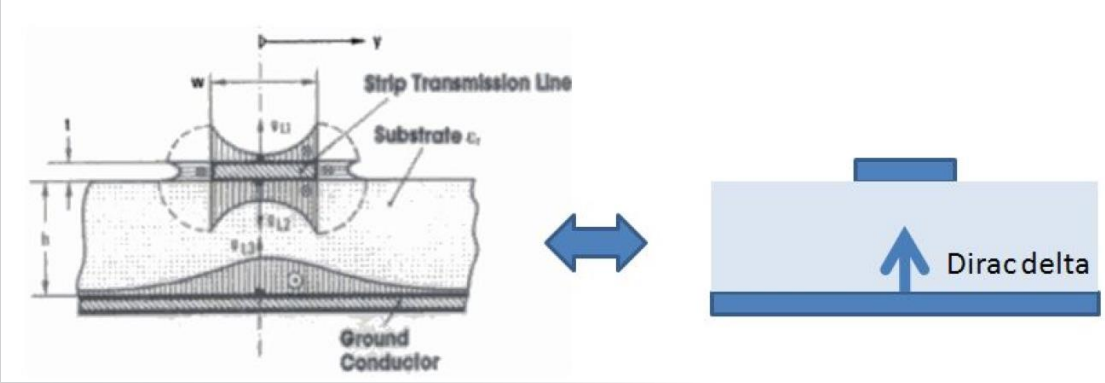
Frequency = 5GHz



Automatic : Fmax = 10GHz

3D return current distribution

- **3D return current distribution check box if you want to accurately model the change of the characteristic impedance of transmission lines caused by a discontinuous ground plane. Instead of injecting the return current of a trace into a single point on the ground plane, the return current for a high impedance trace is now spread out.**



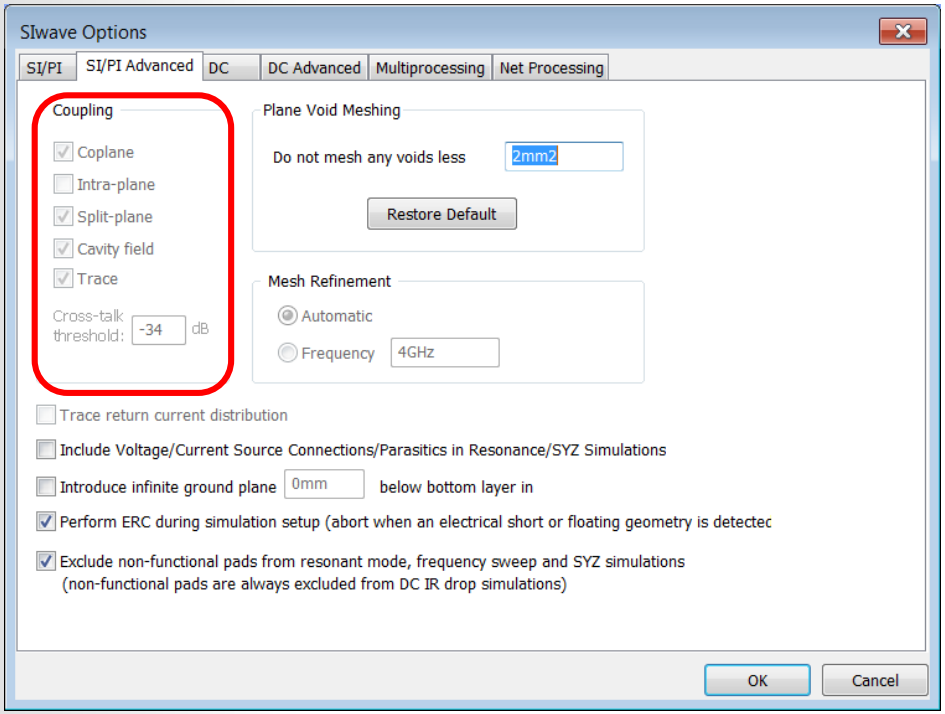
- **The trace return current is not distributed when all traces attached to a node have a characteristic impedance of less than 75 ohms, or if the difference between two connected traces is less than 25 ohms.**
  - Not really necessary for PI relatedsimulations.
  - For SI analysis it is quite useful and improves accuracy.
  - Slow down the simulation noticeably. RAM is slightly increase by more matrix entries and some other overhead.

Coupling Options in SIwave

Solver Coupling Options

- By default, all coupling options are disabled. Please check the box Custom in the SI/PI tab to enable them.

- Co-Plane
- Intra-Plane
- Split-Plane
- Cavity Field
- Trace

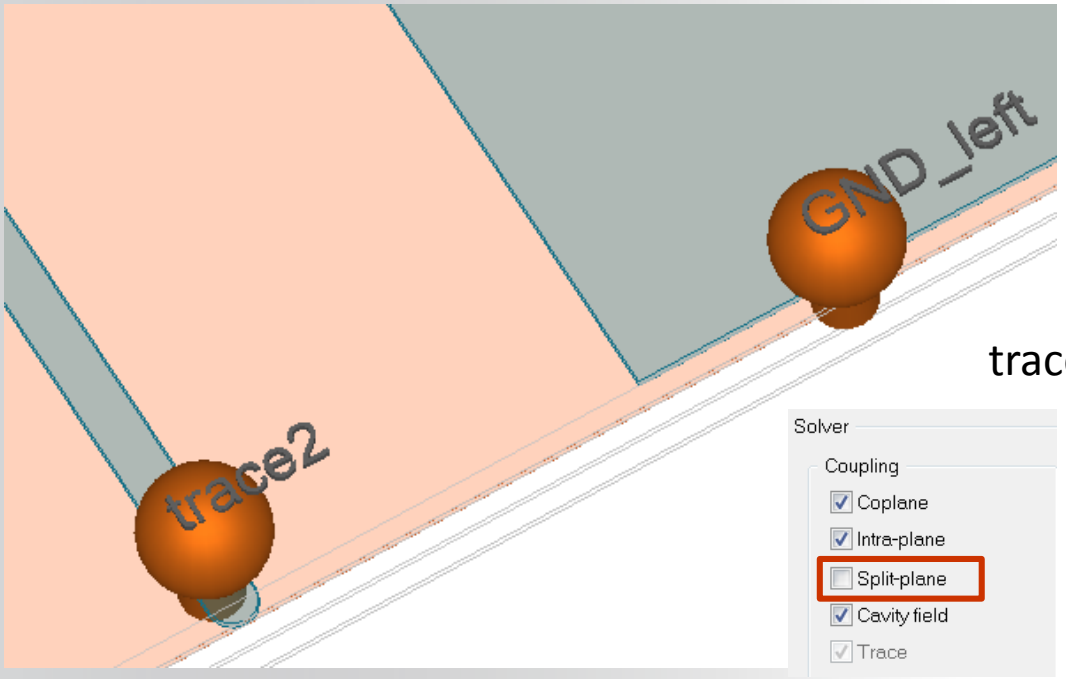


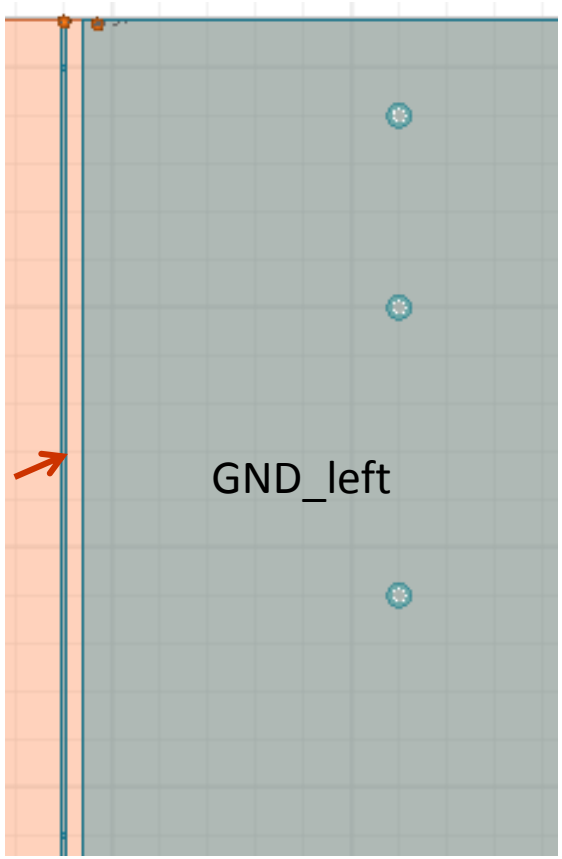
Case 1 – 1 trace, 1 plane

Coupling – Split Plane

With and without Split Plane Coupling

- With all the options enabled, SIwave calculates coupling between trace2 and GND_left
- When Split Plane is disabled there is no coupling between the two

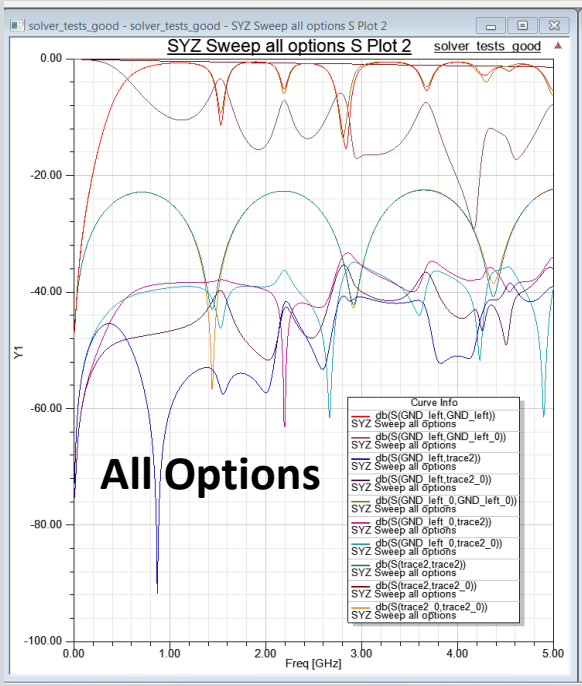


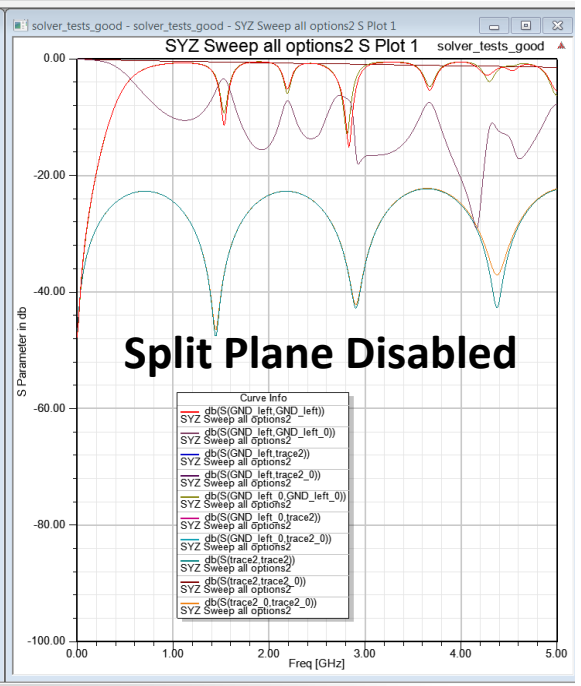


Coupling – Split Plane – Two Cases

With and without Split Plane Coupling

- With all the options enabled, SIwave calculates coupling between trace2 and GND_left
- When Split Plane is disabled there is no coupling between the trace2 and GND_left





	Freq [GHz]	db(S(GND_left,trace2)) SYZ Sweep all options
1	0.001000	-75.481569
2	0.010998	-71.617708
3	0.020996	-66.838655
4	0.030994	-63.441114
5	0.040992	-60.839158
6	0.050990	-58.749028
7	0.060988	-57.252107
8	0.070986	-55.991105
9	0.080984	-54.905827
10	0.090982	-53.956594
11	0.100980	-53.115906
12	0.110978	-52.363950
13	0.120976	-51.686013
14	0.130974	-51.070903
15	0.140972	-50.509937
16	0.150970	-49.996268
17	0.160968	-49.524424
18	0.170966	-49.089985
19	0.180964	-48.689342
20	0.190962	-48.319530
21	0.200960	-47.978098
22	0.210958	-47.663008
23	0.220956	-47.372560
24	0.230954	-47.105335
25	0.240952	-46.860149
26	0.250950	-46.636011
27	0.260948	-46.432098
28	0.270946	-46.247726
29	0.280944	-46.082332
30	0.290942	-45.935456
31	0.300940	-45.806722
32	0.310938	-45.695832
33	0.320936	-45.602548
34	0.330934	-45.526682
35	0.340932	-45.468092
36	0.350930	-45.426667
37	0.360928	-45.402320
38	0.370926	-45.394987
39	0.380924	-45.404614
40	0.390922	-45.431152
41	0.400920	-45.474556
42	0.410918	-45.534781
43	0.420916	-45.611773
44	0.430914	-45.705474
45	0.440912	-45.815817

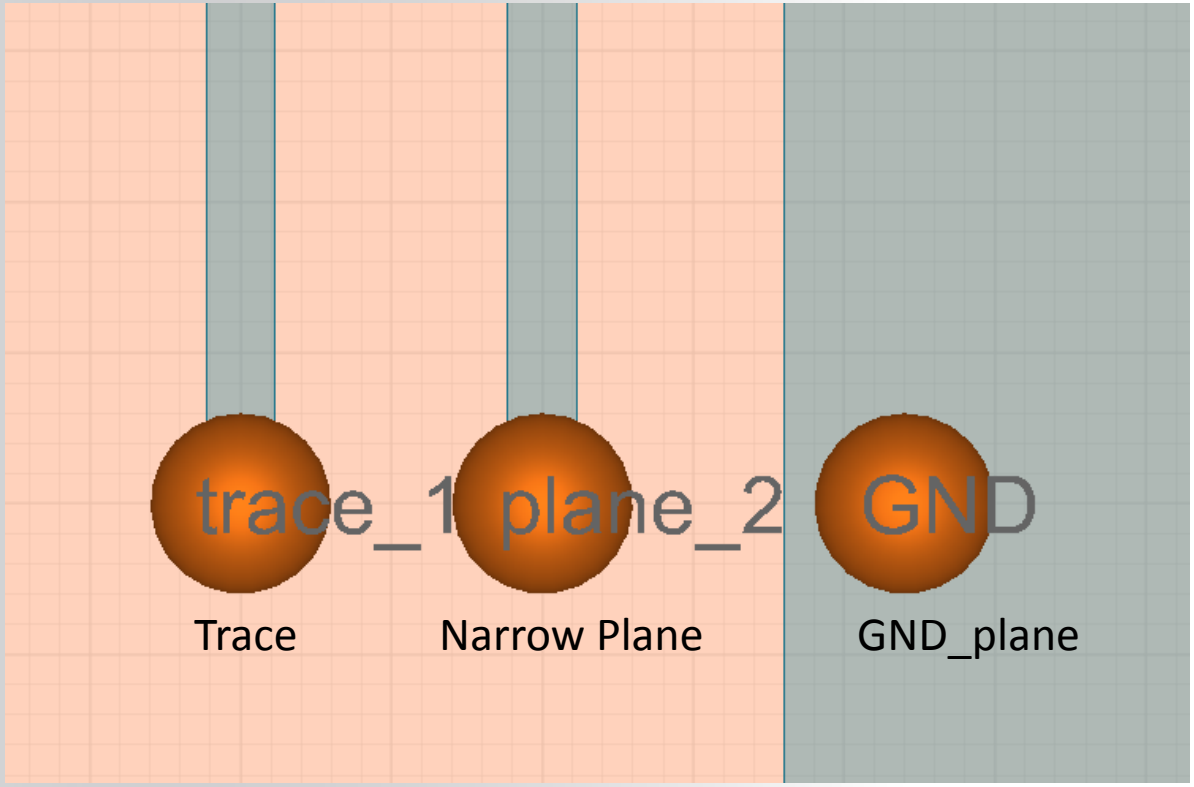
	Freq [GHz]	db(S(GND_left,trace2)) SYZ Sweep all options2
1	0.001000	-inf
2	0.010998	-inf
3	0.020996	-inf
4	0.030994	-inf
5	0.040992	-inf
6	0.050990	-inf
7	0.060988	-inf
8	0.070986	-inf
9	0.080984	-inf
10	0.090982	-inf
11	0.100980	-inf
12	0.110978	-inf
13	0.120976	-inf
14	0.130974	-inf
15	0.140972	-inf
16	0.150970	-inf
17	0.160968	-inf
18	0.170966	-inf
19	0.180964	-inf
20	0.190962	-inf
21	0.200960	-inf
22	0.210958	-inf
23	0.220956	-inf
24	0.230954	-inf
25	0.240952	-inf
26	0.250950	-inf
27	0.260948	-inf
28	0.270946	-inf
29	0.280944	-inf
30	0.290942	-inf
31	0.300940	-inf
32	0.310938	-inf
33	0.320936	-inf
34	0.330934	-inf
35	0.340932	-inf
36	0.350930	-inf
37	0.360928	-inf
38	0.370926	-inf
39	0.380924	-inf
40	0.390922	-inf
41	0.400920	-inf
42	0.410918	-inf
43	0.420916	-inf
44	0.430914	-inf
45	0.440912	-inf

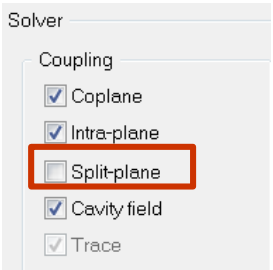
Case 2 – 1 trace, 2 planes

Coupling – Split Plane

With and without Split Plane Coupling

- With all the options enabled, SIwave calculates all coupling including coupling between narrow planes like plane_2 and traces like trace_1
- When Split Plane Coupling is disabled, there is no direct coupling between trace_1 and plane_2

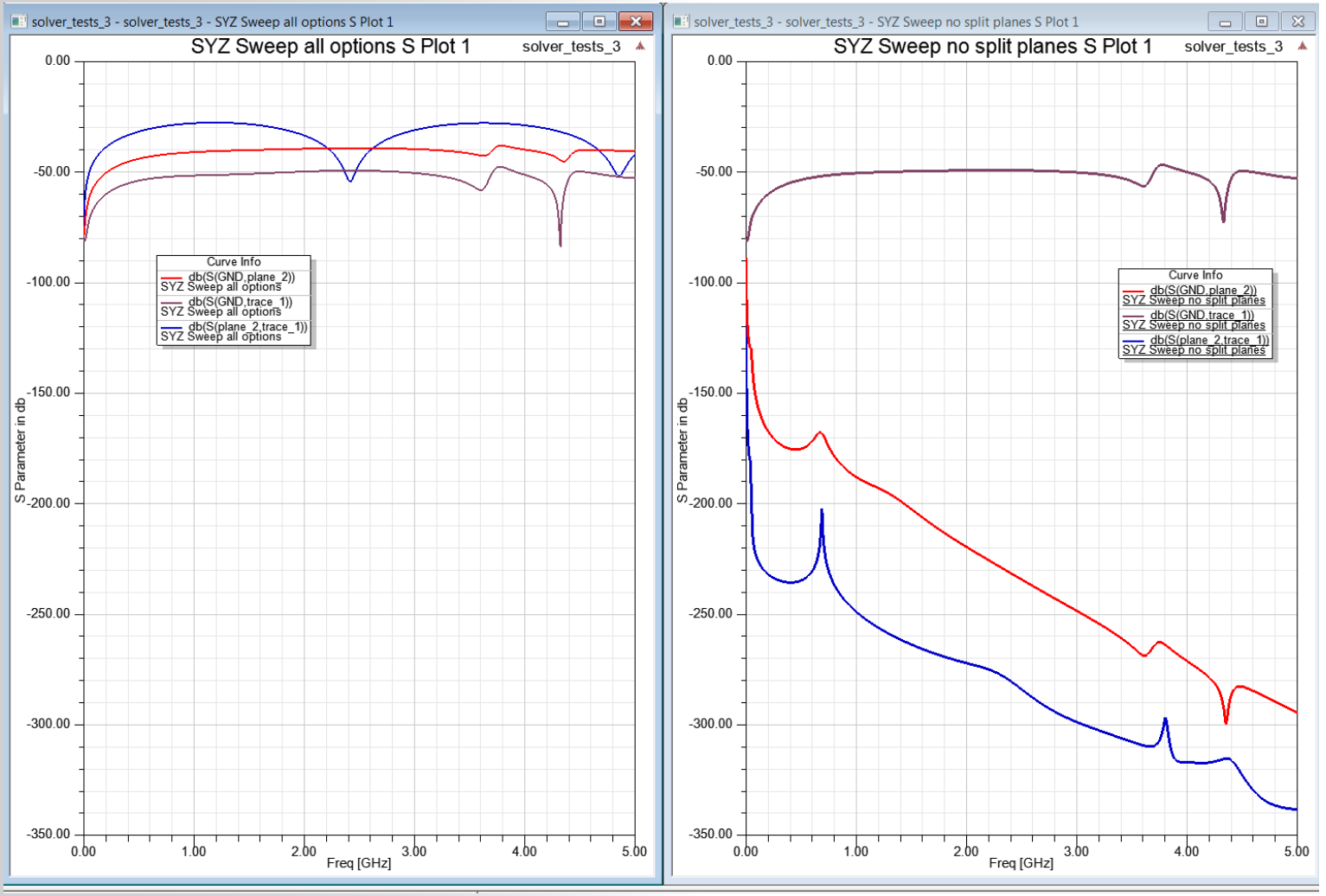




Coupling – Split Plane

With and Without Split Plane Coupling

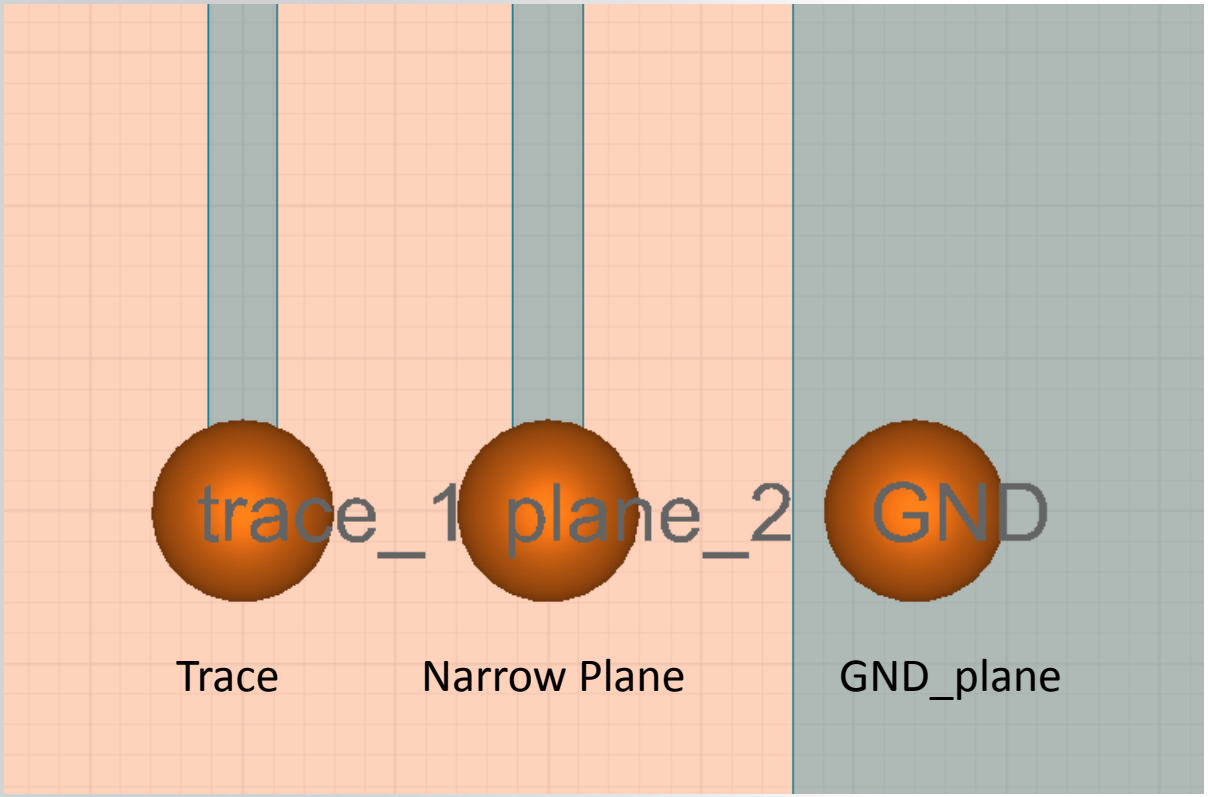
- Only coupling between the trace and GND plane are significant

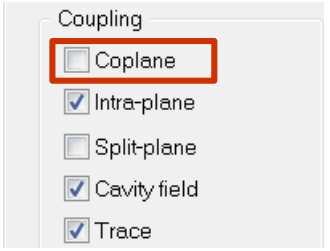


Coupling – Coplane

With and without Coplane Coupling

- When Split Plane Coupling is disabled, there is no direct coupling between trace_1 and plane_2
- If Coplane is also disabled, no coupling is computed between traces and planes

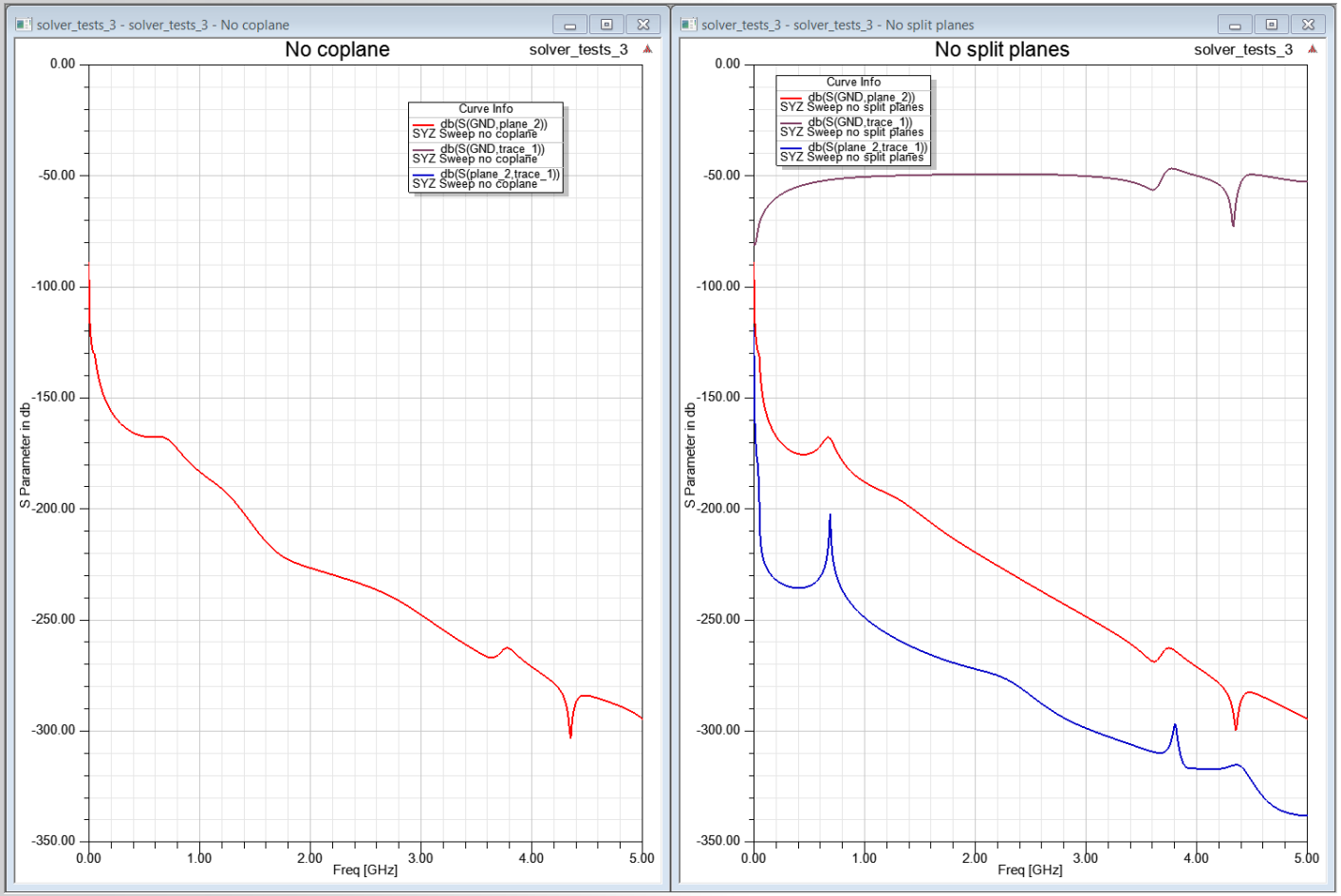




Coupling – Coplane

With and Without Coplane Coupling

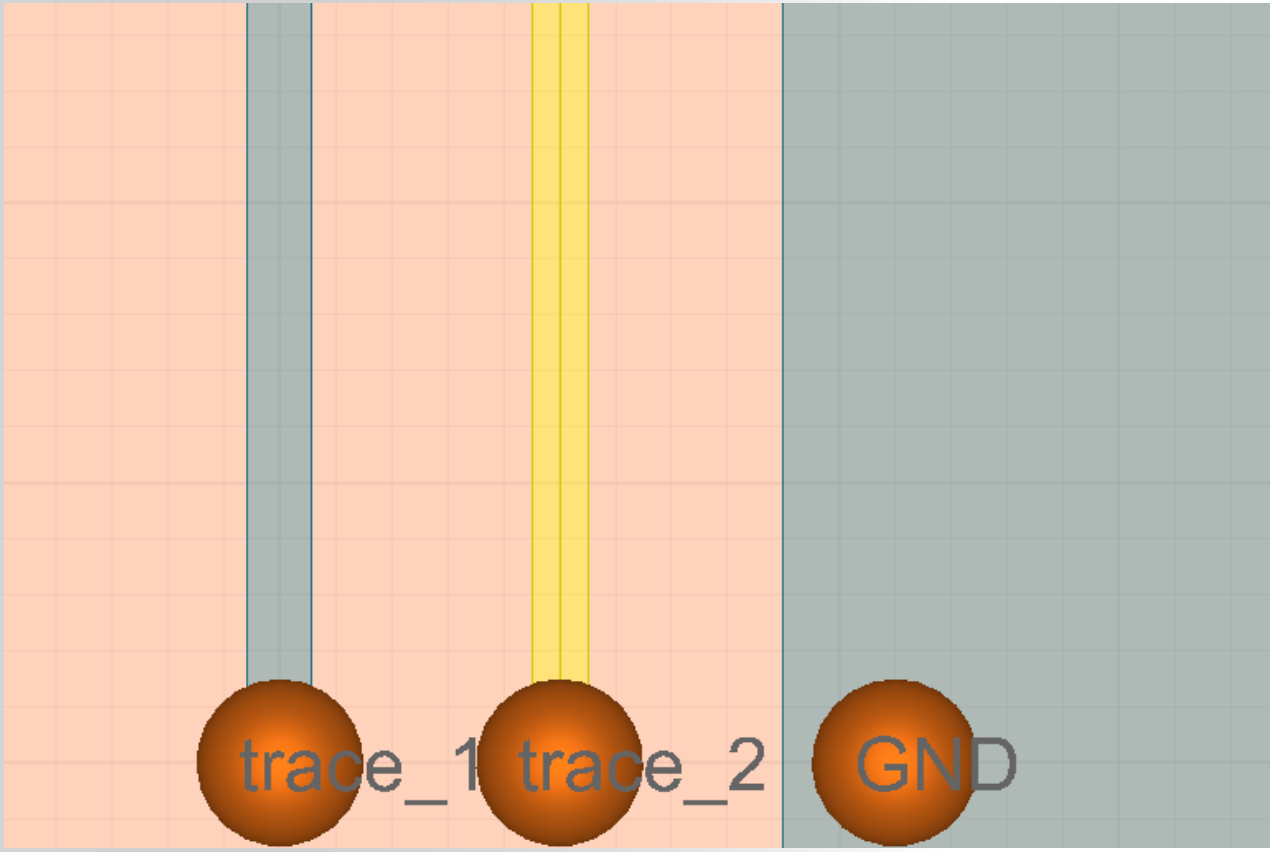
- Only coupling between the planes, plane_2 and GND are reported when Coplane is disabled

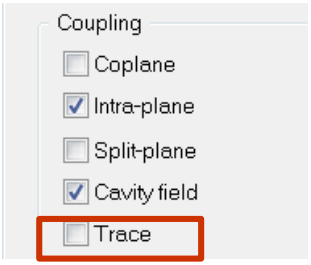


Case 3 – 2 traces, 1 plane

Coupling – Trace

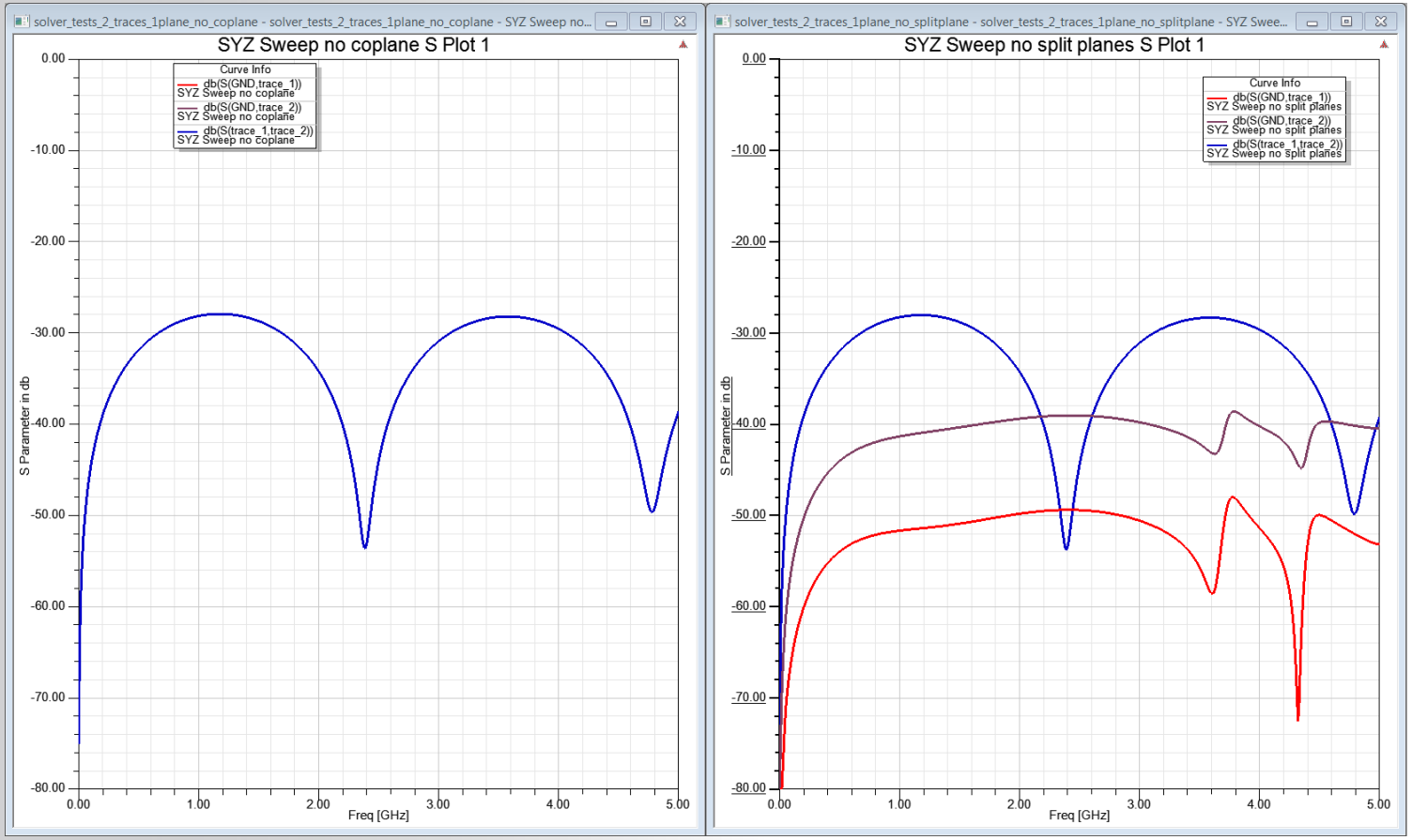
With and without Trace Coupling





Split Plane and Coplane Two Trace Model

- For the Two Trace Model the results are the same as the Split Plane Enabled
- Disabling the Coplane excludes the coupling between each trace and the ground



Coupling – Trace

With and Without Trace Coupling

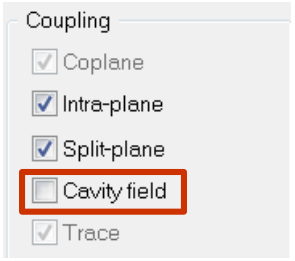
Freq [GHz]	db(S(GND,trace_1)) SYZ Sweep all options two trace model	db(S(GND,trace_2)) SYZ Sweep all options two trace model	db(S(trace_1,trace_2)) SYZ Sweep all options two trace model
0.001000	-80.094041	-79.939533	-80.268550
0.010998	-81.500037	-74.406131	-63.452760
0.020996	-79.837461	-69.370202	-58.019106
0.030994	-77.104160	-66.019871	-54.757956
0.040992	-74.213273	-63.519997	-52.439362
0.050990	-71.614311	-61.531155	-50.645301
0.060988	-70.062135	-60.043304	-49.143095
0.070986	-68.753971	-58.786333	-47.869037
0.080984	-67.626534	-57.699034	-46.762601
0.090982	-66.637847	-56.741630	-45.784876
0.100980	-65.758885	-55.886934	-44.909291
0.110978	-64.968820	-55.115593	-44.116836
0.120976	-64.252223	-54.413357	-43.393409
0.130974	-63.597366	-53.769421	-42.728244
0.140972	-62.995129	-53.175396	-42.112926
0.150970	-62.438292	-52.624630	-41.540749
0.160968	-61.921043	-52.111755	-41.006282
0.170966	-61.438639	-51.632369	-40.505065
0.180964	-60.987161	-51.182820	-40.033393
0.190962	-60.563334	-50.760038	-39.588152
0.200960	-60.164395	-50.361418	-39.166703
0.210958	-59.787992	-49.984729	-38.766791
0.220956	-59.432106	-49.628047	-38.386472
0.230954	-59.094988	-49.289698	-38.024060
0.240952	-58.775118	-48.968215	-37.678086
0.250950	-58.471159	-48.662309	-37.347257
0.260948	-58.181934	-48.370838	-37.030433
0.270946	-57.906399	-48.092784	-36.726604
0.280944	-57.643621	-47.827237	-36.434869
0.290942	-57.392766	-47.573381	-36.154421
0.300940	-57.153082	-47.330479	-35.884537
0.310938	-56.923888	-47.097862	-35.624563
0.320936	-56.704568	-46.874923	-35.373909
0.330934	-56.494560	-46.661110	-35.132038
0.340932	-56.293350	-46.455915	-34.898460
0.350930	-56.100465	-46.258873	-34.672731
0.360928	-55.915472	-46.069557	-34.454441
0.370926	-55.737971	-45.887570	-34.243215
0.380924	-55.567591	-45.712547	-34.038708
0.390922	-55.403988	-45.544148	-33.840601
0.400920	-55.246843	-45.382057	-33.648601
0.410918	-55.095858	-45.225980	-33.462434
0.420916	-54.950755	-45.075642	-33.281847
0.430914	-54.811272	-44.930786	-33.106607
0.440912	-54.677165	-44.791169	-32.936492
0.450910	-54.548206	-44.656566	-32.771301
0.460908	-54.424177	-44.526762	-32.610841
0.470906	-54.304875	-44.401557	-32.454934
0.480904	-54.190106	-44.280761	-32.303413
0.490902	-54.079690	-44.164193	-32.156122

Freq [GHz]	db(S(GND,trace_1)) SYZ Sweep no trace two trace model	db(S(GND,trace_2)) SYZ Sweep no trace two trace model	db(S(trace_1,trace_2)) SYZ Sweep no trace two trace model
0.001000	-inf	-inf	-inf
0.010998	-inf	-inf	-inf
0.020996	-inf	-inf	-inf
0.030994	-inf	-inf	-inf
0.040992	-inf	-inf	-inf
0.050990	-inf	-inf	-inf
0.060988	-inf	-inf	-inf
0.070986	-inf	-inf	-inf
0.080984	-inf	-inf	-inf
0.090982	-inf	-inf	-inf
0.100980	-inf	-inf	-inf
0.110978	-inf	-inf	-inf
0.120976	-inf	-inf	-inf
0.130974	-inf	-inf	-inf
0.140972	-inf	-inf	-inf
0.150970	-inf	-inf	-inf
0.160968	-inf	-inf	-inf
0.170966	-inf	-inf	-inf
0.180964	-inf	-inf	-inf
0.190962	-inf	-inf	-inf
0.200960	-inf	-inf	-inf
0.210958	-inf	-inf	-inf
0.220956	-inf	-inf	-inf
0.230954	-inf	-inf	-inf
0.240952	-inf	-inf	-inf
0.250950	-inf	-inf	-inf
0.260948	-inf	-inf	-inf
0.270946	-inf	-inf	-inf
0.280944	-inf	-inf	-inf
0.290942	-inf	-inf	-inf
0.300940	-inf	-inf	-inf
0.310938	-inf	-inf	-inf
0.320936	-inf	-inf	-inf
0.330934	-inf	-inf	-inf
0.340932	-inf	-inf	-inf
0.350930	-inf	-inf	-inf
0.360928	-inf	-inf	-inf
0.370926	-inf	-inf	-inf
0.380924	-inf	-inf	-inf
0.390922	-inf	-inf	-inf
0.400920	-inf	-inf	-inf
0.410918	-inf	-inf	-inf
0.420916	-inf	-inf	-inf
0.430914	-inf	-inf	-inf
0.440912	-inf	-inf	-inf
0.450910	-inf	-inf	-inf
0.460908	-inf	-inf	-inf
0.470906	-inf	-inf	-inf
0.480904	-inf	-inf	-inf
0.490902	-inf	-inf	-inf

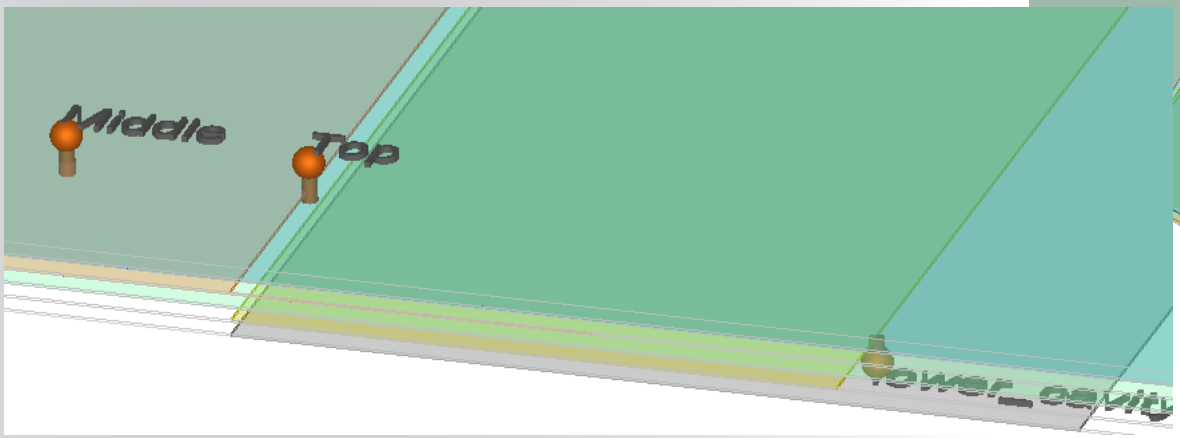
Coupling – Cavity

With and without Cavity Field Coupling

- Cavity Field coupling models the effect of fringe field between cavities
- Two cavities are represented by the following stackup



C...	Name	Type
	DIELECTRIC-1	DIELECTRIC
	Top	METAL
	DIELECTRIC-2	DIELECTRIC
	Middle	METAL
	DIELECTRIC-3	DIELECTRIC
	Bottom	METAL
	DIELECTRIC-4	DIELECTRIC
	Middle2	METAL
	DIELECTRIC-5	DIELECTRIC
	Bottom2	METAL



Coupling – Trace

With and Without Trace Coupling

- Coupling between the Top Layer, top cavity and bottom layer, bottom cavity

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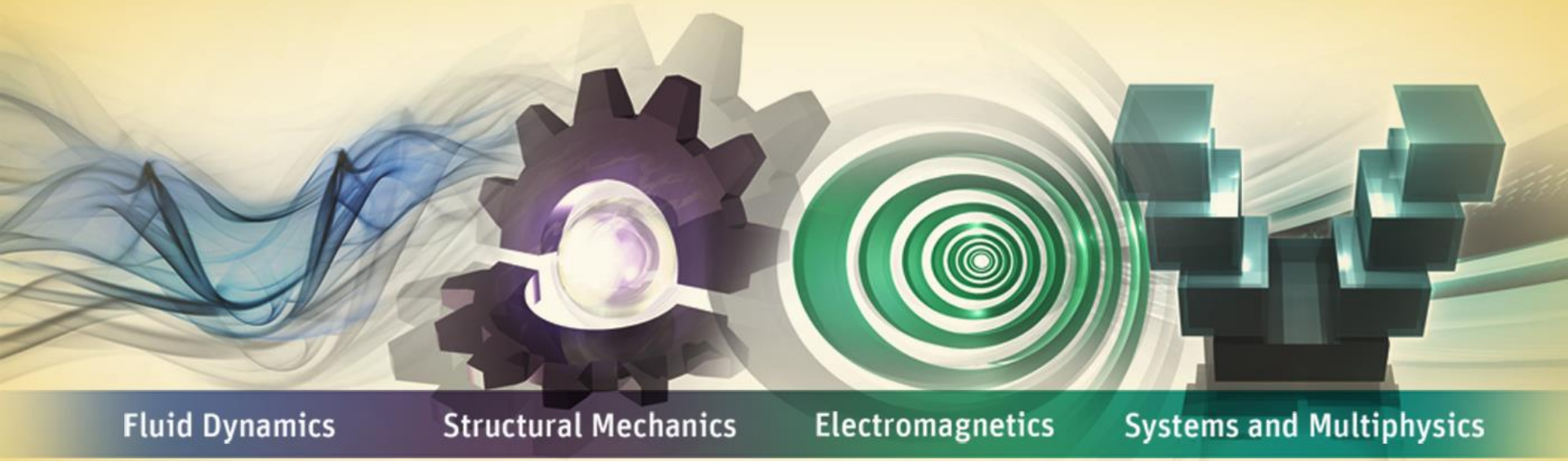
Recommended SIwave Solution Settings

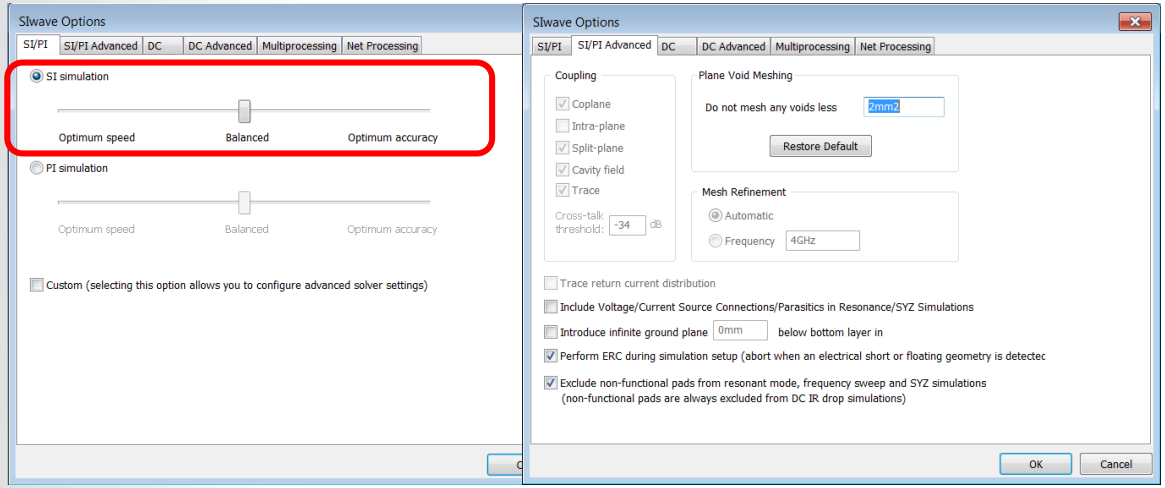


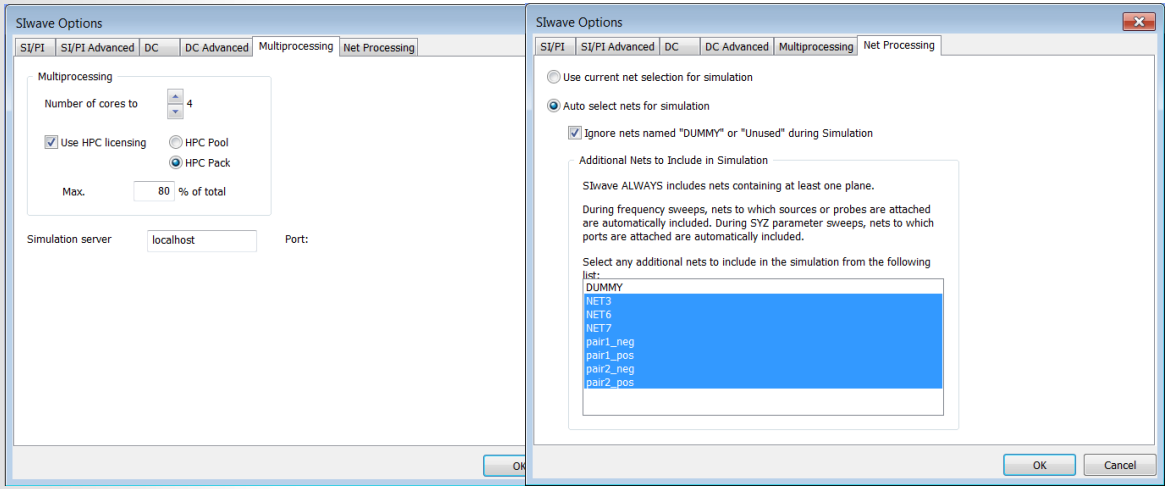
SYZ-SI

Recommended Settings

- Automatic void detection preferred
- Enable coupling except intra-plane coupling
- Disable trace return current distribution
- Do not select additional nets to include in the simulation

- Use Trace return current distribution when signal traces switch layers frequently (slowdown)



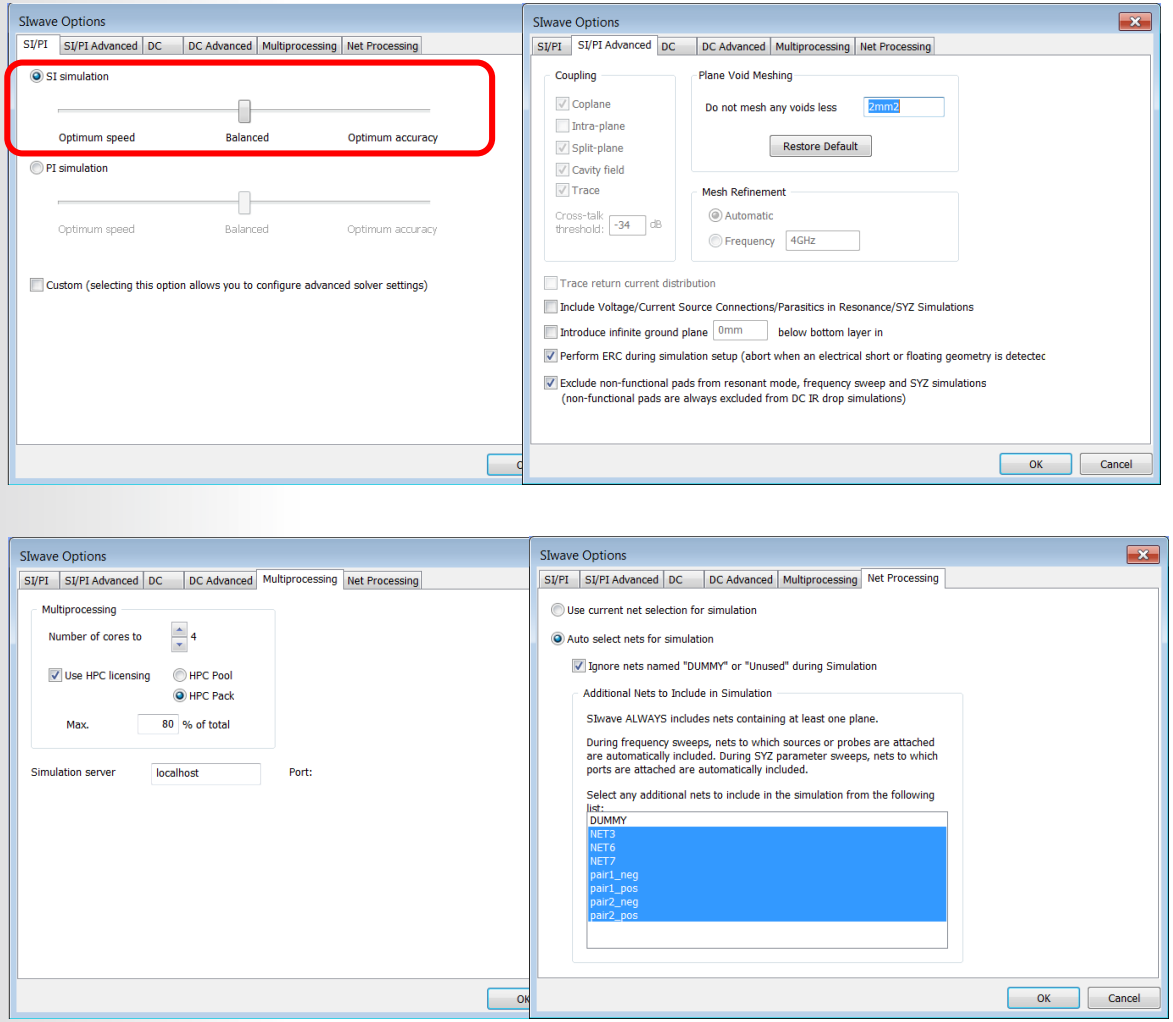


SYZ-RF

Recommended Settings

- Explicitly set the Plane Void Meshing for a low bandwidth sweep up to a few GHz
- Enable coupling except intra-plane coupling
- Disable trace return current distribution
- Select additional nets to include in the simulation if S-parameters models are attached to components

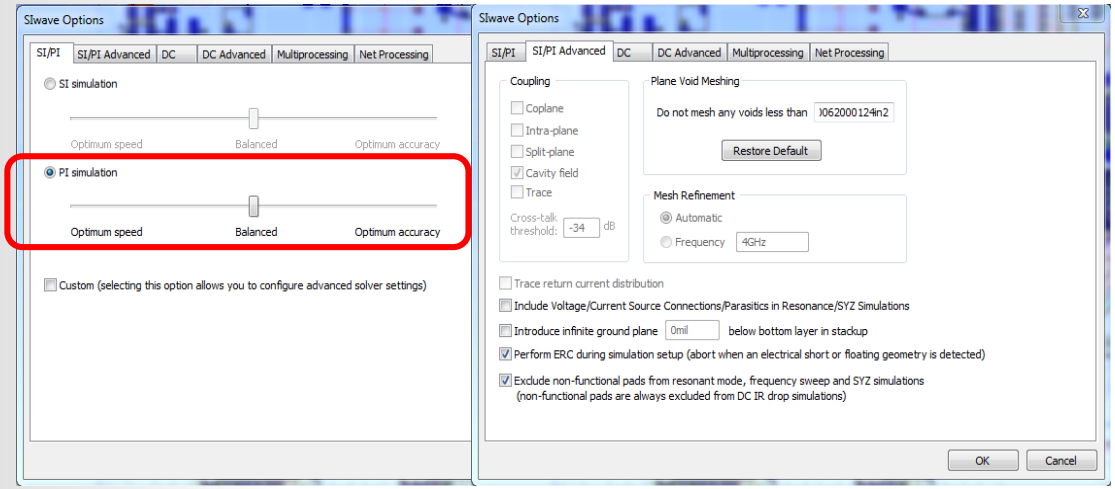
- Use Trace return current distribution when signal traces switch layers frequently (slowdown)



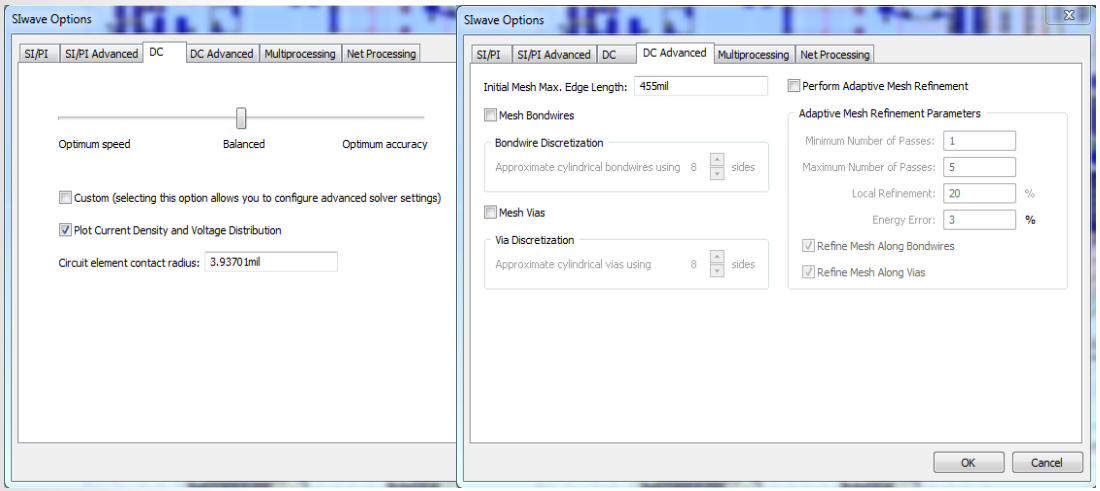
SYZ-PI

Recommended Settings

- Automatic void detection preferred
- Disable all coupling
- Disable trace return current distribution
- Do not select additional nets to include in the simulation



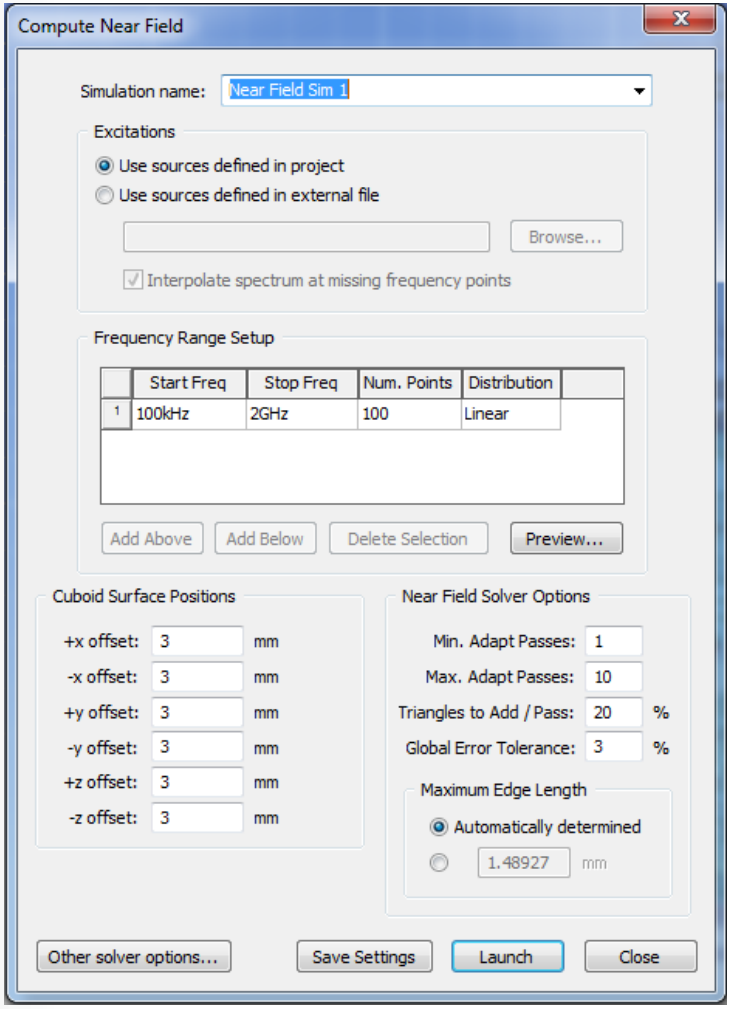
- Use do not Explicitly Mesh voids < 0mm^2 when PI solutions contain Hatched Planes (Slowdown)
- Use Intra-plane Coupling when DC solution accuracy is extremely important (RAM increase & slowdown)



Near Field

Recommended Settings

- Select a few frequency points only (harmonics)
- Select an observation layer at least 3mm away from the PCB



SIwave Setup Guide for SYZ simulation

- **Use the Djordjevic-Sarkar model**
  - SIwave "standard" dielectrics use Djordjevic-Sarkar by default
- **Frequency Sweep**
  - Include DC point
  - Decade sweep from low frequency to around 1GHz
  - Linear spaced sweep for 1GHz to highest frequency
  - Set highest frequency to a minimum .35/tr where tr is the rise time
  - Error Tolerance : Set to .001 (default is .005)
- **Impedances**
  - Set power plane solution impedances to 1 ohm
  - Set transmission line solution impedances to 50 ohm
- **Exporting s-parameter files**
  - Renormalize to 50 ohm or 1 ohm according to application.

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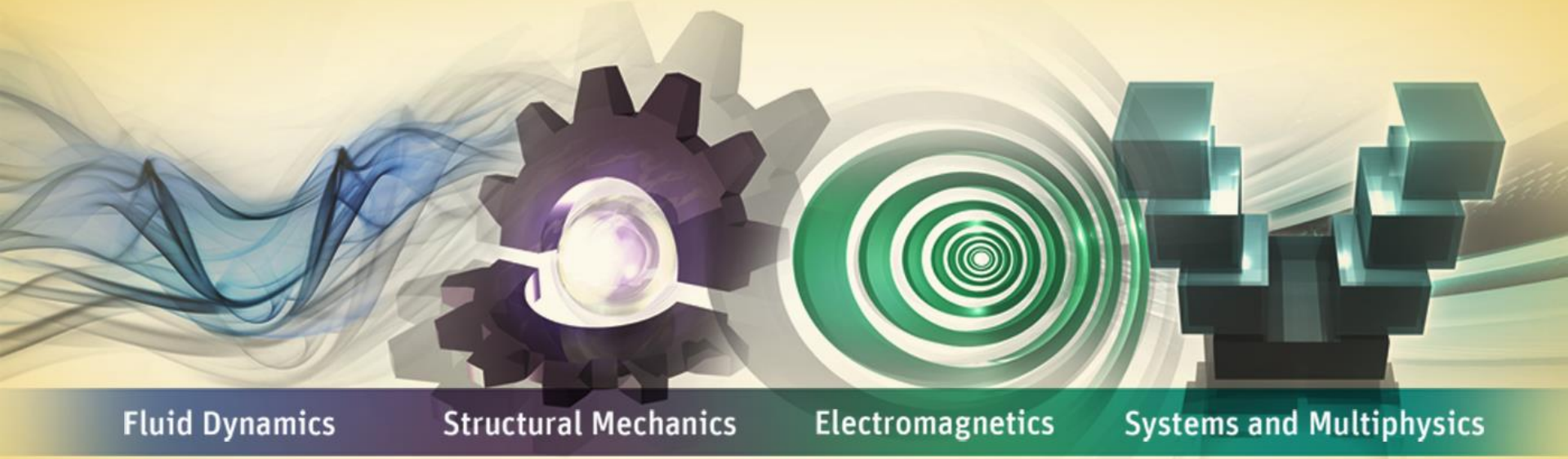
Signal Integrity simulation - Basics



Signal Integrity Analysis

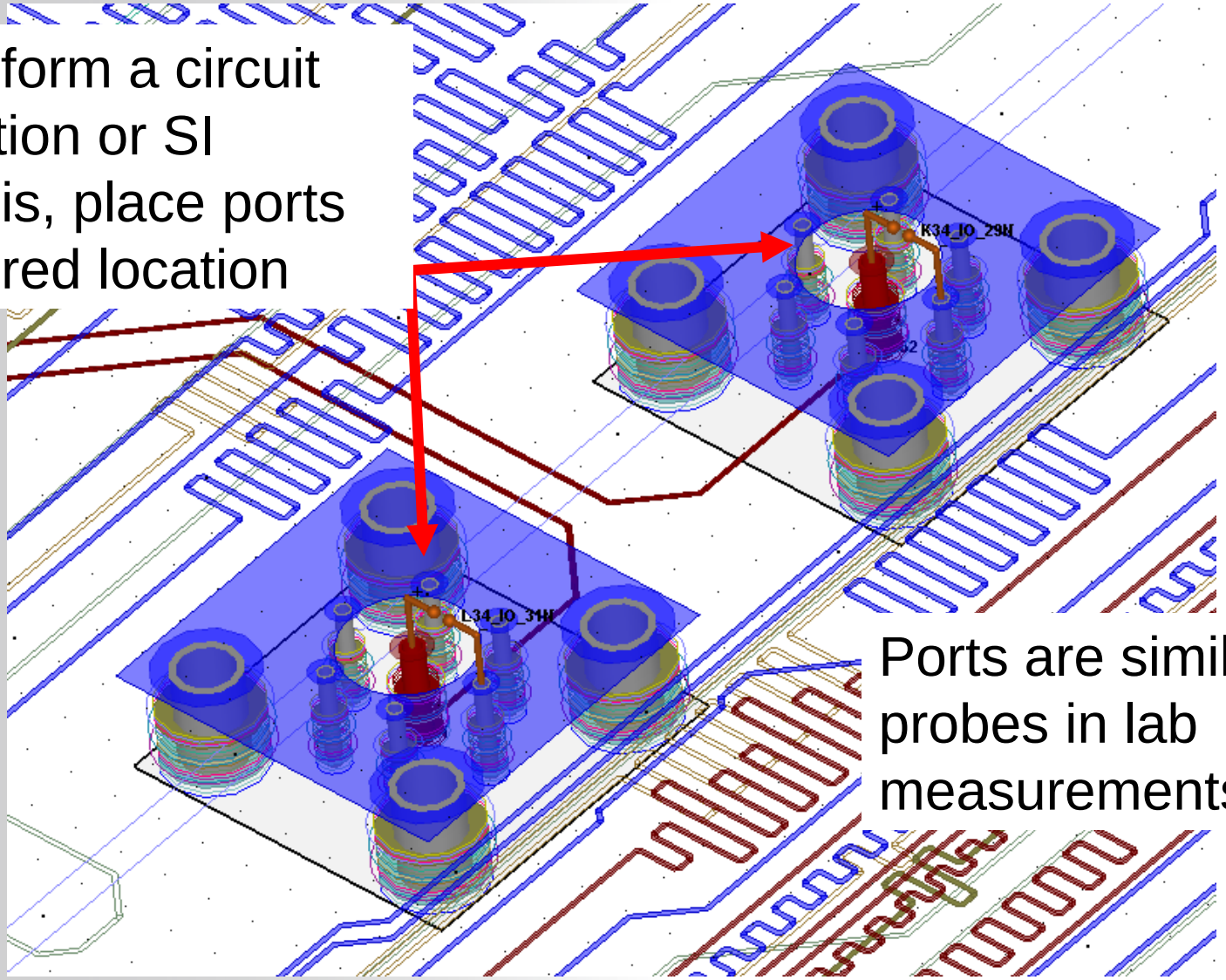
- SIwave can be used to extract models that accurately model return path, parasitics and all relevant coupling .
- Models can be in the form of a Touchstone file (v1.0 and v2.0), FWS SPICE subcircuit, lumped RLGC and others, and can be used for any time/frequency analysis

- SSO
  - Verify signaling with non-ideal power delivery to drivers
- Eye diagrams
  - Verify signal is clean enough for proper detection
- Cross-talk
  - Verify neighbors do not cause excessive noise

- Within SIwave environment, some analyses include Insertion/Return loss, Coupling, TDR and TDT, you can view frequency domain data and time domain data using an IFFT

SI Analysis Setup

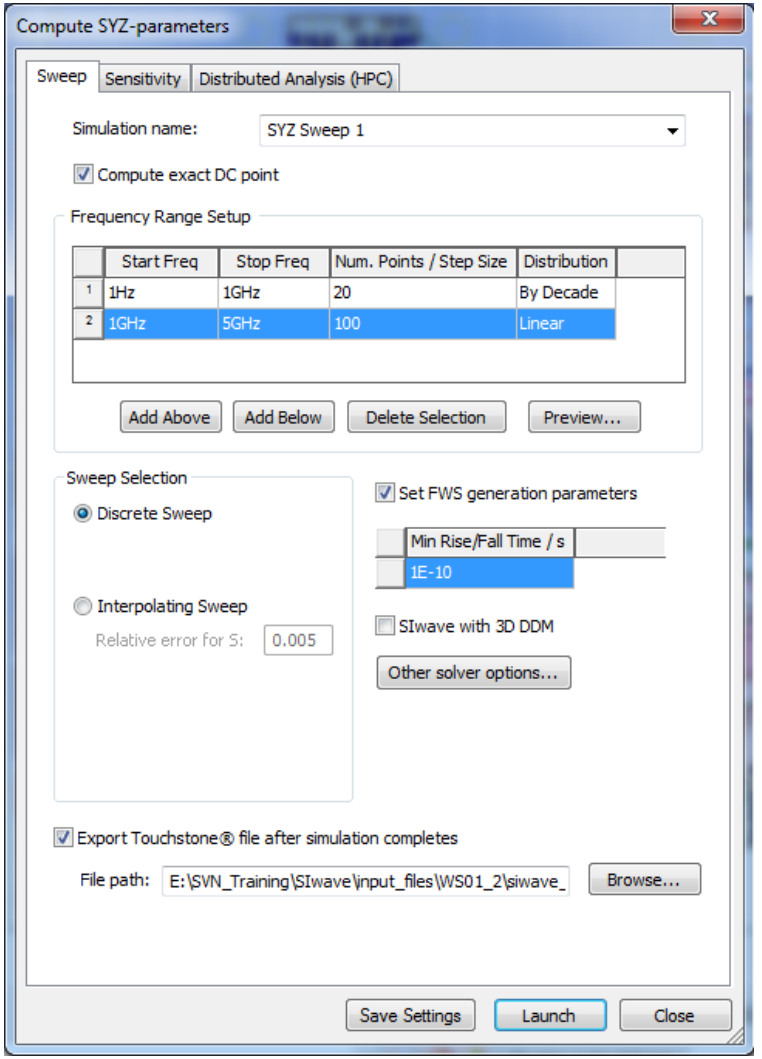
To Perform a circuit extraction or SI analysis, place ports in desired location



Ports are similar to probes in lab measurements

S-,Y-, Z- Analysis

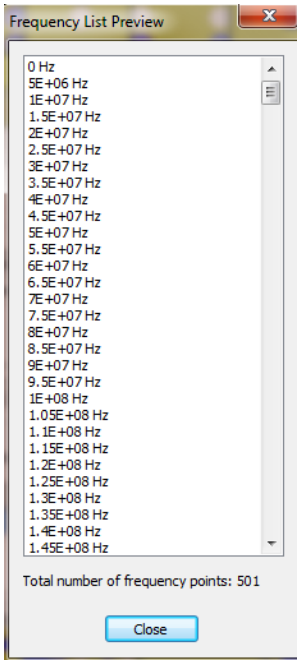
- **To extract S, Y and Z matrix for the predefined ports :**
  - **Simulation > Compute S-,Y-,Z-parameters**
  - **Enter the value for Start Frequency.**
    - Include DC point
    - Decade sweep from low frequency to around 1GHz
    - Linear spaced sweep for 1GHz to highest frequency
    - Set highest frequency to a minimum .35/tr where tr is the rise time
  - **Specify the Number of Solution Points.**
  - **Select the method for distributing points**
  - **Choose the sweep Selection**
    - **Discrete sweep**
    - **Interpolating sweep**



Frequency Sweep Selection box

Discrete Sweep :

- **All frequency points in the list are solved. Look at the Frequency List Preview.**



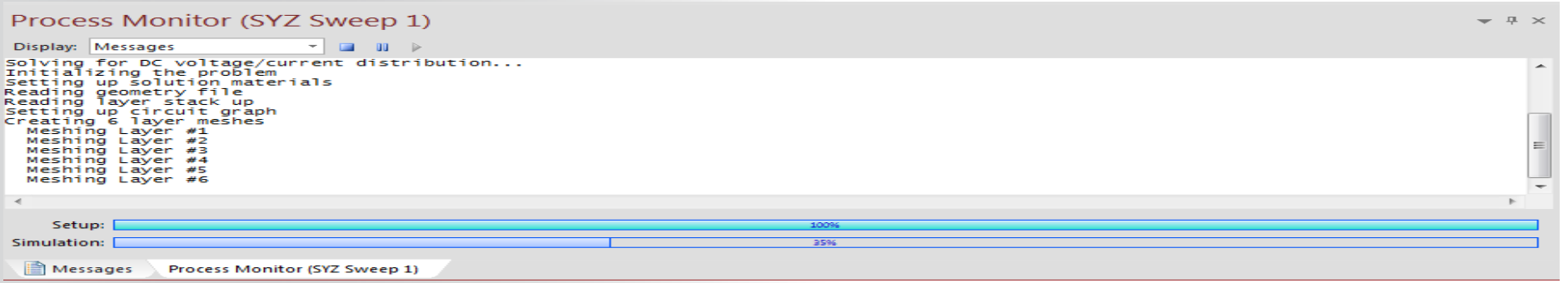
Interpolating Sweep :

- Following an Error tolerance, an interpolating sweep estimates a frequency response for an entire frequency range by solving at a relatively small number of frequency points within that range. Between the actual solution frequencies, the frequency response is obtained by rational interpolation. SIwave adaptively chooses the frequency points at which it computes the field solution. After a new frequency point is solved, a new interpolating fit is generated. This is compared to the interpolant from the previous step, and the maximum difference between the two is determined. If the difference exceeds the requested tolerance, then a new frequency point is chosen for a solution. The interpolating sweep is complete when the difference between successive interpolants is less than the error tolerance criterion.

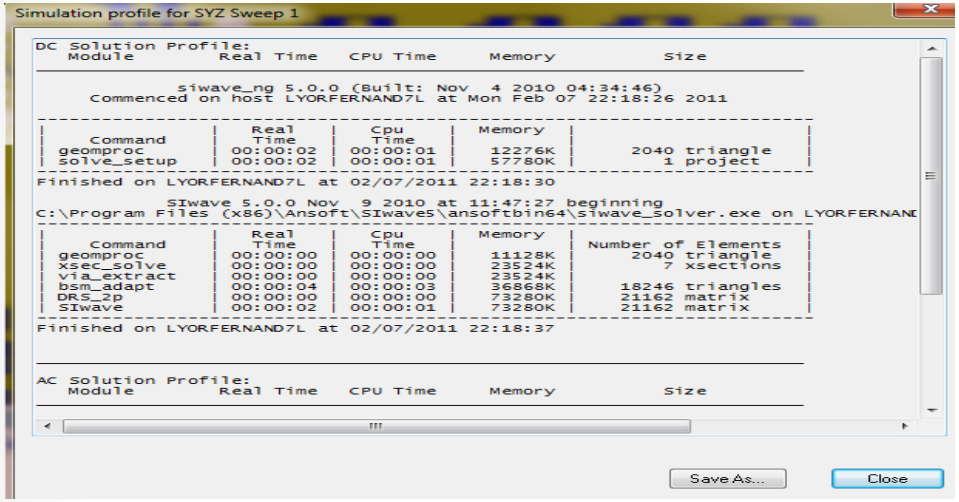
- **Optionally, to save these settings and use them for subsequent simulations, click the Save Settings button**

Simulation Profile

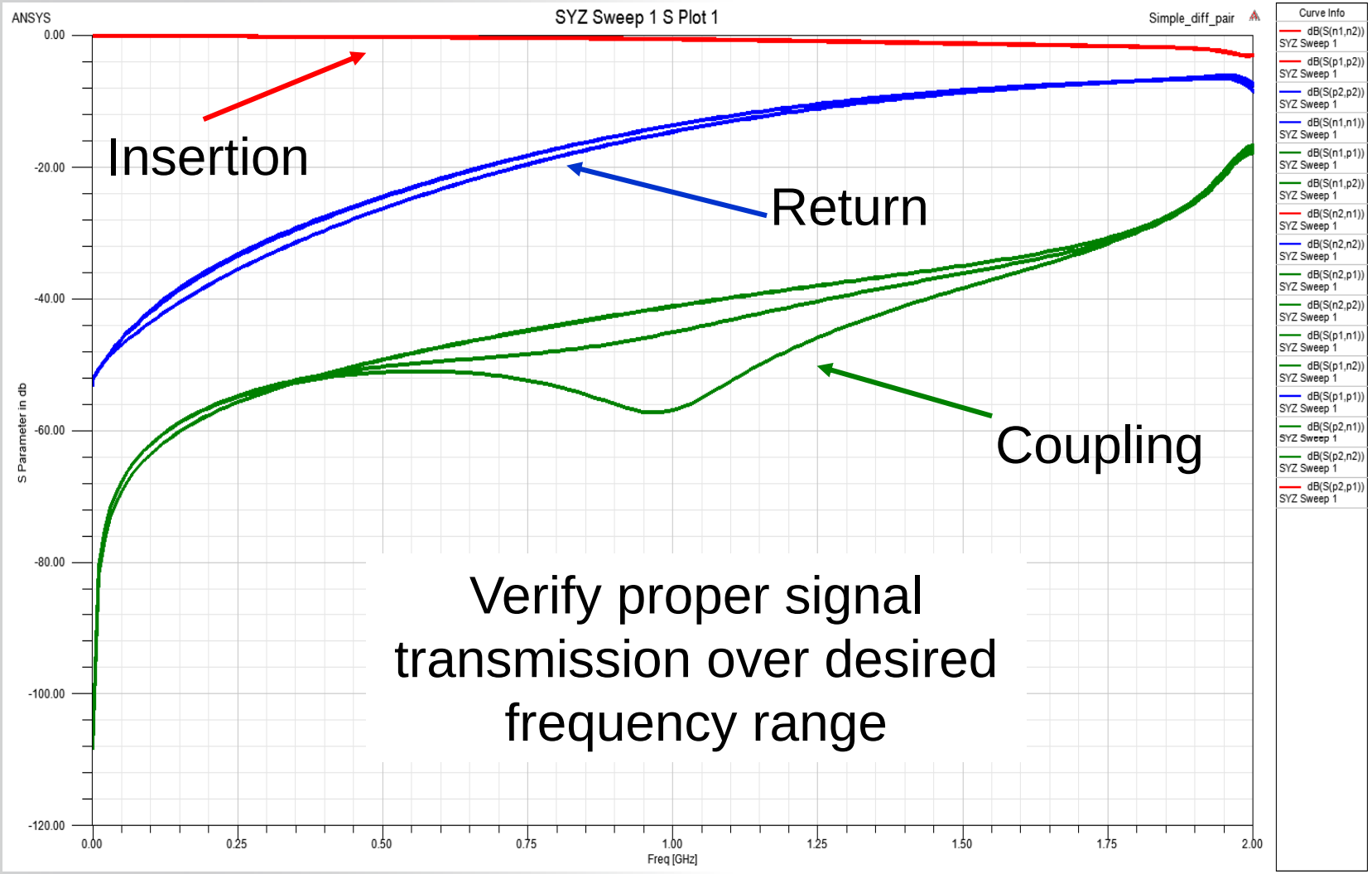
- During simulation, in the Process Monitor workspace, you can follow the simulation progress. profile, monitoring the real time, CPU time, memory requirements and view the matrix informations.



- When the simulation is done, the profile is available with real time, CPU time, memory requirements and view the matrix informations.
- Results > Analysis Name > View profile



Frequency Analysis



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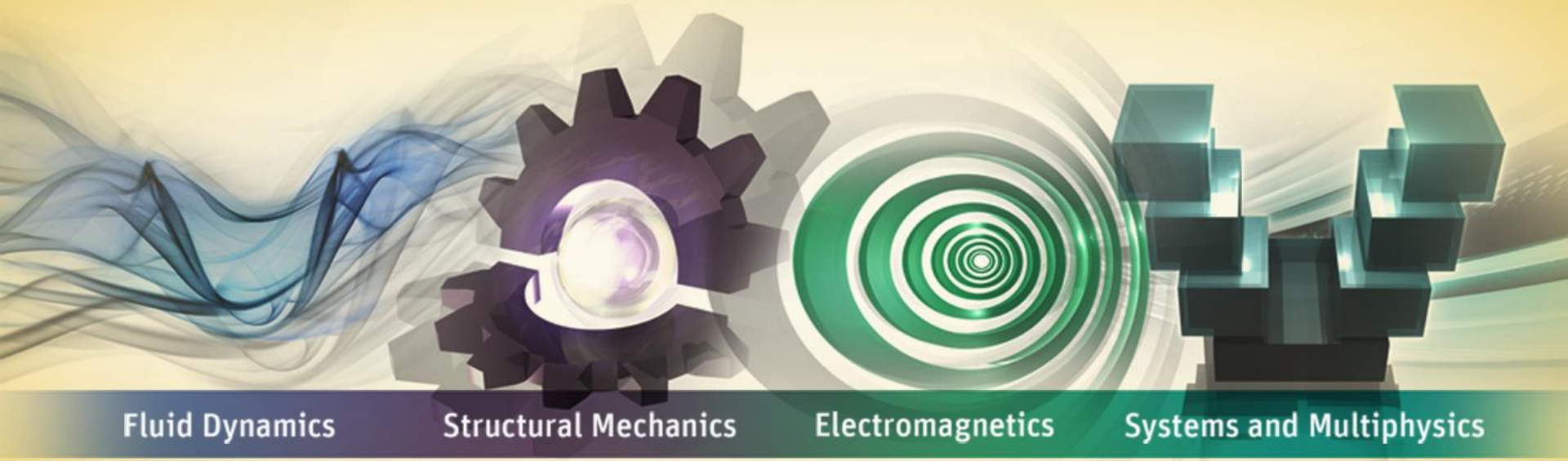
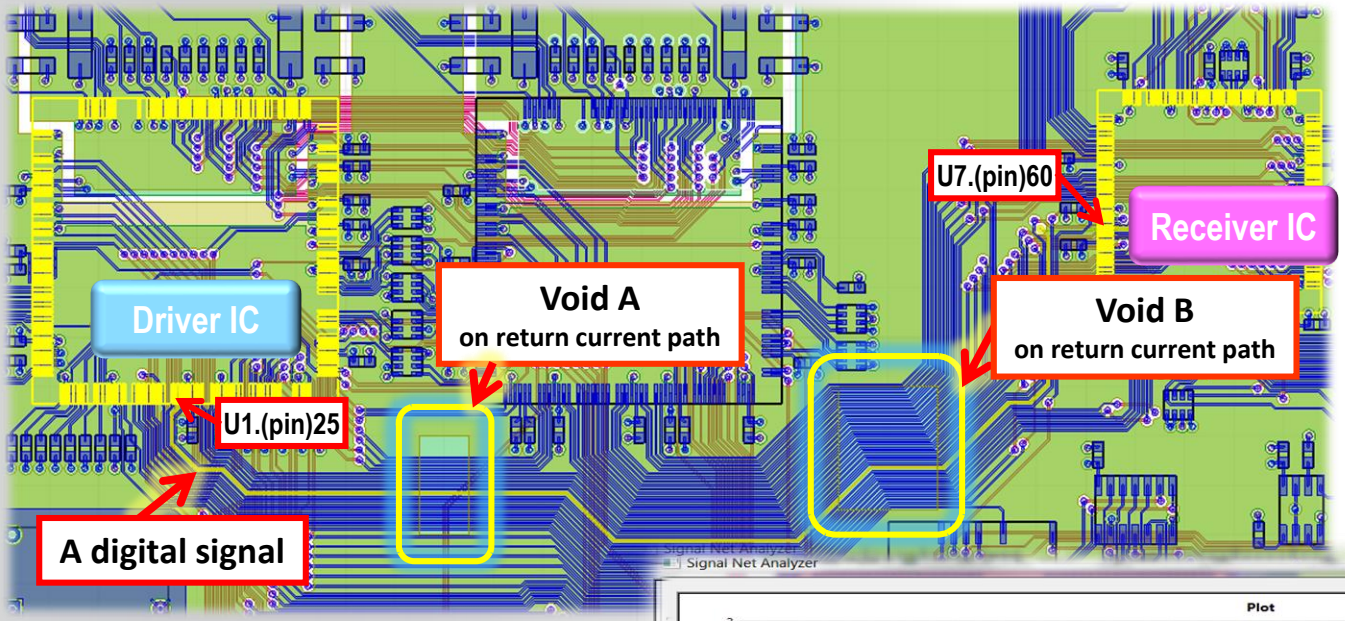
Signal Net Analyzer



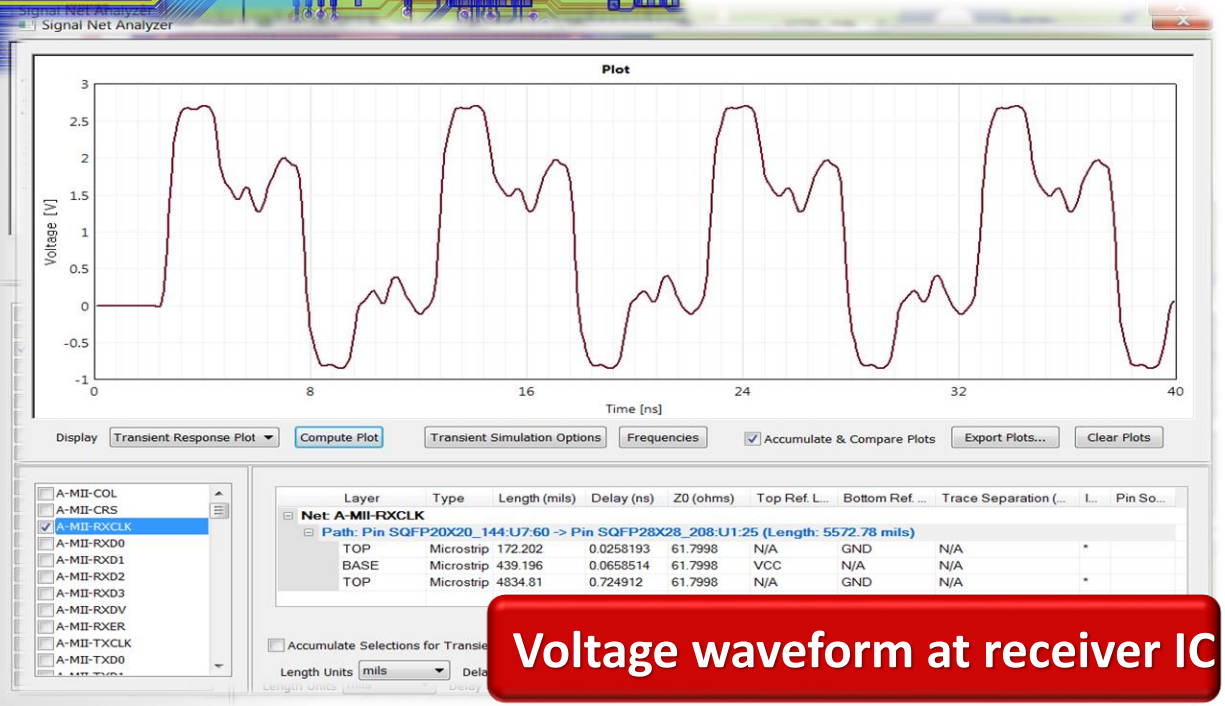
Signal Net Analyzer (SNA) in SIwave



SNA provides:

1. Z_o Profile & Delay for all paths of a signal.

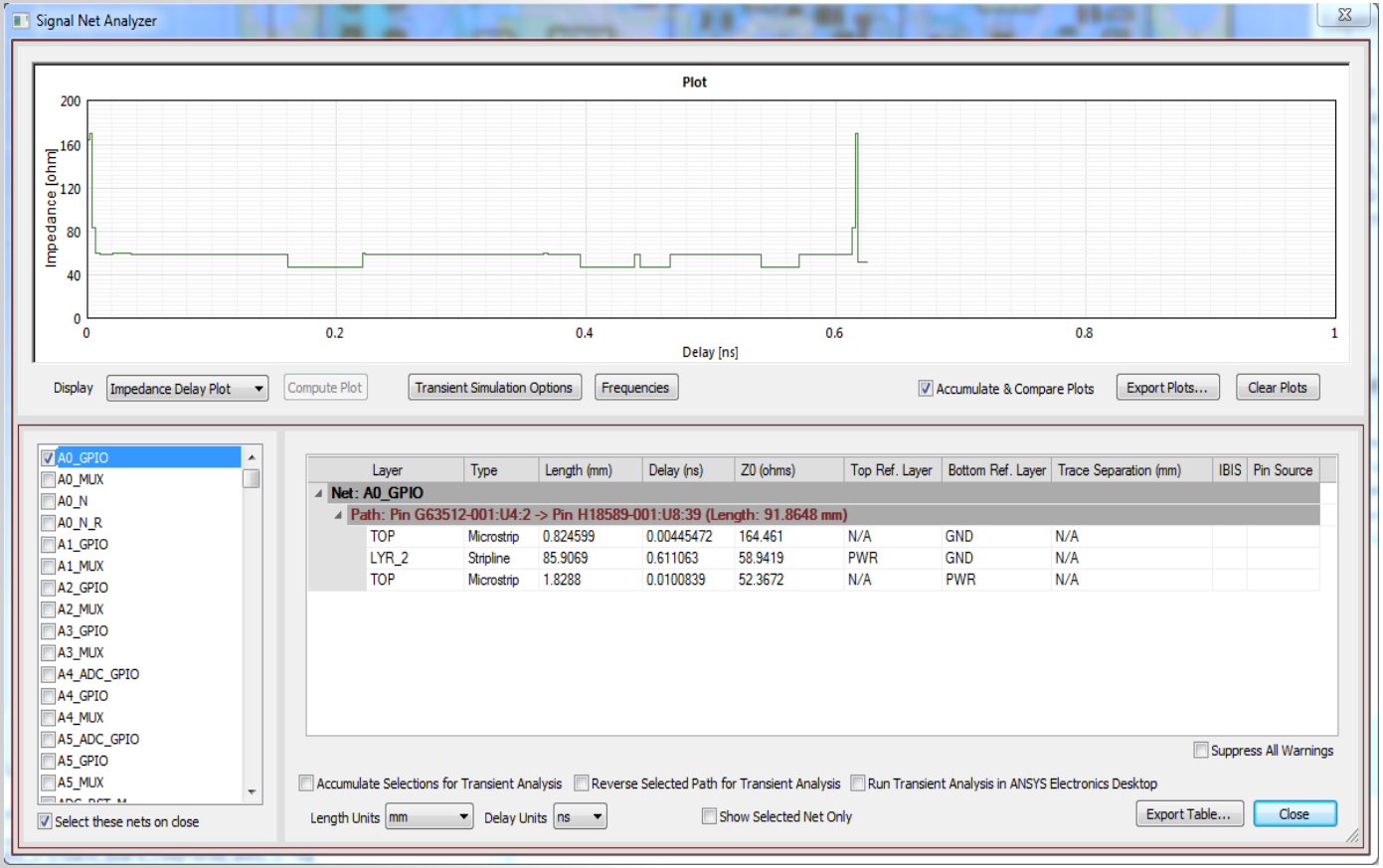
2. Reflection Noise through transient analysis.



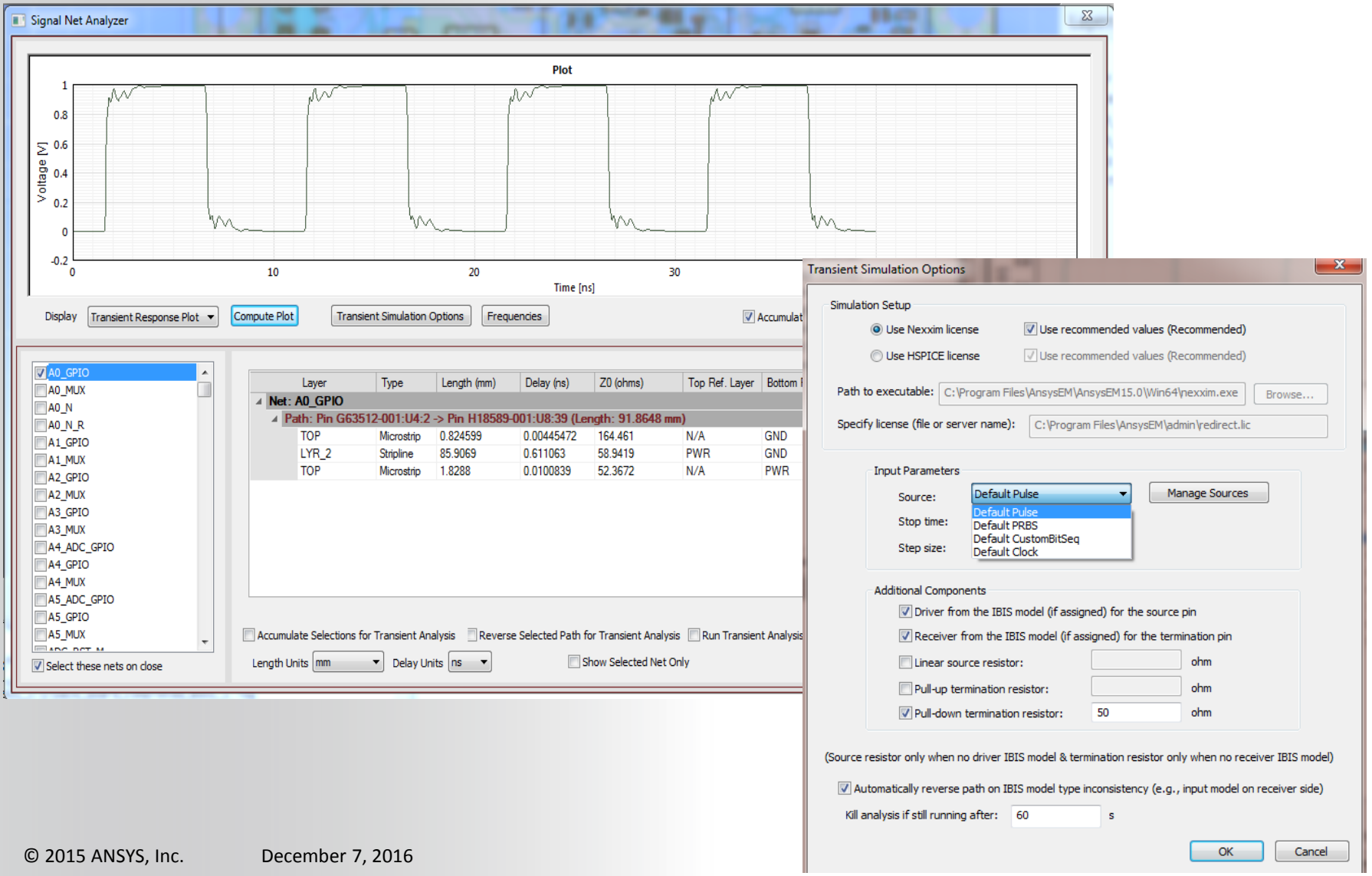
Voltage waveform at receiver IC

Signal Net Analyzer – Impedance Delay

- The Signal Net Analyzer gives you the ability to get a quick idea of characteristic impedance and also to rapidly generate transient voltage waveforms (using HSPICE or Nexxim simulations) of pin-to-pin signal propagation. The Signal Net Analyzer generates an impedance delay plot for each trace path selected. It also works for differential pairs.
- Tools > Signal Net Analyzer



Signal Net Analyzer – Transient Response



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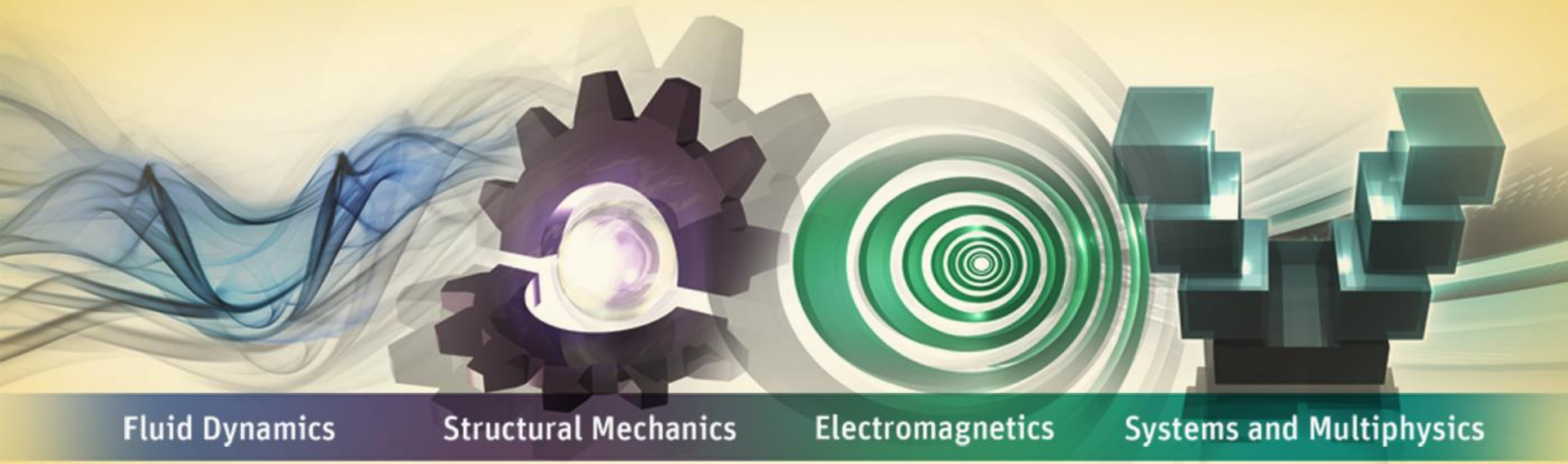
SIwizard

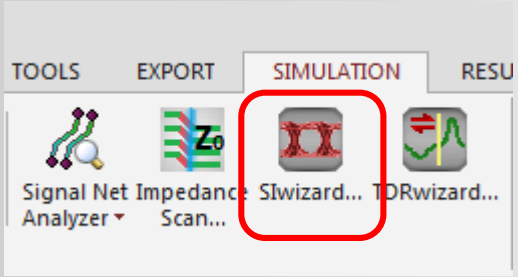


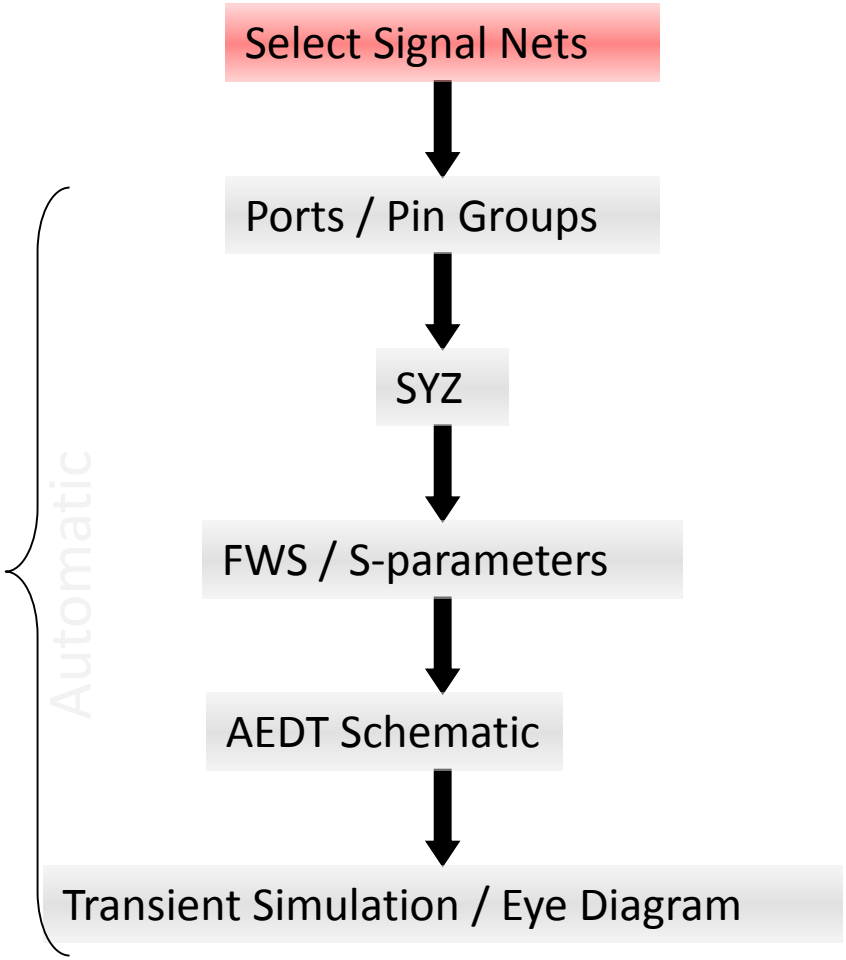
SIwizard

Simulation > SIwizard…

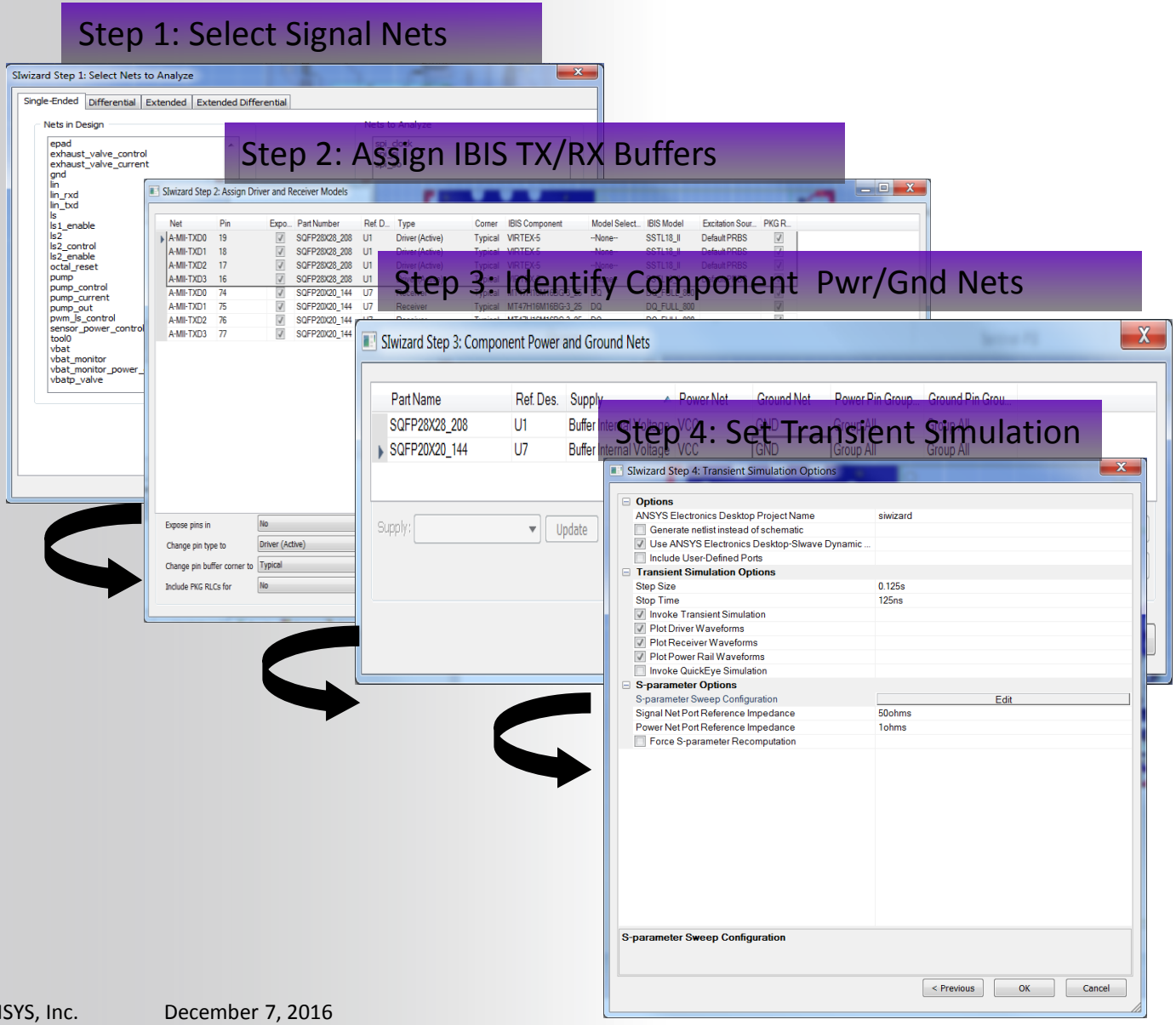
Automates the creation of

- **Pin groups containing power/ground pins**
- **Ports on both signal and power nets**
- **SYZ data (DC to fstop, based on signal TR/TF)**
- **FWS deck**
- **AEDT schematic**
- **Time domain voltage waveforms at drivers, receivers and power supply pins of all buffers**
- **Eye diagrams**



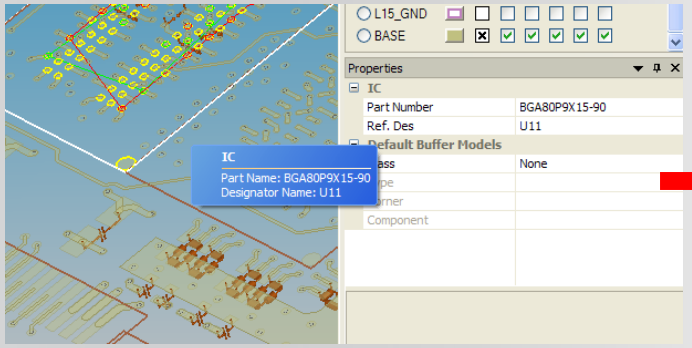


SIwizard

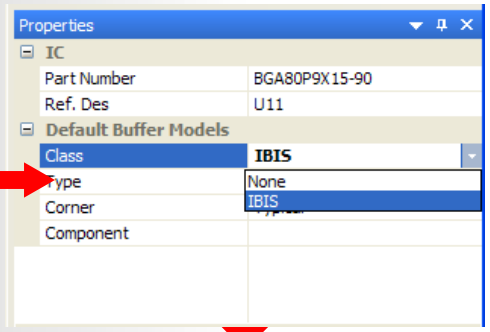


Buffer Assignment

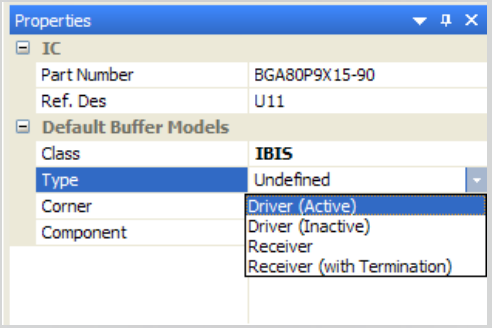
Select component in drawing area



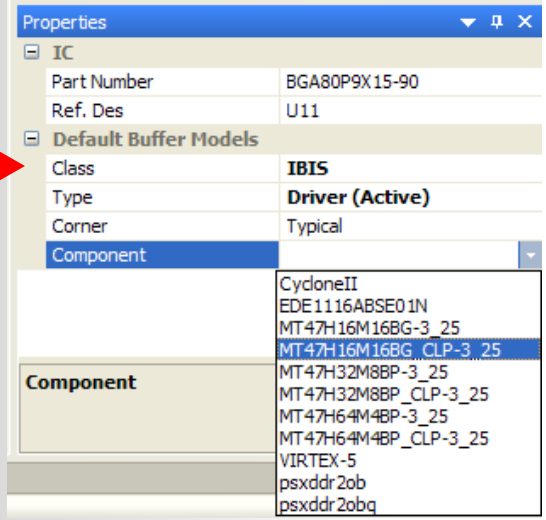
Set “Class” to IBIS



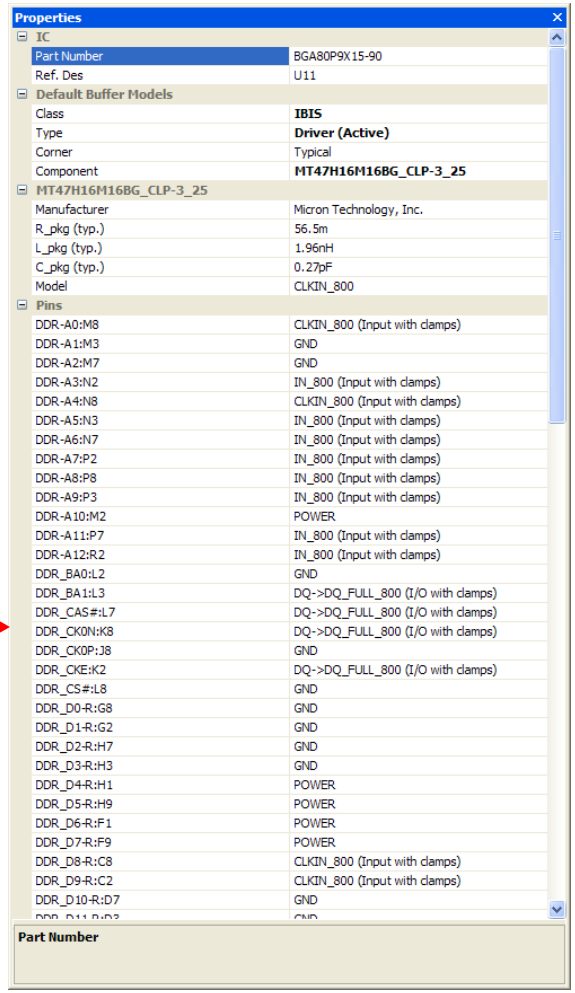
Set “Type”



Select IBIS Component

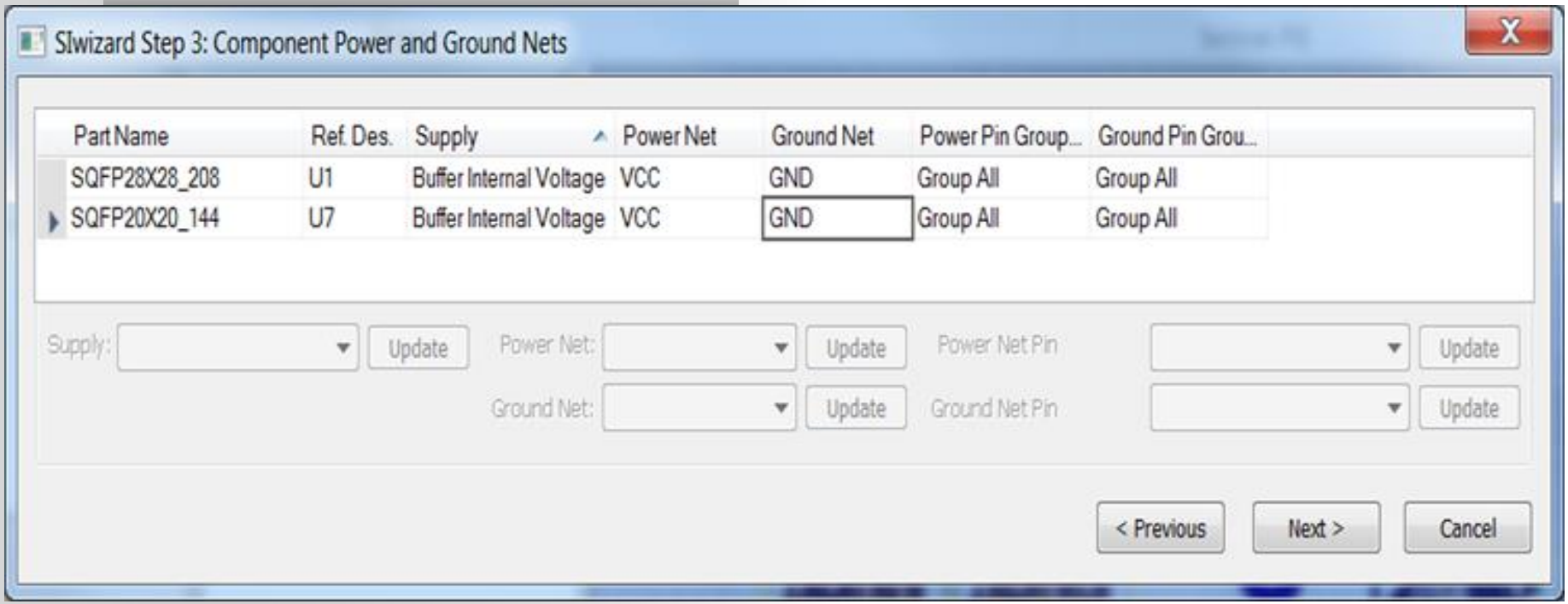


Correct IBIS buffer model assigned to all component pins



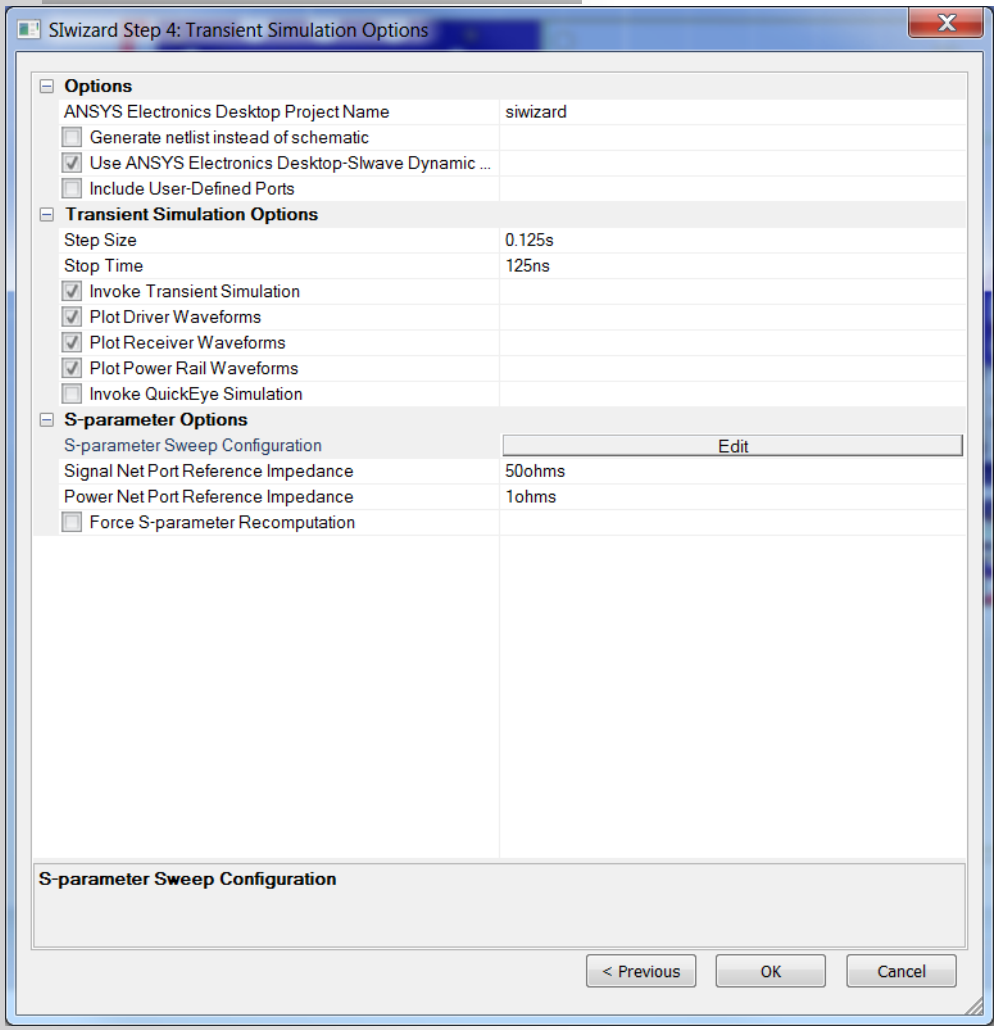
Automated Simulation Setup

Identify Component Pwr/Gnd Nets

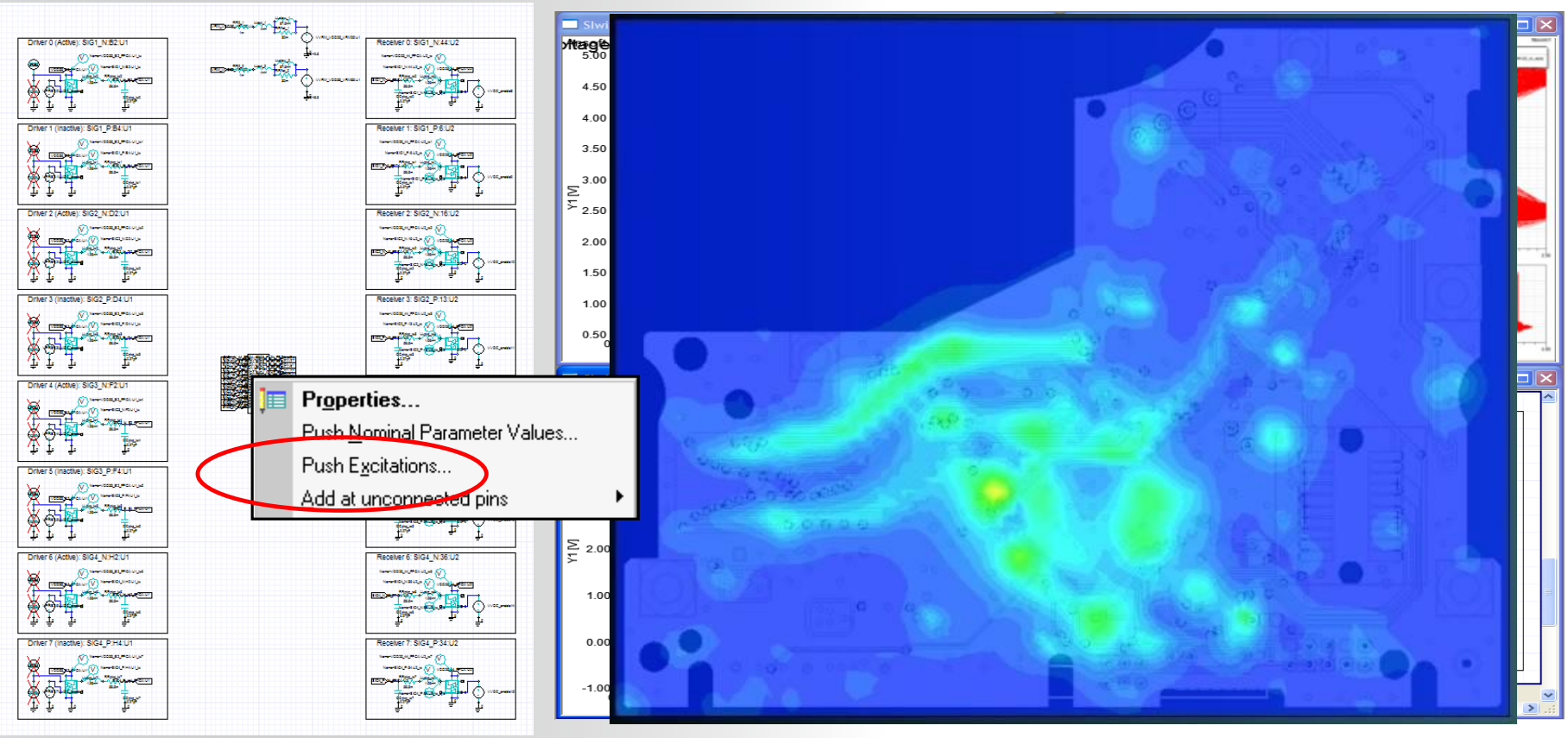


Automated Simulation Setup

Set Transient Simulation



Auto Generated AEDT Project and Transient Simulation Results



When Transient Analysis is complete, voltage/currents at the PCB terminals are „pushed“ back to the field solver.

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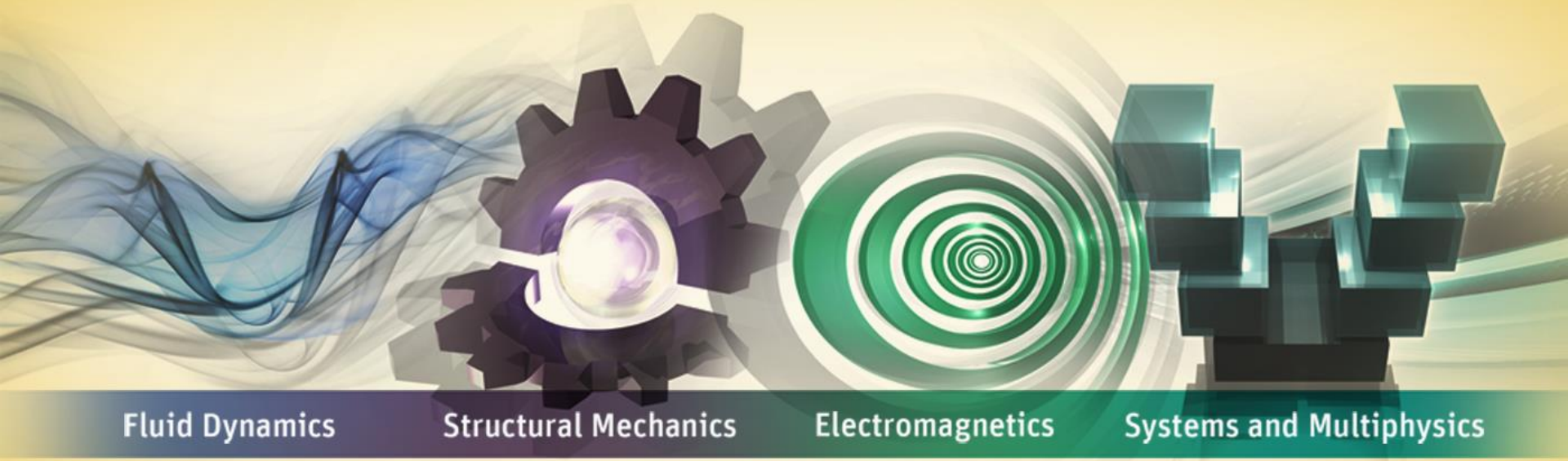
Power Integrity simulation - Basics



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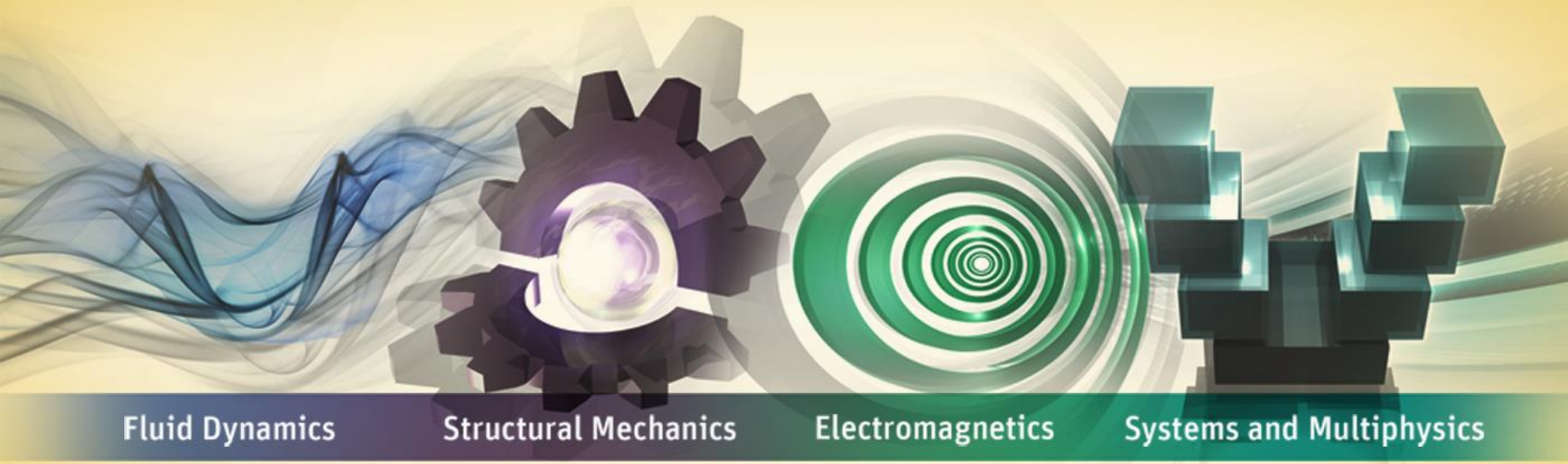
DC Analysis



SIwave - DC Analysis

- **IR Drop**
  - Verify supplied voltage at all active parts
- **Electromigration**
  - Verify maximum current denisity through vias
- **Bottle Necks**
  - Visualize regions of high current or voltage change

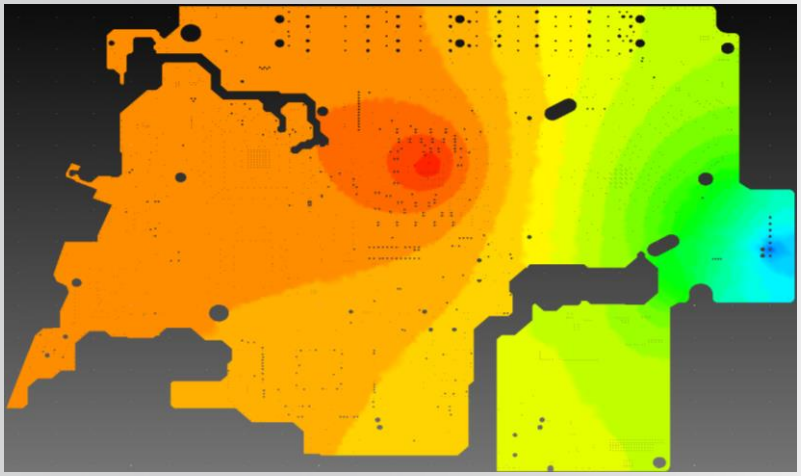
Perforated power and ground planes make for non-ideal DC supply rails

Components with different proximity to VRM will have different supplied voltage

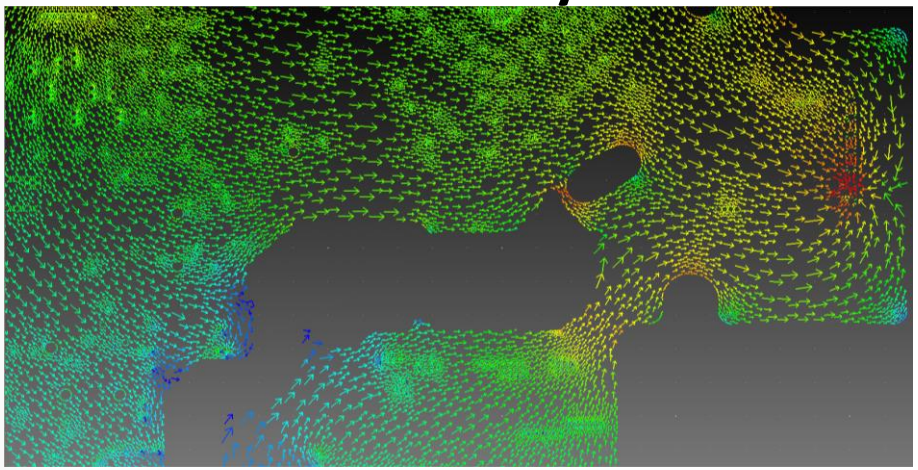
Voltage seen at each load must remain within specified tolerances of chip

SIwave - DC Solver

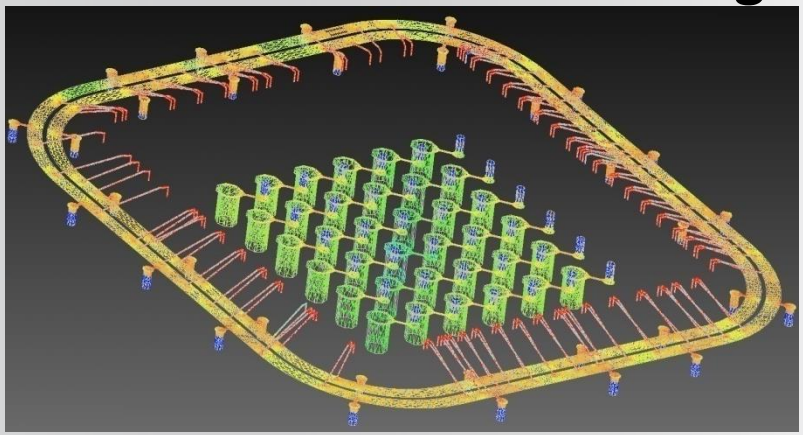
- DC Voltage Distributions



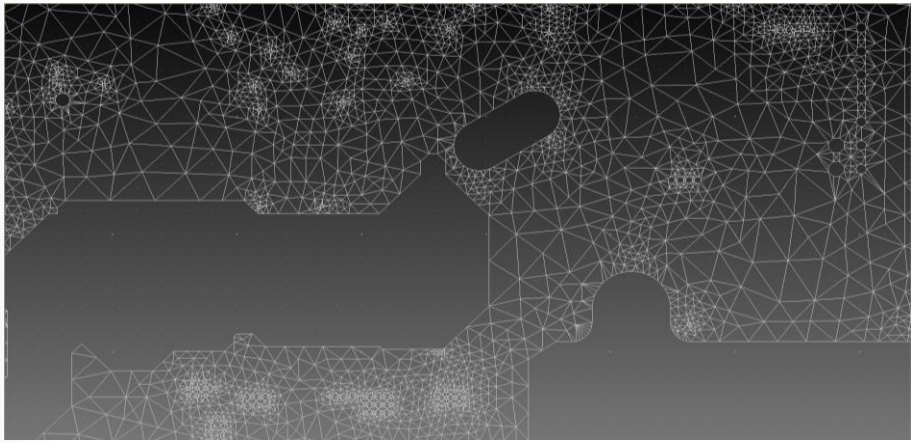
- DC Current Density Plots



- Via and Bondwire Modeling



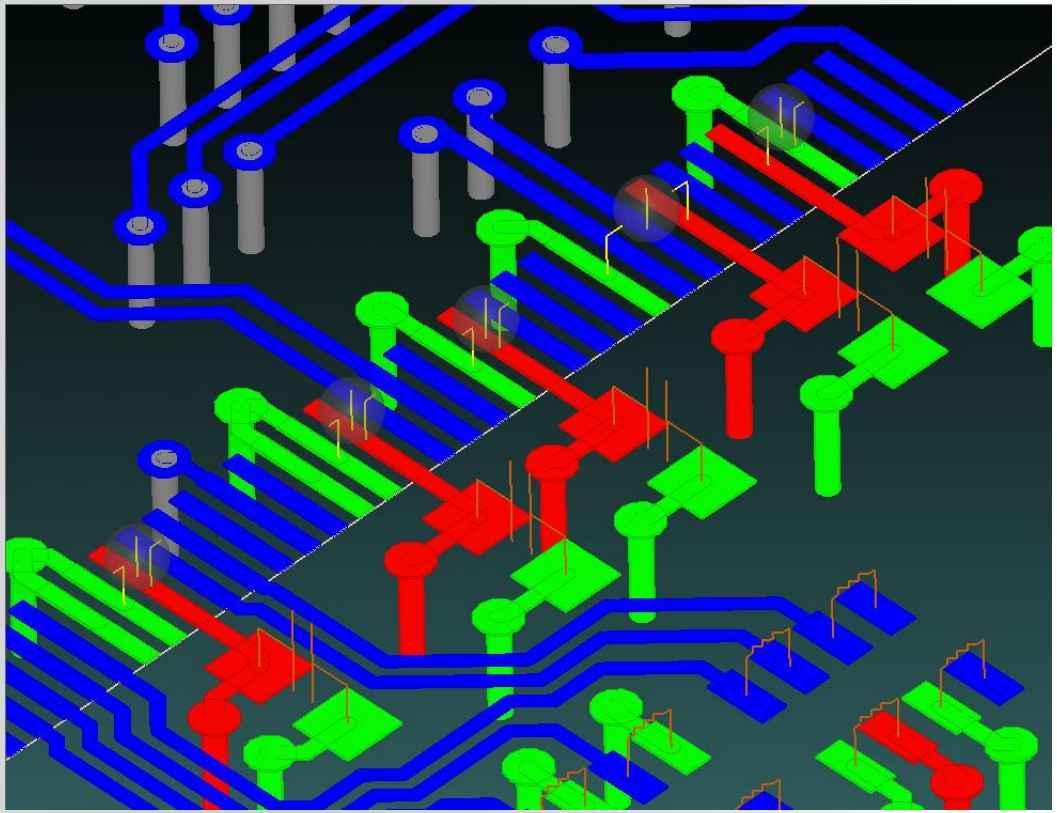
- Adaptive Mesh Refinement



I2R Drop

- Place voltage source at VRM location
- Setup current sources at all IC loads;

Pin by Pin or Total Current



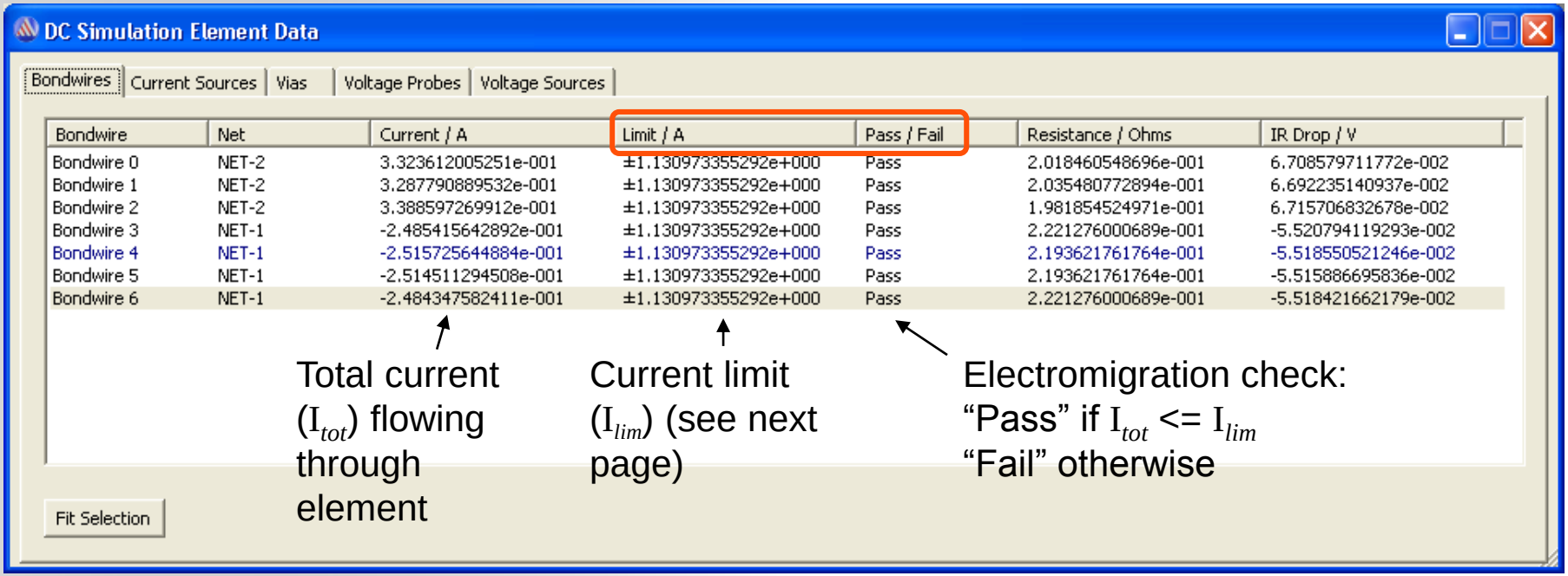
DC Simulation Element Data

Bondwires | Current Sources | Vias | Voltage Probes | Voltage Sources

Probe Name	Value / V
VPROBE_U0200_AA27_1	1.032994422649e+000
VPROBE_U0200_Y28_1	1.033036287815e+000
VPROBE_U0200_AB28_1	1.033378295162e+000
VPROBE_U0200_AA29_1	1.033424868080e+000
VPROBE_U0200_V20_1	1.034408546710e+000
VPROBE_U0200_Y22_1	1.034414785251e+000
VPROBE_U0200_Y24_1	1.034480893074e+000
VPROBE_U0200_Y20_1	1.034496852552e+000
VPROBE_U0200_AA23_1	1.034588522646e+000
VPROBE_U0200_W19_1	1.034604139185e+000
VPROBE_U0200_AA21_1	1.034612264663e+000
VPROBE_U0200_V18_1	1.034627139438e+000
VPROBE_U0200_AA25_1	1.034726999829e+000
VPROBE_U0200_AB22_1	1.034773167804e+000
VPROBE_U0200_Y18_1	1.034792394522e+000
VPROBE_U0200_AA19_1	1.034815780404e+000
VPROBE_U0200_AB24_1	1.034844478055e+000
VPROBE_U0200_AB20_1	1.034856579405e+000
VPROBE_U0200_AB18_1	1.035152306565e+000
VPROBE_U0200_AA17_1	1.035207524112e+000
VPROBE_U0200_Y16_1	1.035252125032e+000
VPROBE_U0200_AB16_1	1.035587041452e+000
VPROBE_U0200_AA15_1	1.035891159874e+000
VPROBE_U0200_Y14_1	1.036026698599e+000
VPROBE_U0200_Y30_1	1.036086352598e+000
VPROBE_U0200_AB14_1	1.036338998195e+000
VPROBE_U0200_AB30_1	1.036409611440e+000
VPROBE_U0200_V22_1	1.036504100767e+000
VPROBE_U0200_AA31_1	1.036531319396e+000

Verify min/max voltages at all loads

Elctromigration



Bondwire	Net	Current / A	Limit / A	Pass / Fail	Resistance / Ohms	IR Drop / V
Bondwire 0	NET-2	3.323612005251e-001	±1.130973355292e+000	Pass	2.018460548696e-001	6.708579711772e-002
Bondwire 1	NET-2	3.287790889532e-001	±1.130973355292e+000	Pass	2.035480772894e-001	6.692235140937e-002
Bondwire 2	NET-2	3.388597269912e-001	±1.130973355292e+000	Pass	1.981854524971e-001	6.715706832678e-002
Bondwire 3	NET-1	-2.485415642892e-001	±1.130973355292e+000	Pass	2.221276000689e-001	-5.520794119293e-002
Bondwire 4	NET-1	-2.515725644884e-001	±1.130973355292e+000	Pass	2.193621761764e-001	-5.518550521246e-002
Bondwire 5	NET-1	-2.514511294508e-001	±1.130973355292e+000	Pass	2.193621761764e-001	-5.515886695836e-002
Bondwire 6	NET-1	-2.484347582411e-001	±1.130973355292e+000	Pass	2.221276000689e-001	-5.518421662179e-002

Total current (I_{tot}) flowing through element

Current limit (I_{lim}) (see next page)

Electromigration check:
"Pass" if I_{tot} <= I_{lim}
"Fail" otherwise

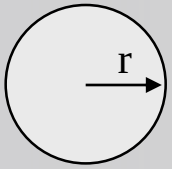
- **Globally scan all vias and bondwires**
- **Reduce current density by adding additional vias to vicinity**

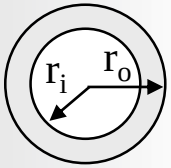
Bondwire/Via Current Limit

Define current limit (Ilim) as value above which electromigration is likely to be a problem

Computed using simple Ilim = tA formula

- **t (A/m2): user-editable value in "dc_coeff.txt" (located in the SIwave V5 installation directory)**
- **A: cross-sectional area of conductor**



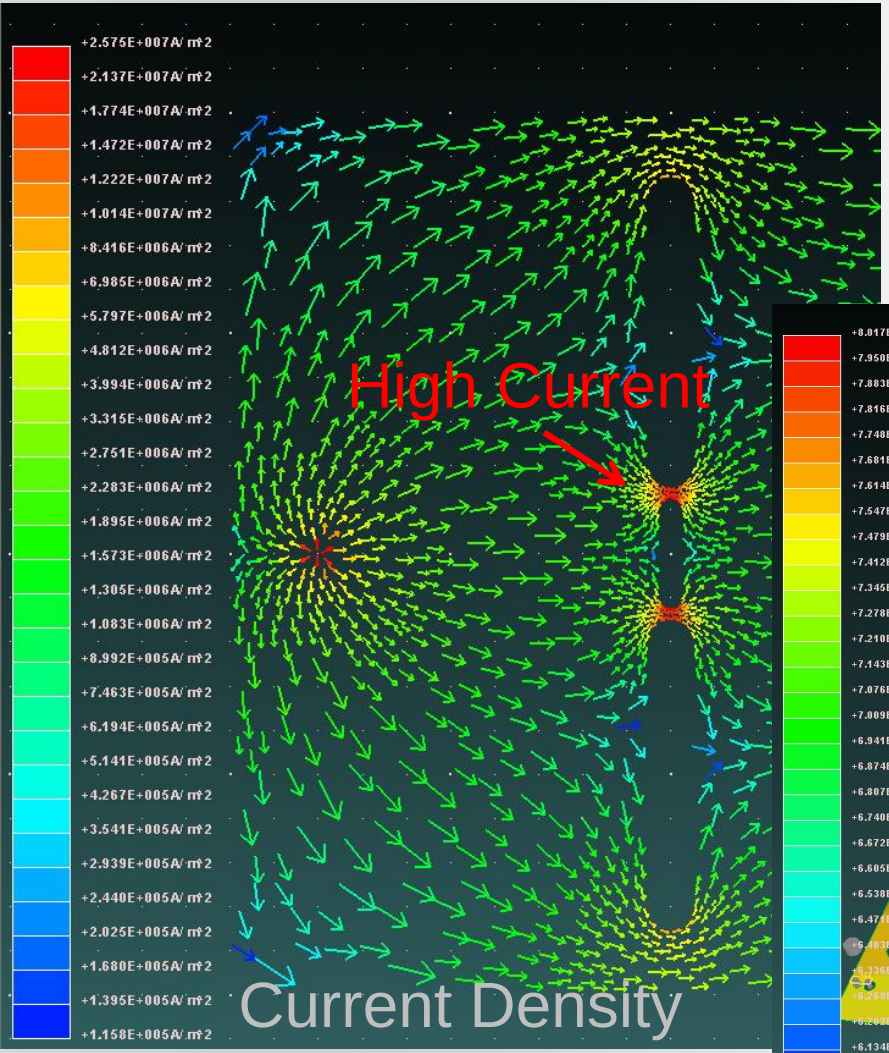


Bondwire: $A = \pi r^2$ Via: $A = \pi(r_o^2 - r_i^2)$

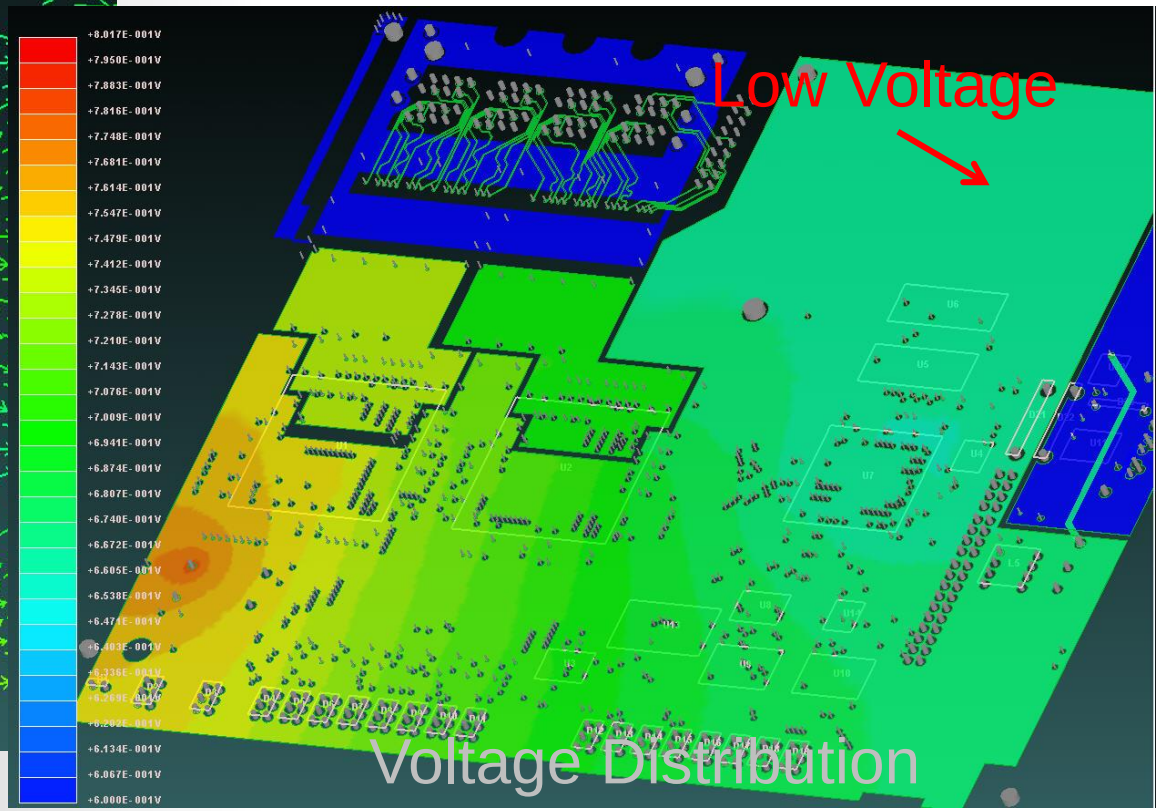
```
# Ansoft Corporation
#
# SIwave DC Current Coefficients
#   User-controllable values specified herein are used to set the
#   maximum legal current magnitude in bondwires, solderballs,
#   solderbumps and vias
#
# Note: all values (except METAL_VOLTAGE and METAL_POWER) are in A/m^2
#       METAL_VOLTAGE is in volts
#       METAL_POWER is in W/m^2

BONDWIRE 900e6
SOLDERBALL 6e6
SOLDERBUMP 60e6
VIA 90e6
METAL_VOLTAGE 3.0
METAL_CURRENT 5e6
METAL_POWER 5e4
```


Bottlenecks



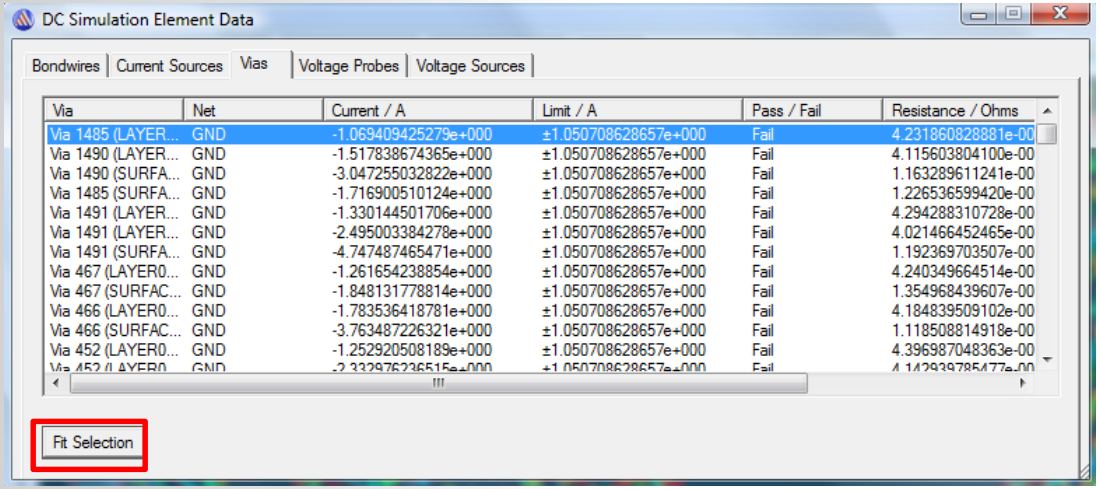
Visualize where design improvements could be made

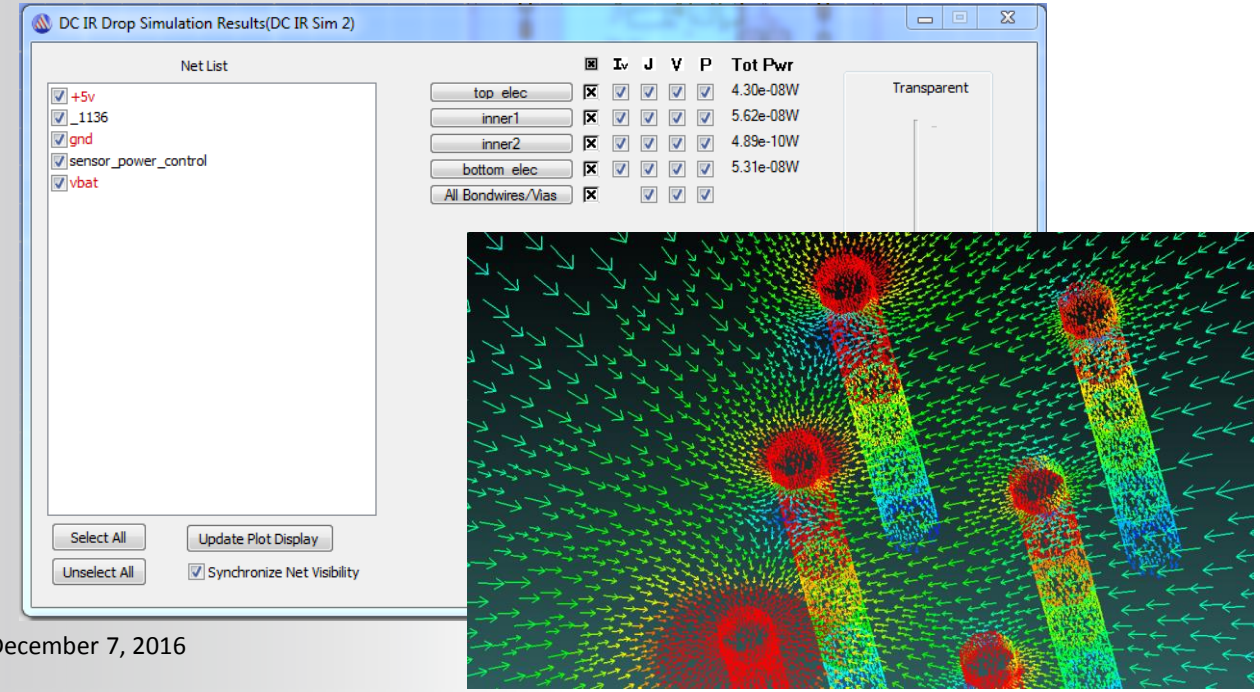


SIwave - Zoom to problem Areas

Visualize Current on all layers to help determine a solution

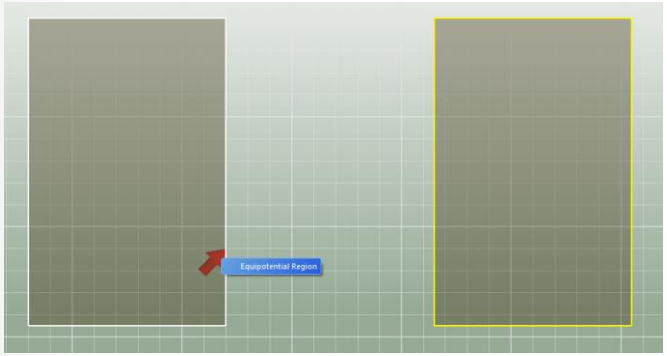
INCLUDING The GND RETURN PATH





Define Equipotential Regions for DC IR

- Equipotential regions are used by the DC IR drop solver to force equal voltage across a specified region, including specified pads.
- To define equipotential regions, click **Draw>Equipotential Regions**
- The cursor is activated to draw a rectangle. Use the menu selection to draw one or more regions on the Top or Bottom of the layout.
  - Hide all layers to see the regions



- Use the Delete All Regions button to erase any previously-defined regions

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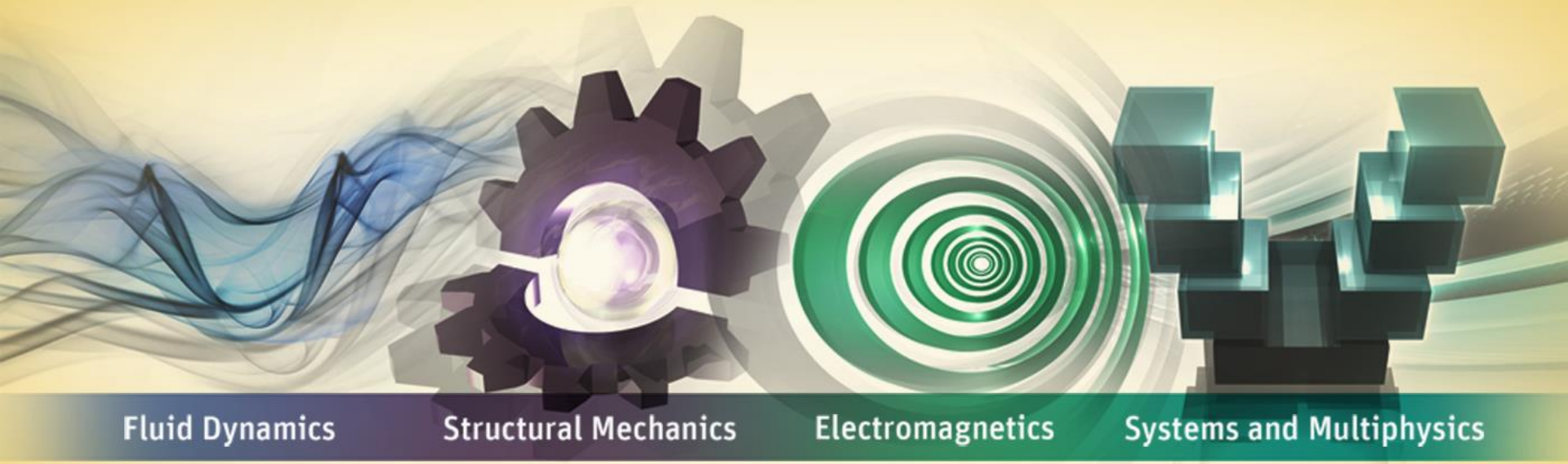
Resonant Modes Analysis



Resonance Simulation

Eigenmode analysis identifies location and frequency of natural cavity resonances that exist between planes

Scans entire PCB/PKG on all layers

If a resonance is excited, Signal Integrity can be compromised :

- High Z, null in S21, EMI etc.

Resonances should be moved away from critical parts and outside operating frequency

Reducing Resonance :

- Resonances always exist but you can reduce their impact by:
  - Changing the decoupling scheme
  - Changing the stackup
  - Changing plane dimensions
  - Adding via stitching
  - Moving discrete parts

Resonance Simulation : Rectangular Cavity

Structure: two metal planes, 60mm x 40mm

Dielectric: FR4 (er = 4.4, tan d = 0), 1 mm thick

Analytic solutions for voltage at resonance:

$$v(x,y) = \cos(n\pi x/a)\cos(m\pi y/b) \qquad n,m = 1,2,3,\ldots$$

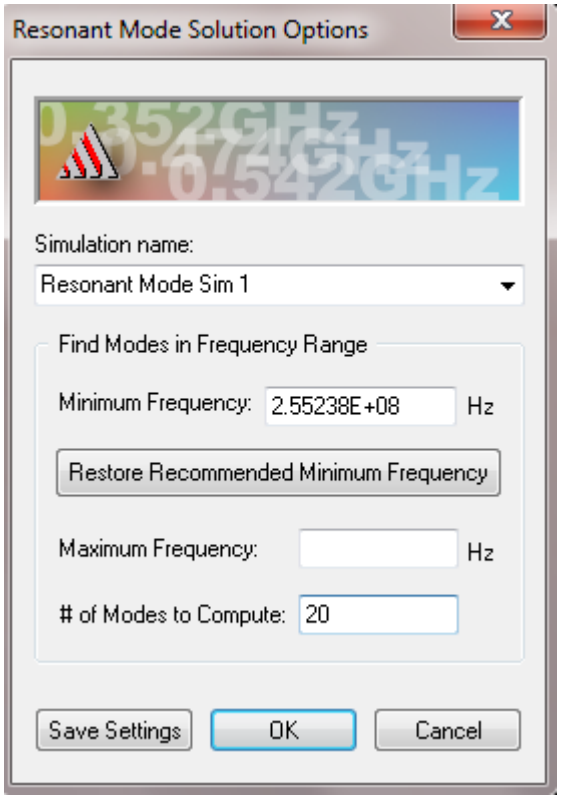
Analytic solutions for resonance frequencies:

$$f_{nm} = \frac{c}{\lambda_{mn}} = \frac{c_0}{2\sqrt{\varepsilon_r}}\sqrt{\left(\frac{n}{a}\right)^2 + \left(\frac{m}{b}\right)^2}$$

m,n	SIwave (GHz)	Analytic (GHz)
1,0	1.192615376	1.19182823655
0,1	1.790103257	1.78774235483
1,1	2.154560548	2.14859890922
2,0	2.397284602	2.38365647311
2,1	3.000732847	2.97957059139

SIwave Resonance Analyse

- **Easy setup, no sources are required. To solve the resonant mode of the cavity using the Eigenmode solver :**
  - Simulation > Compute Resonant Modes.
  - Enter the value for Minimum Frequency.
  - Enter the value for Maximum Frequency.
    - You can leave this field blank.
  - Specify the # of Modes to Compute.
    - The modes indicate the frequencies at which the cavity responds very strongly. This determines the voltage pattern between the top and bottom planes.
  - OK



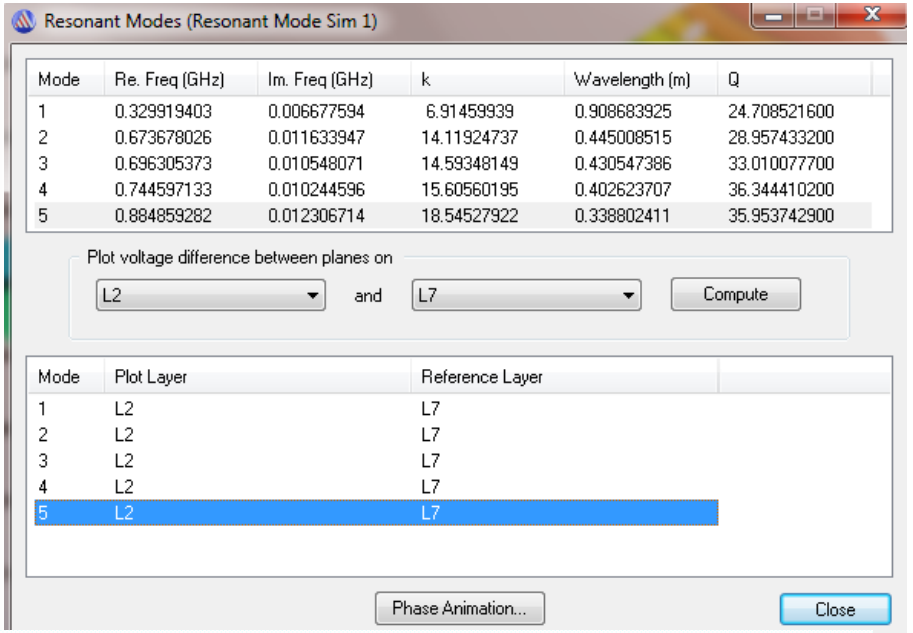
Resonance Mode results

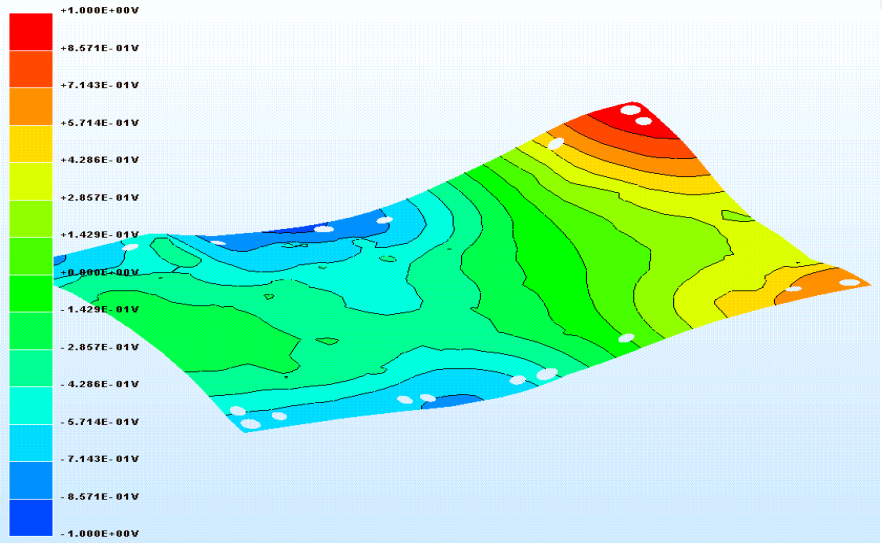
Each mode is computed as well as several parameters.

- Re{f} corresponds to the frequency at which it will oscillate.
- Im{f} corresponds to the loss
- Wavelength(in vacuum) = c / Re{f}
- K = 2*pi / Wavelength
- Q = Re{f} / (2*pi*Im{f})

Display Voltage distribution between planes at resonance

- Red and blue areas indicate high impedances at a particular frequency
- Viewing Phase Animation
  - Select Metals plane
  - Compute
  - Generate Frames





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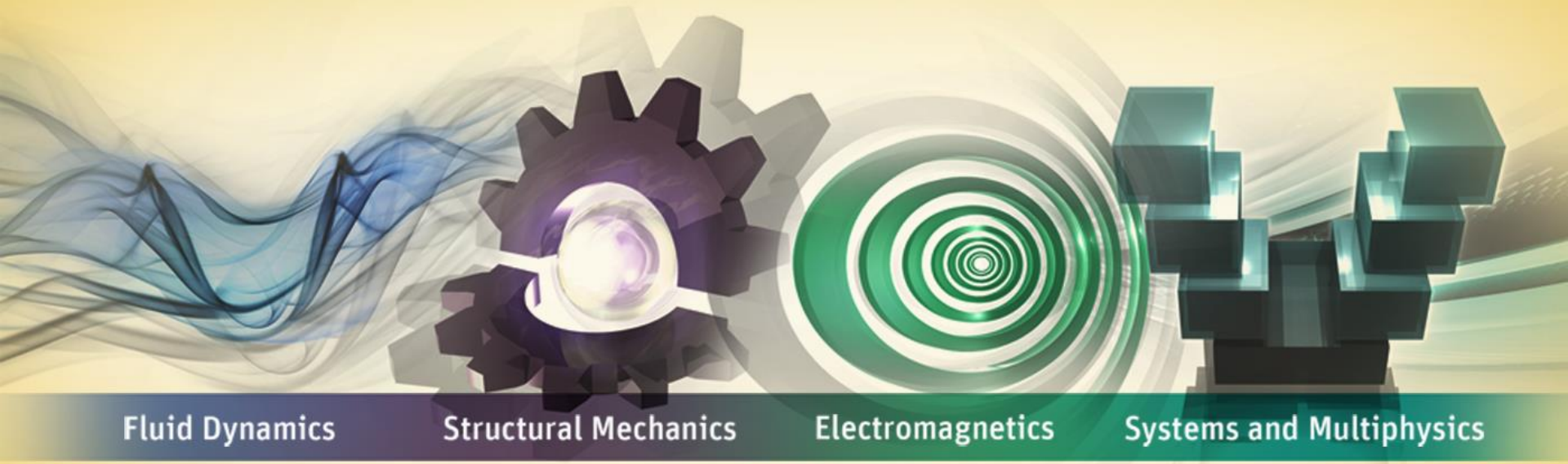
Frequency Sweep Analysis



Frequency Sweep Analysis Review

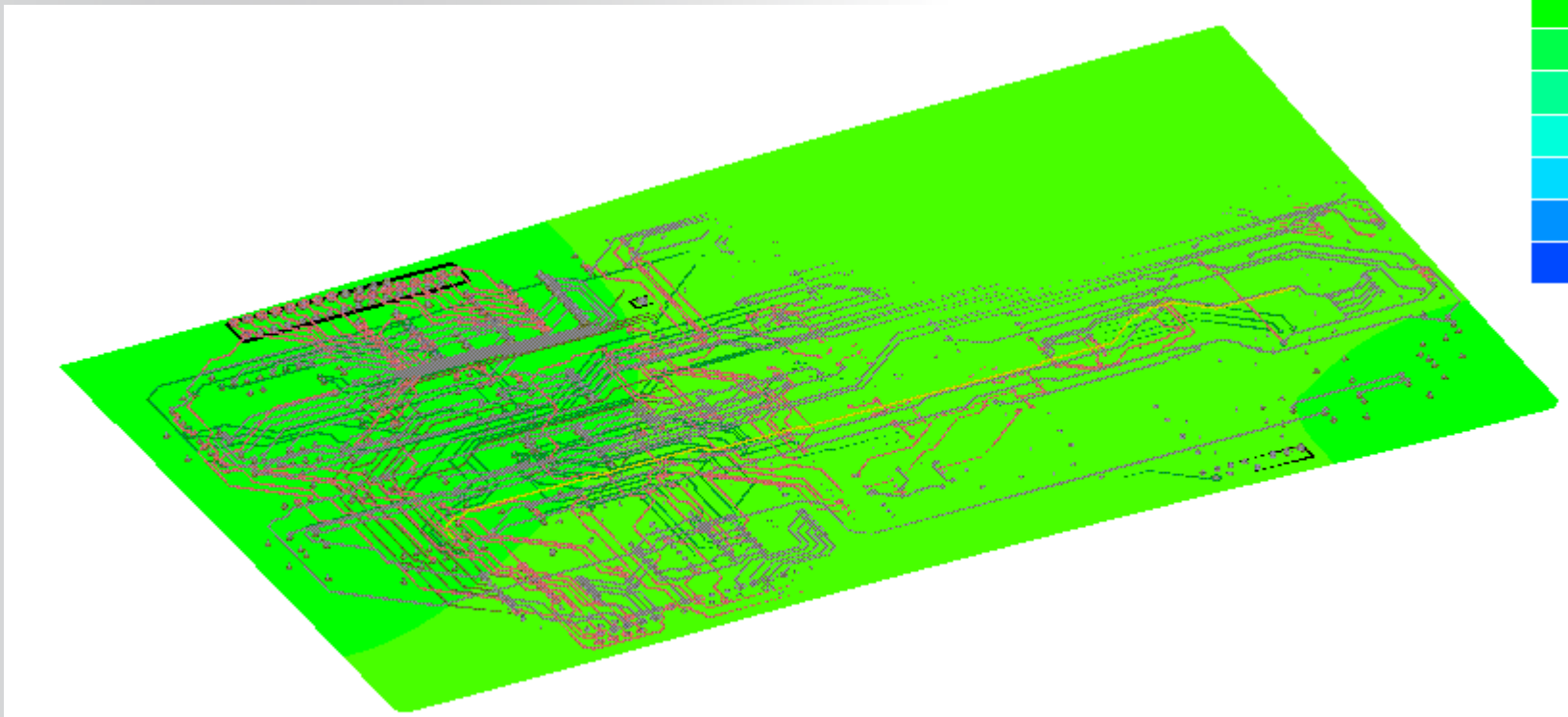
- Although resonant modes are inevitable, they may or may not be excited depending on the location of the source.
- With the Frequency Sweep Analysis, the designer can excite the design in specified locations and see the aggregate response of all the resonant modes of the board for the given source location.
  - Verify maximum IR drop across frequencies

SIwave Analyses

Frequency Sweep

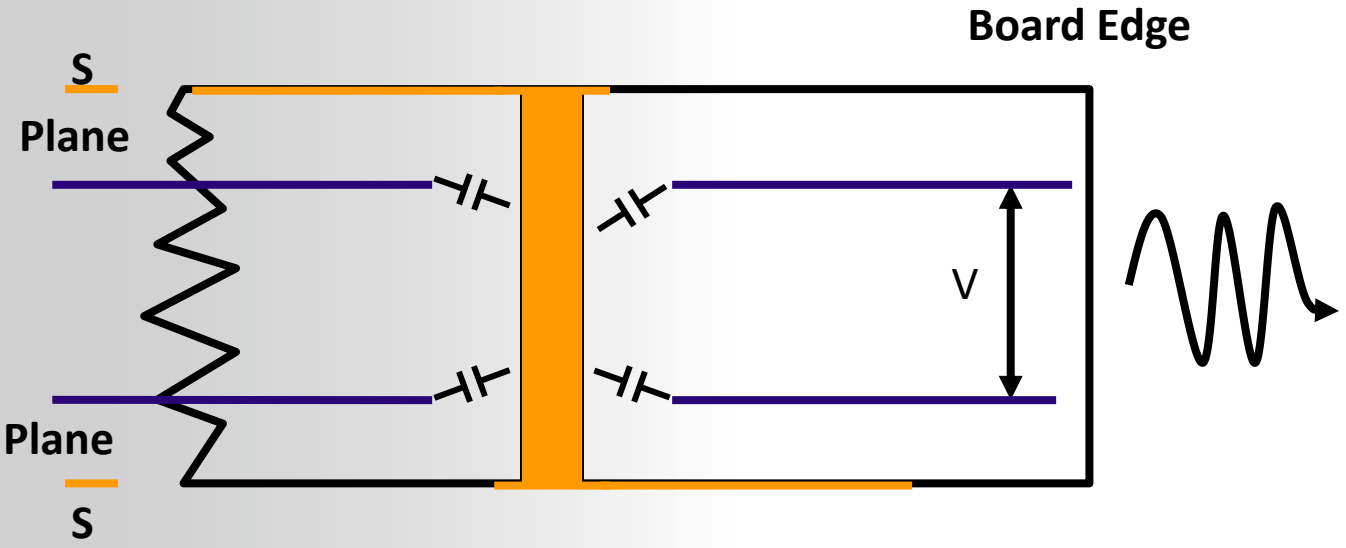
- Current or voltage sources
- Voltage distribution at all desired frequencies.
- Voltage probes for quantitative dependence.

Sweep from DC to 2 GHz



Why Resonances Mode Analysis?

- Return path current is disrupted at the via.
- Signal vias couple to the planes.
- Creates a feed for the parallel plate waveguide.



Simple SIwave Experiment

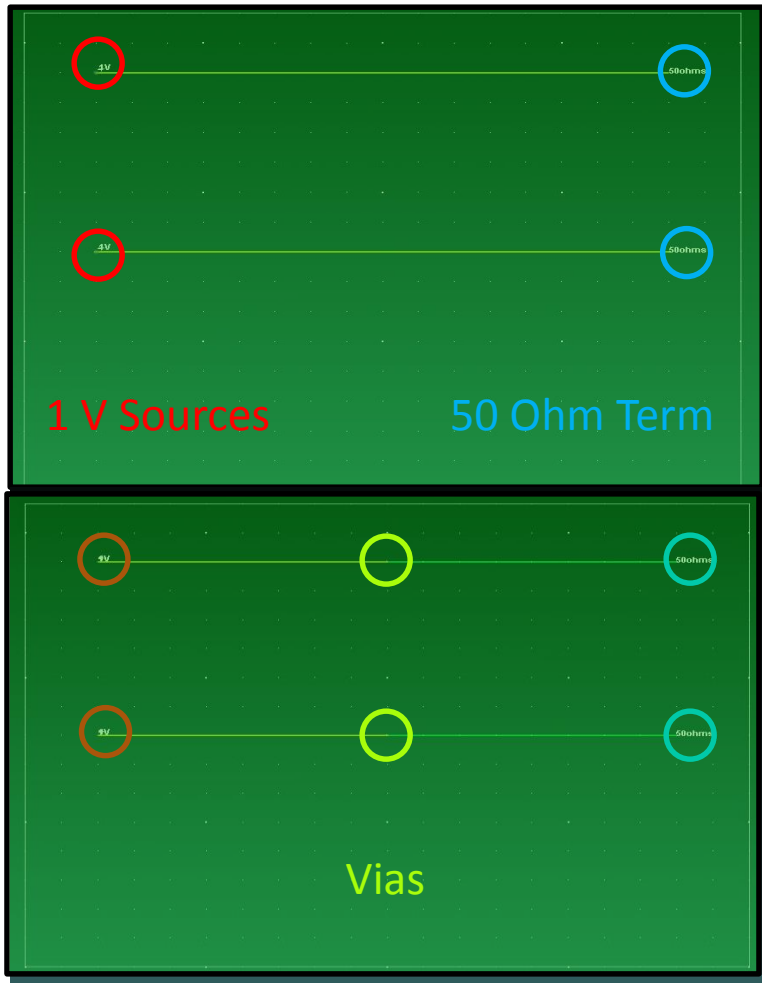
4 Layer 8x10” PCB

Control Case :

- **Microstrip transmission line without a via transition**

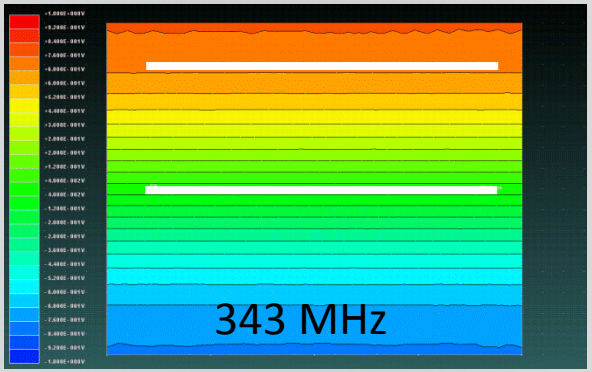
Test Case :

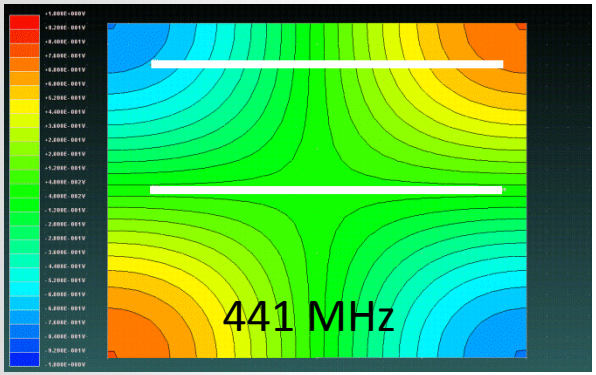
- **Same length transmission line with a via transition from top to bottom**

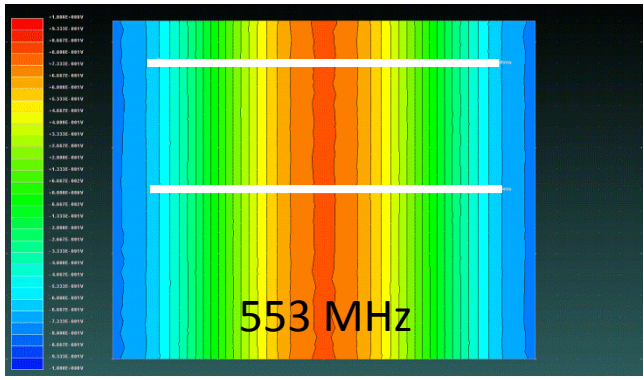


Resonance Results

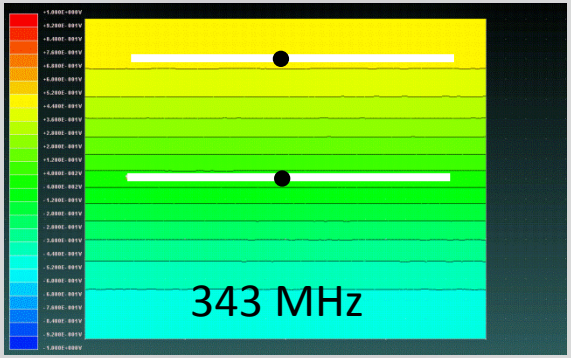
Control Case

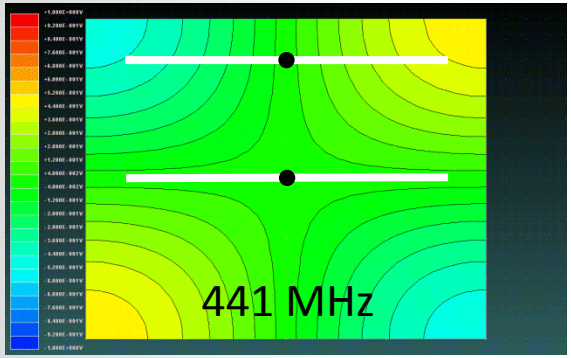


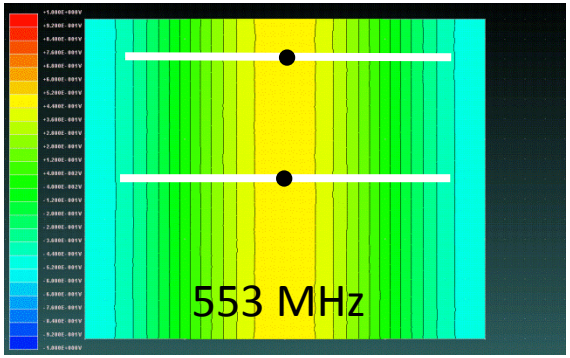




Test Case

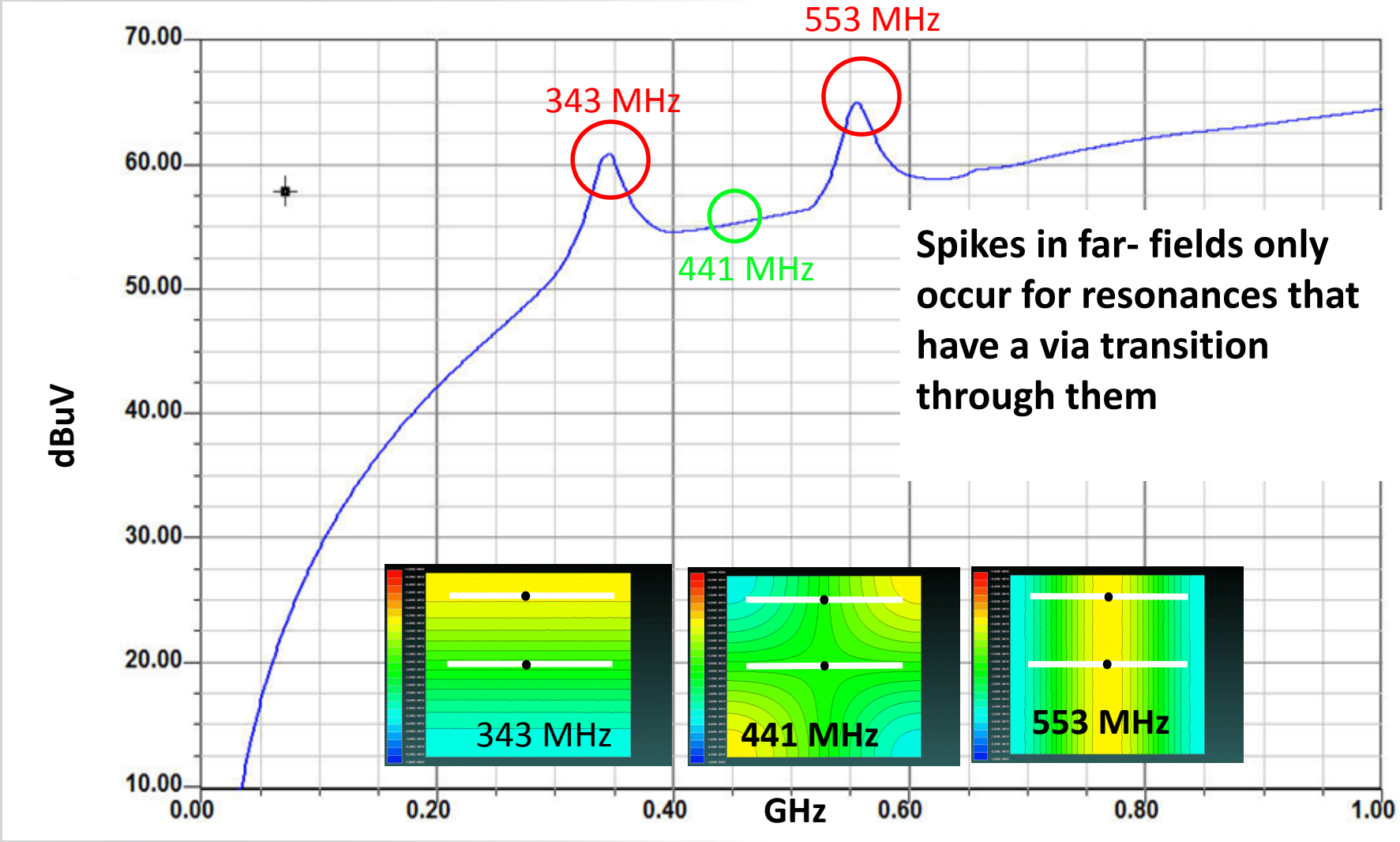






- **The blue and the red represent the resonance points. Where green has no resonance.**

Far Fields at 3 Meters



Spikes in far- fields only occur for resonances that have a via transition through them

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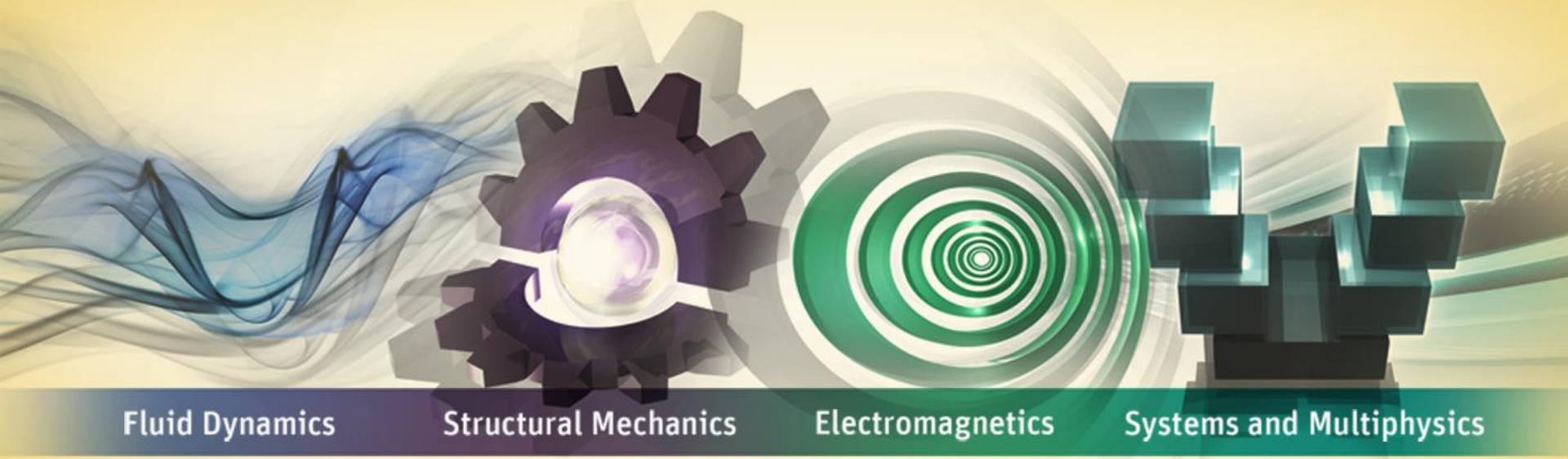
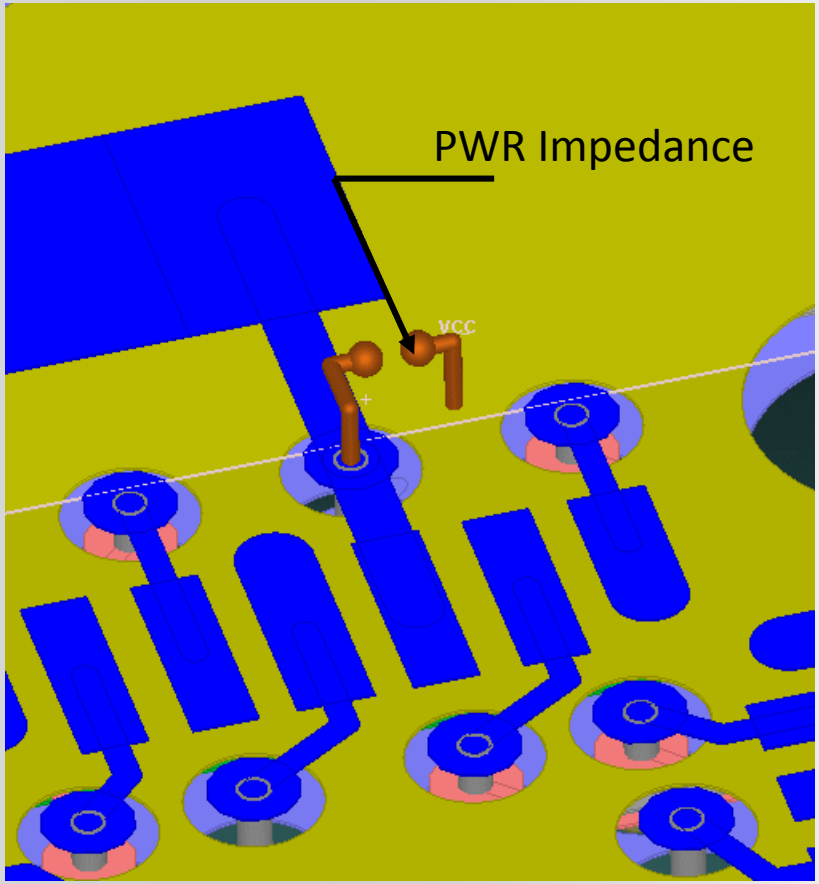
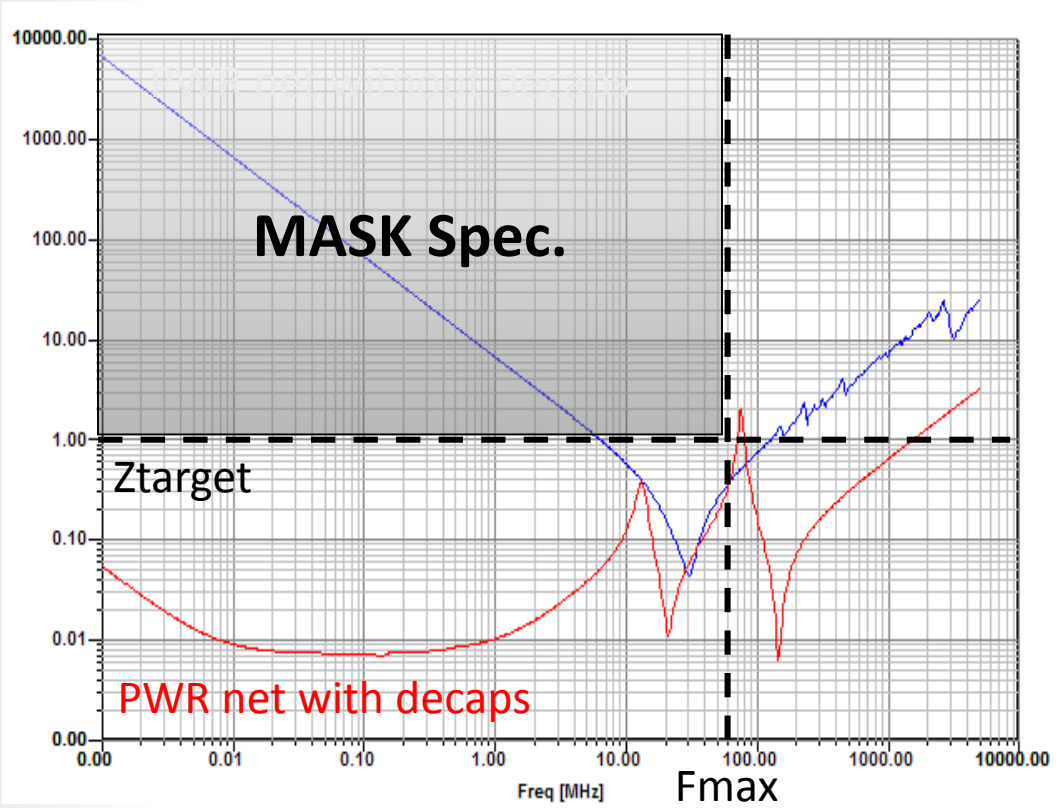
Computing Impedance of PDN using S-,Y-, Z- Analysis



Plane impedance Simulation

- Same setup as S-Parameter extraction. Place ports in locations of interest. Pin Grouping can be useful
- Verify low impedance up to device cut-off frequency



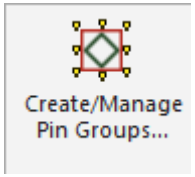


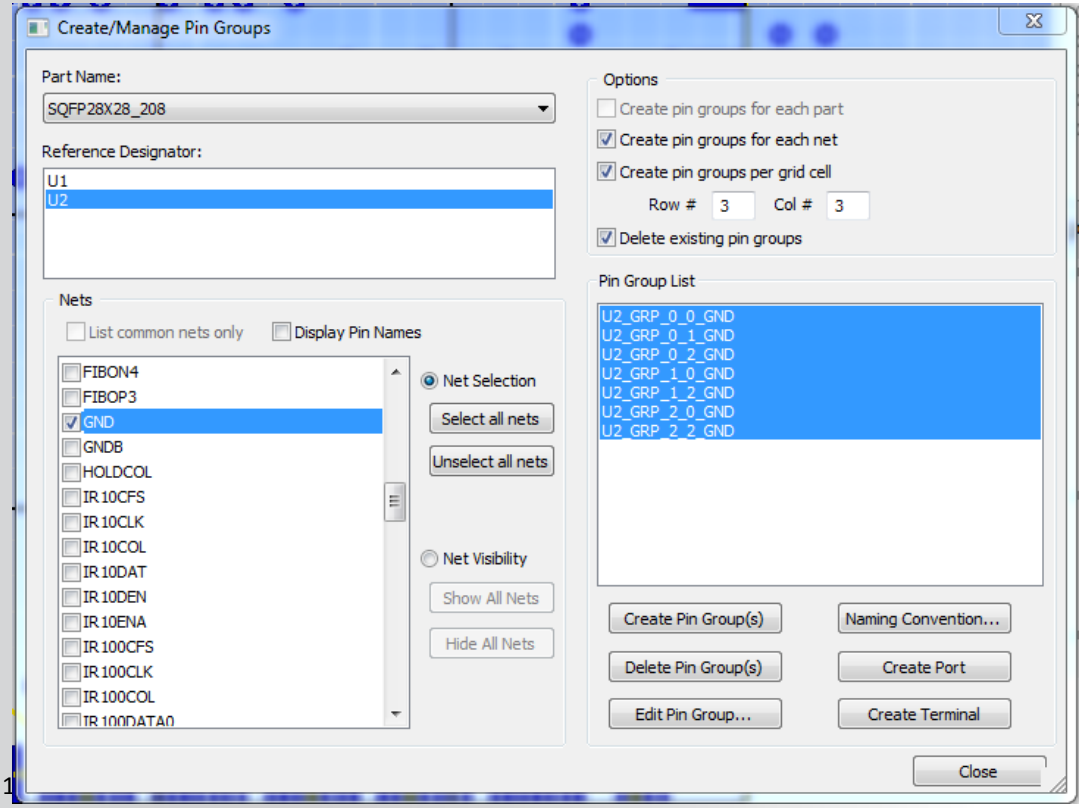
SIwave : Grouping Pins

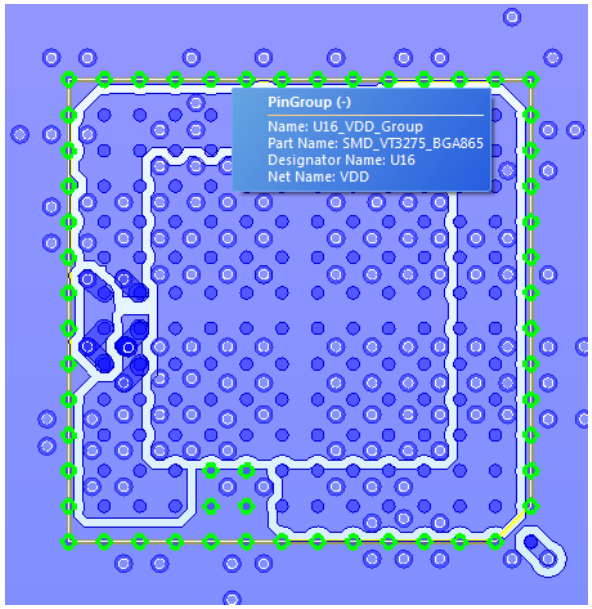
You can create pin groups for various components. The grouped pins will be treated as if they were electrically connected during the analysis.

You can use this pin group to create ports

- **Tools > Create/Manage Pin Groups...**
- **Double click on the IC component in the 3D modeler**





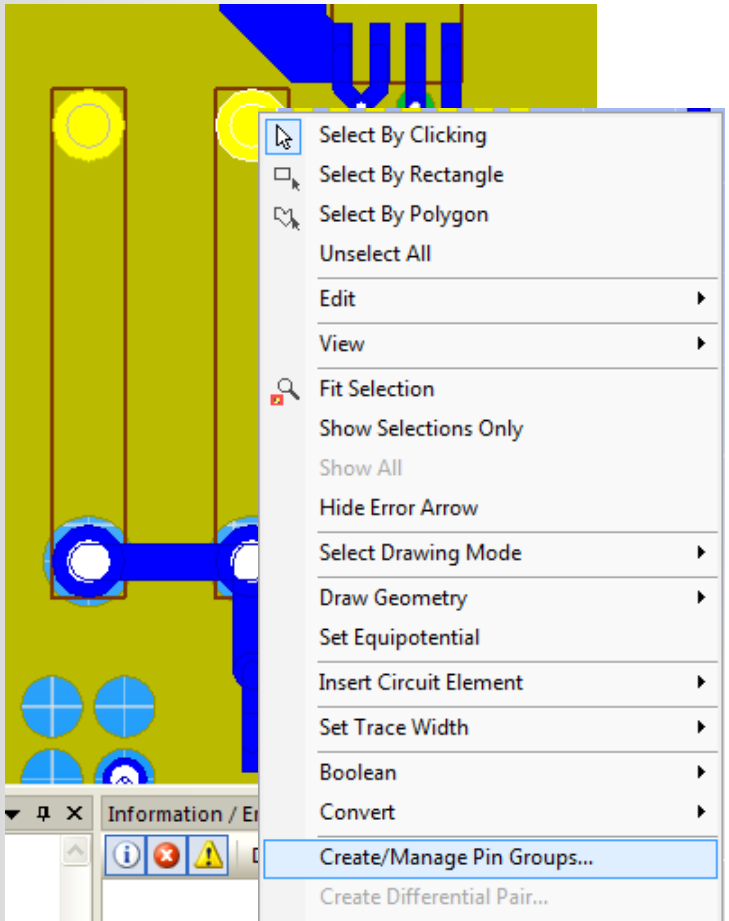


Pin grouping port between different components

Create a Pin Group from multiple components:

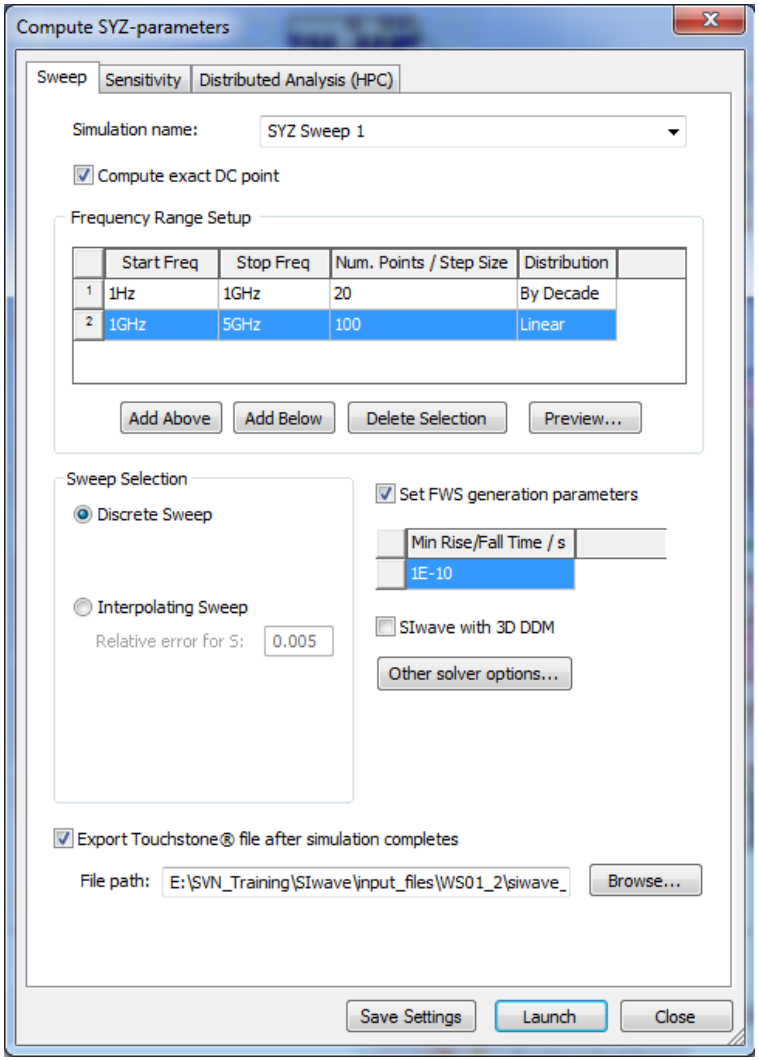
Multi-select Pins in GUI

- **RT click -> Create/Manage Pin Groups…**



S-,Y-, Z- Analysis

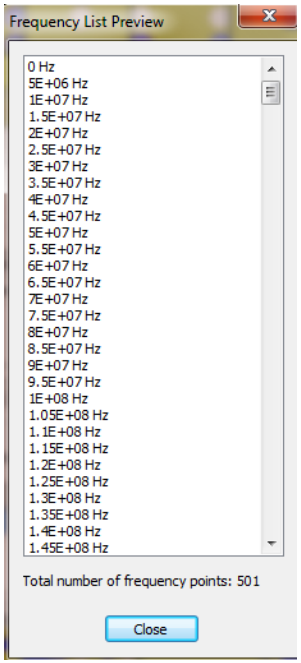
- To extract S, Y and Z matrix for the predefined ports :
  - Simulation > Compute S-,Y-,Z-parameters
  - Enter the value for Start Frequency.
  - Set the stop frequency or rise time information
    - (Frequency Bandwith= 0.5/min rise time)
  - Specify the Number of Solution Points.
  - Select the method for distributing points
  - Choose the sweep Selection
    - Discrete sweep
    - Interpolating sweep



Frequency Sweep Selection box

Discrete Sweep :

- All frequency points in the list are solved. Look at the Frequency List Preview.



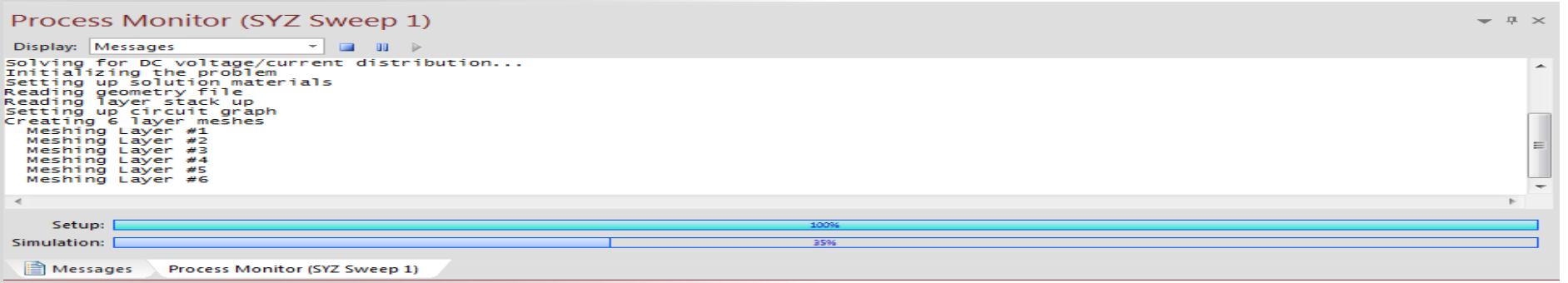
Interpolating Sweep :

- Following an Error tolerance, an interpolating sweep estimates a frequency response for an entire frequency range by solving at a relatively small number of frequency points within that range. Between the actual solution frequencies, the frequency response is obtained by rational interpolation. SIwave adaptively chooses the frequency points at which it computes the field solution. After a new frequency point is solved, a new interpolating fit is generated. This is compared to the interpolant from the previous step, and the maximum difference between the two is determined. If the difference exceeds the requested tolerance, then a new frequency point is chosen for a solution. The interpolating sweep is complete when the difference between successive interpolants is less than the error tolerance criterion.

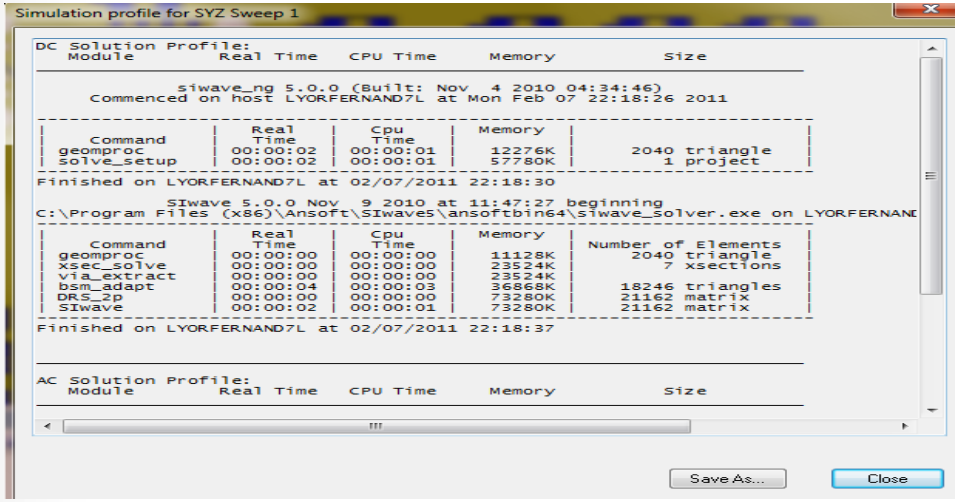
Optionally, to save these settings and use them for subsequent simulations, click the Save Settings button

Simulation Profile

- During simulation, in the Process Monitor workspace, you can follow the simulation progress. profile, monitoring the real time, CPU time, memory requirements and view the matrix informations.



- When the simulation is done, the profile is available with real time, CPU time, memory requirements and view the matrix informations.
- Results > Analysis Name > View profile



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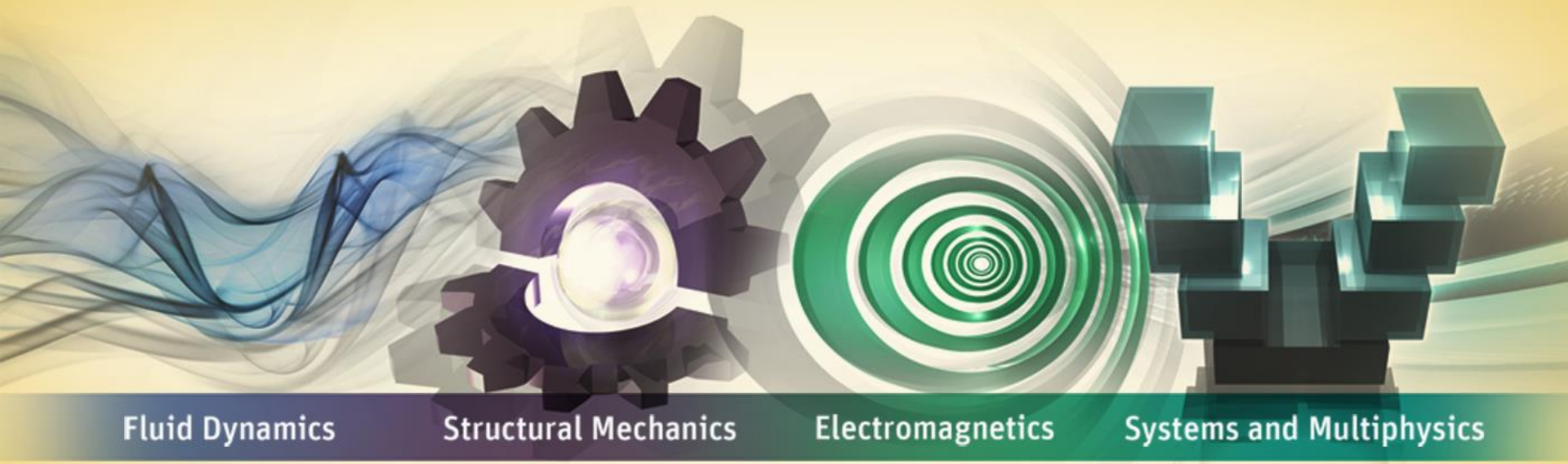
Sensitivity Analysis



Sensitivity Analysis

Sensitivity analysis computes the derivative of a circuit response (an S-, Y- or Z-parameter) with respect to the impedance of a circuit element, typically a decoupling capacitor.

Therefore it is a measure of how much that output parameter will change in response to a change in the circuit element.

- A low sensitivity indicates that the circuit element has little influence on the circuit response of interest
- A high sensitivity indicates that the response is a strong function of the circuit element.

This information can help a designer to identify which circuit elements need to be adjusted to improve a circuit response. It can be used to find unnecessary decoupling capacitors--ones that aren't affecting the results significantly. It can also help to identify which circuit elements need loose or tight tolerances.

Sensitivity Analysis

- **Advantages :**
- **Sensitivity analysis can be computed very quickly for a large number of circuit elements once you have solved for the nominal S-parameters.**
- **Using the built-in sensitivity analysis capability, you can reduce that time to a small fraction (perhaps 5%) of the analysis time for the nominal problem. It is essentially "free" information**

Sensitivity Analysis in details

The software internally computes the derivative the circuit responses that you designate with respect to the impedance of the circuit elements you choose. To make this more concrete, suppose you pick an Sparameter *Sij* and a capacitor *C* . The impedance of the capacitor is *Zc=jwC* . So the software computes the derivative, *dSij/dZc*.

This "raw" derivative is then normalized as follows to make it easier to interpret:

$$\text{normalized sensitivity} = \frac{dS_{ij}}{dZ_c} \cdot \frac{Z_c}{S_{ij}} = \left(\frac{dS_{ij}}{S_{ij}}\right) / \left(\frac{dZ_c}{Z_c}\right)$$

- **As shown in the formula above, the normalized sensitivity can be interpreted as the ratio of the fractional change in the output parameter to the fractional change in the impedance of the circuit element. So if the normalized sensitivity is 10, that would indicate that a 1% change in the capacitor's impedance would result in a 10% change in the output S-parameter. Normalized sensitivity makes it easy to compare the sensitivities of circuit elements with widely varying impedances.**

- **The normalized sensitivity is a complex number. The software reports the magnitude of the normalized sensitivity, so what you see in the user interface is a real number.**

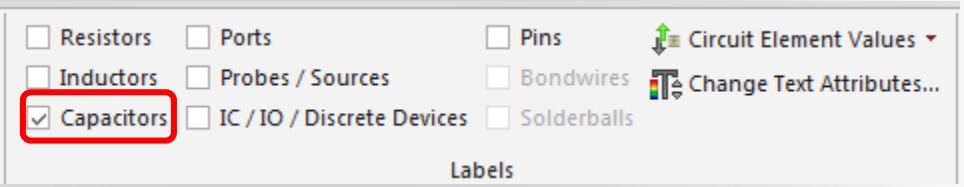
Capacitors Name Visibility

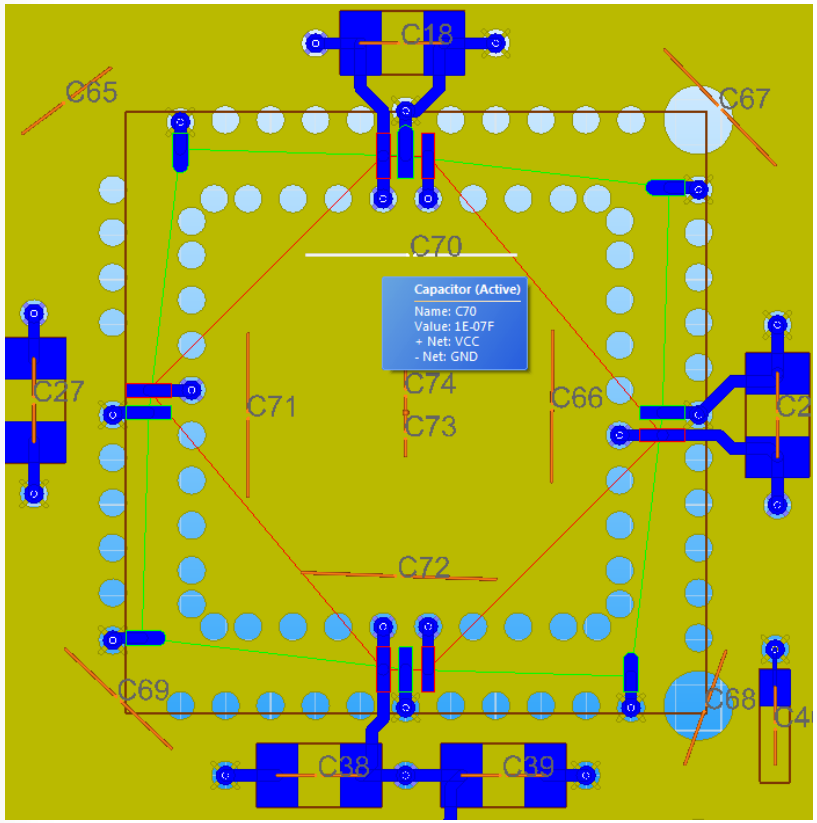
Change visibility settings for element names :

- Visibility > Labels > Capacitors

Adjust the size of the text

- Visibility > Labels > Change Text Attributes…

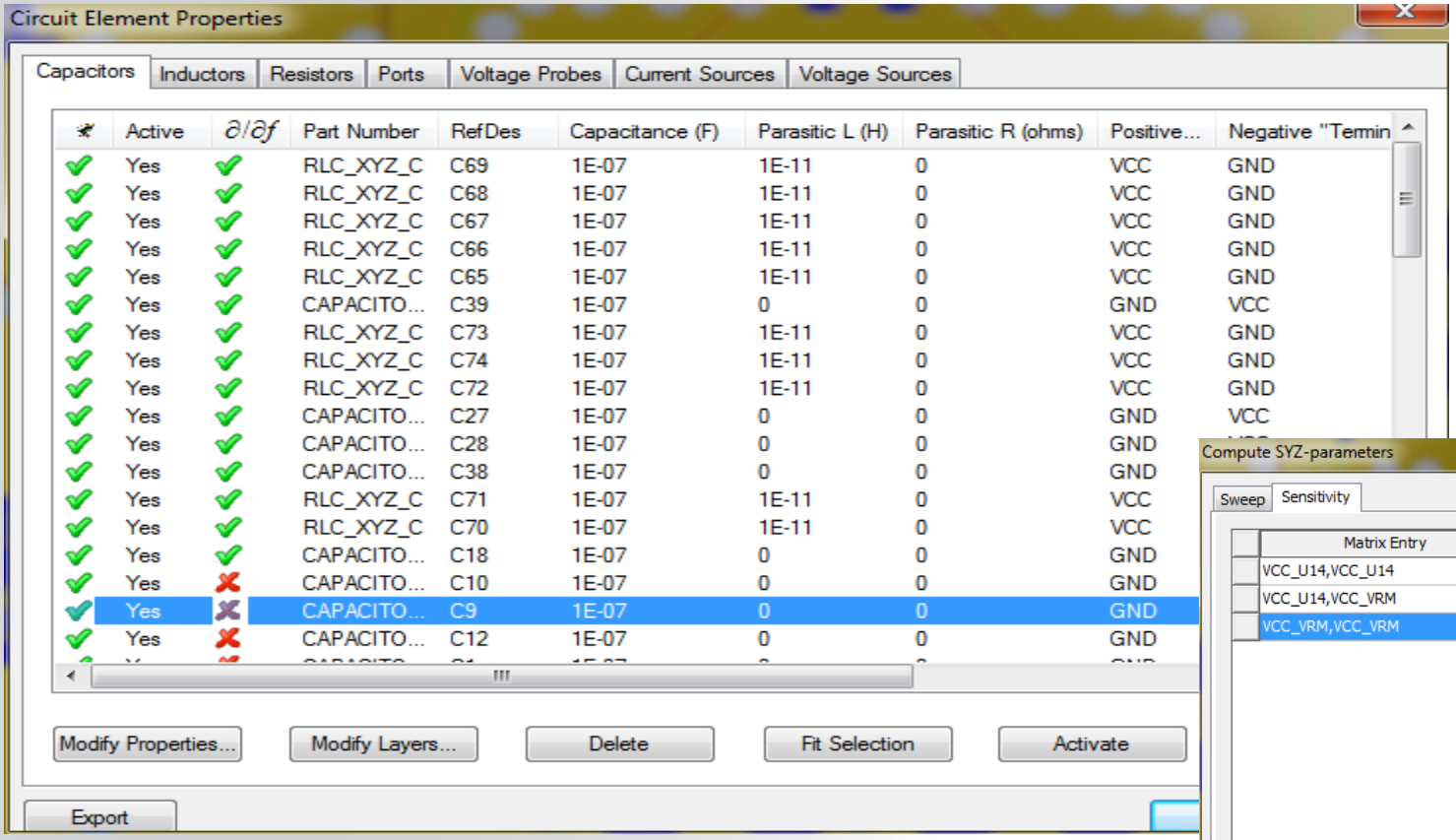


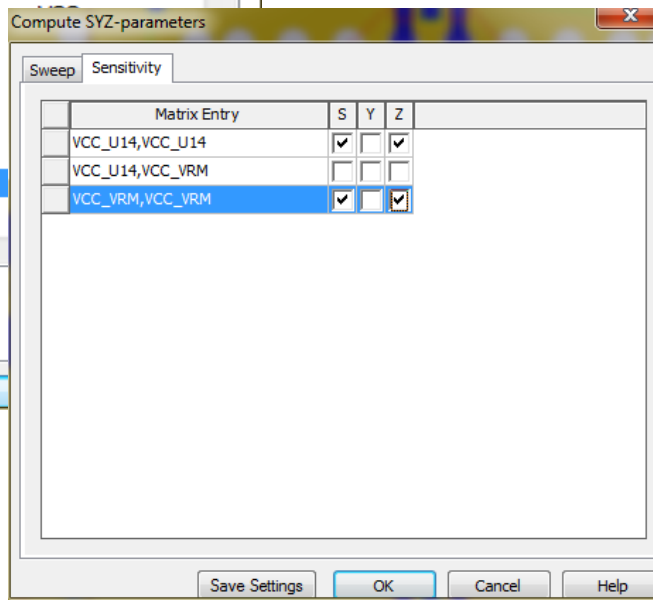


Set sensitivity computation for capacitors, inductors and inductors

Edit > Circuit Element Parameters.

- **Select capacitors that will be available for sensitivity analysis**



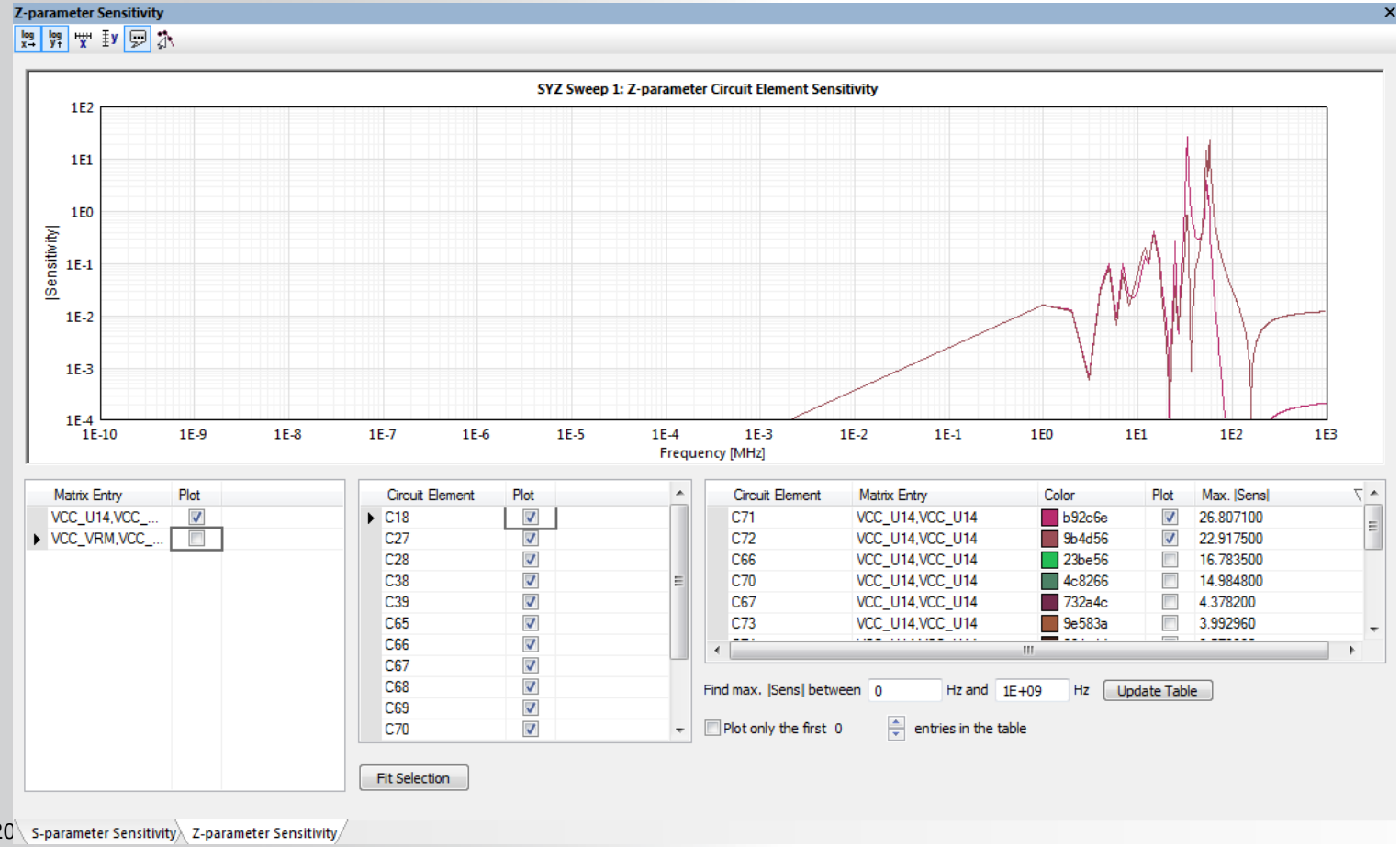


- **Simulation > Compute SYZ parameters**
- **Check Matrix entry in Sensitivity tab**

Results >SYZ > Plot Sensitivity

Here, the max normalized sensitivity is 26.8 for C71 :

- It indicate that a 1% change in the capacitor's impedance would result in a 26.8% change in the output Z-parameter.



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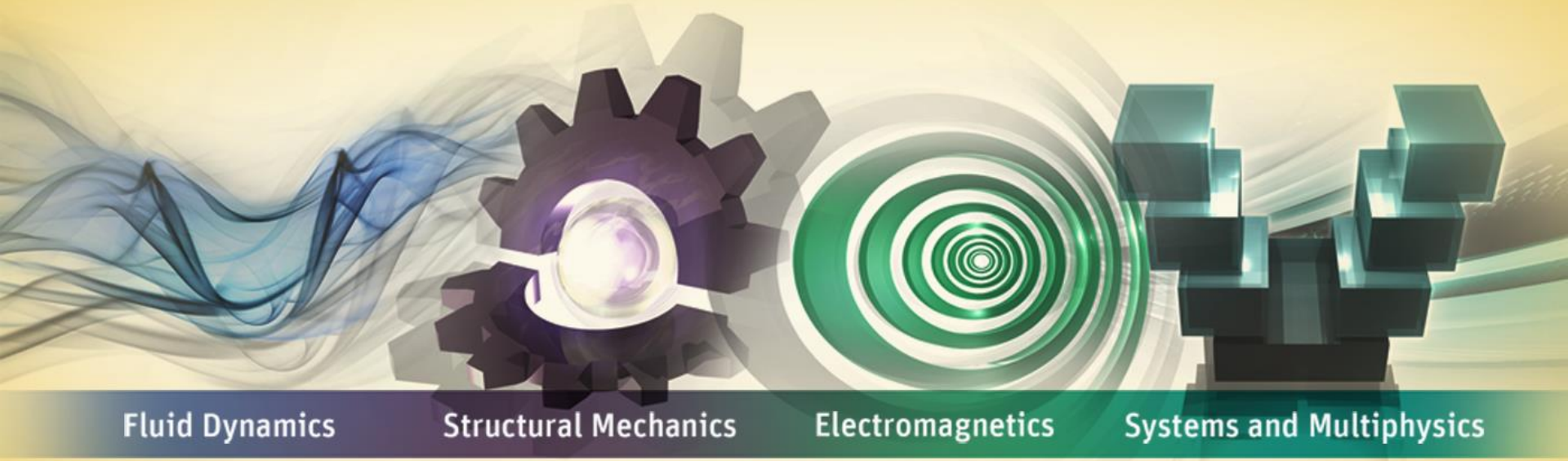
Power Distribution System & PI Methodology



Power Distribution System

PDS Design Goal:

- **Reduce noise in the power distribution system to a level that is acceptable for system performance.**

- **System Engineer**

$\Delta V(\omega)$ Acceptable Ripple Voltage

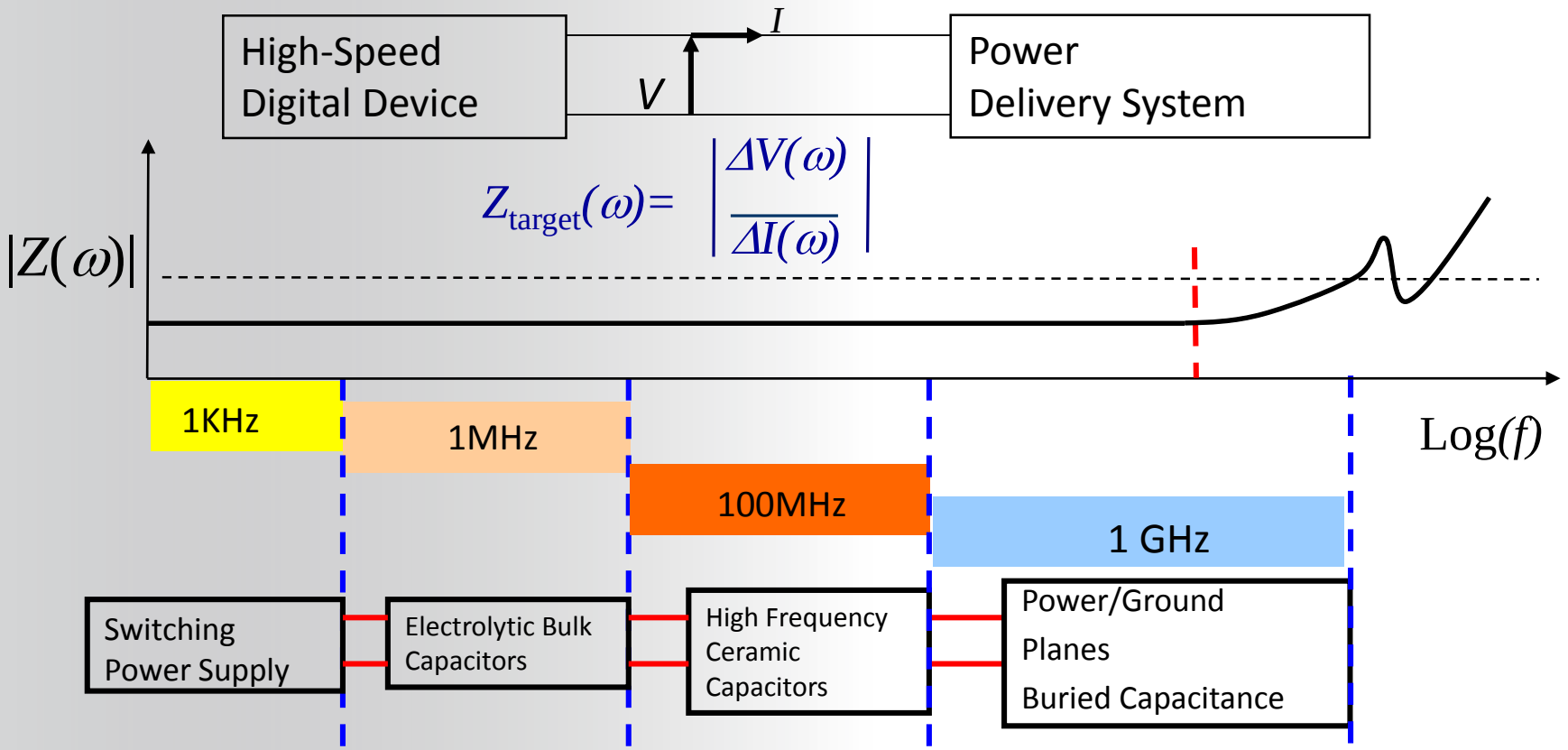
- **Active Device Current Spectrum**

$\Delta I(\omega)$ Current Spectrum

- **Power Distribution Impedance Specification**

$$Z(\omega) = \frac{\Delta V(\omega)}{\Delta I(\omega)}$$ **Target Impedance**

Target Impedance of PDS



1. The Impedance looks into PDS at the device should be kept low over a broad frequency range (from DC to package cut-off frequency)!
2. The Desired Frequency Range and Impedance Value is called Target Impedance.
3. Target impedance goal is set with the help of allowable ripple on the power/ground plane over a specified frequency range.

Target Impedance Calculation & Trends

$$Z_{\text{Target}} = \frac{(Power\_Supply\_Voltage) \times (Allowed\_Ripple)}{Current}$$

$$Z_{\text{Target(2.5v)}} = \frac{(2.5V) \times (5\%)}{40.3A} = 3.1m\Omega$$

- **Target Impendence is the goal that designers should hit!**

Year of first production	1997	1999	2002	2005	2008
Chip technology	0.25um	0.18um	0.13um	0.10um	0.07um
Across Chip Frequency (MHz)	450	600	800	1000	1100
Max. Chip Power (W)	100	120	140	160	180
Max current (A)	40.3	66.7	93.3	133.3	180.0
Power Supply (V)	2.5	1.8	1.5	1.2	0.9
Target Impedance (mΩ)	3.1	1.3	0.8	0.45	0.25

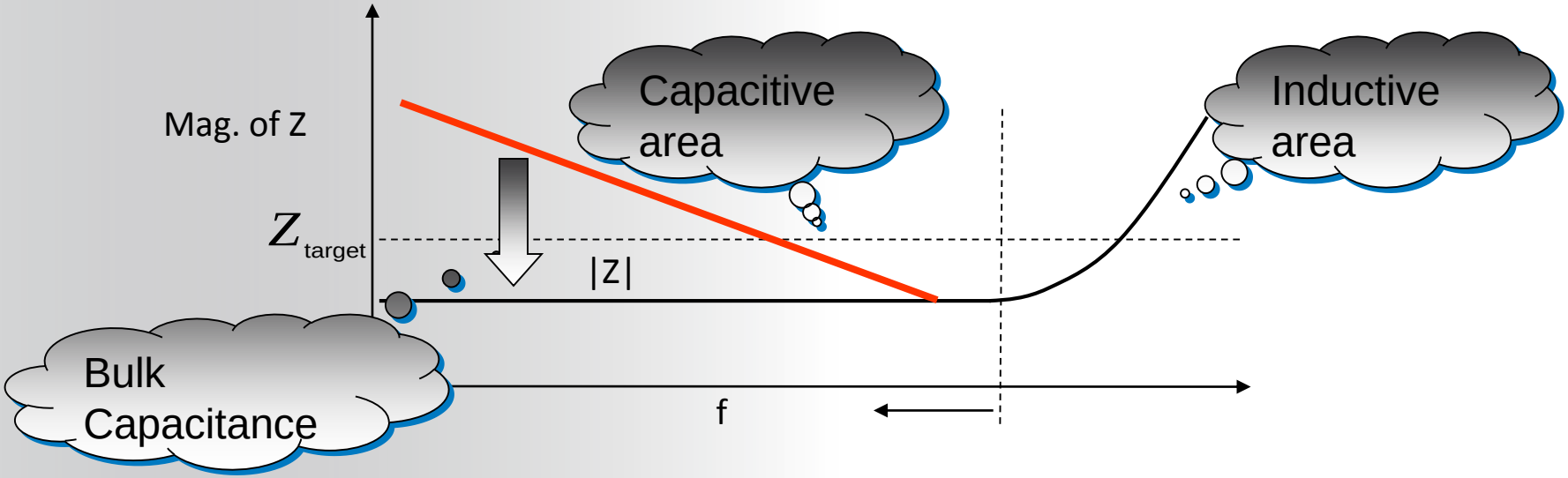
*Source: International Technology Roadmap for Semiconductors

*Target Impedance is falling ~ 1.6x, every 3 years

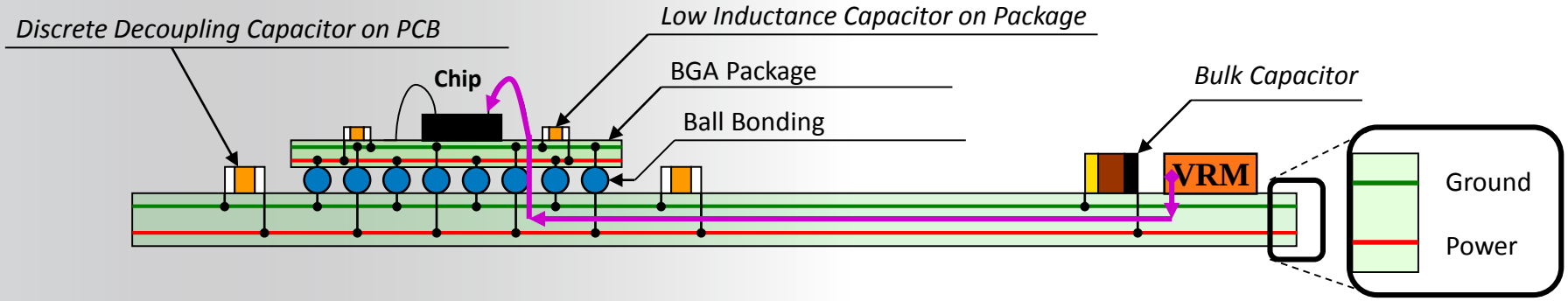
Components of Z

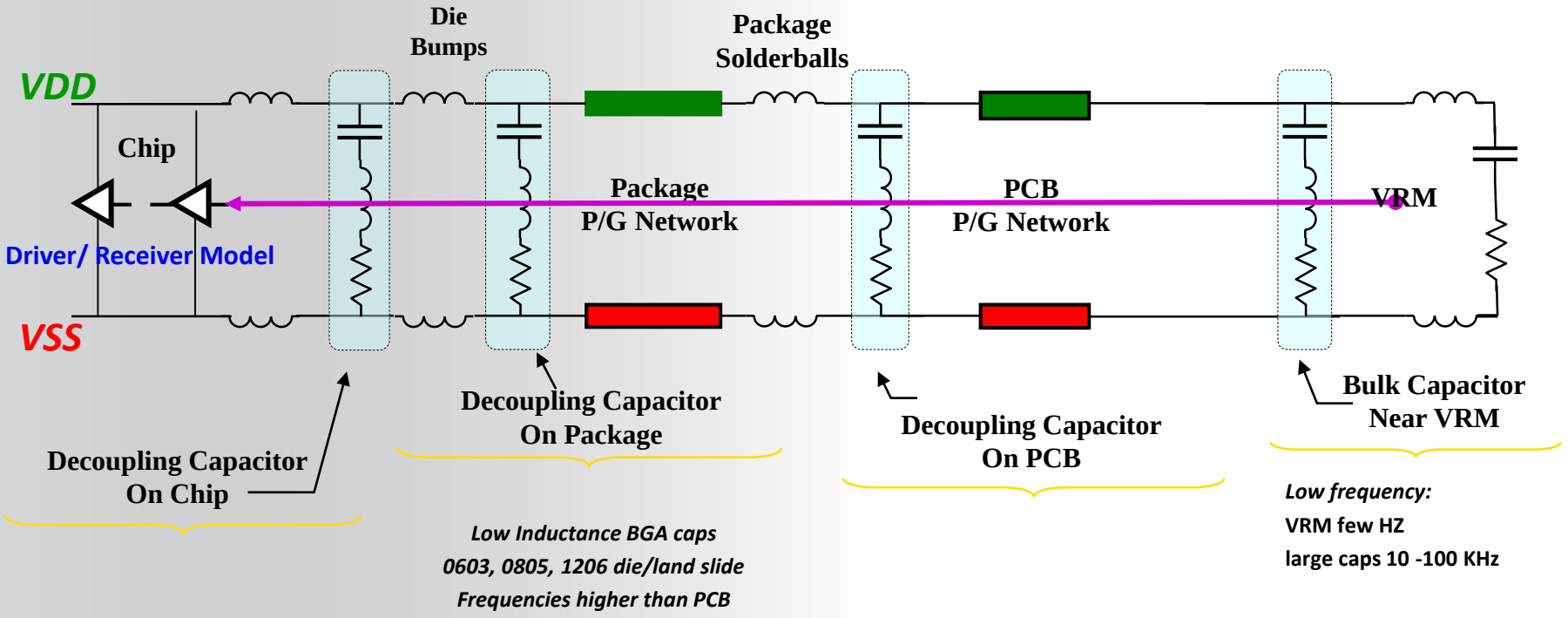
Impedance consists of

- **Capacitive factor, decreases with frequency** $\frac{1}{2\pi f\ C}$
- **Inductive factor, increases with frequency**
- **Inductance includes plane inductance, ESL of decoupling capacitors, traces and vias which connect planes to capacitors** $2\pi f\ L$



Core Power Delivery Network





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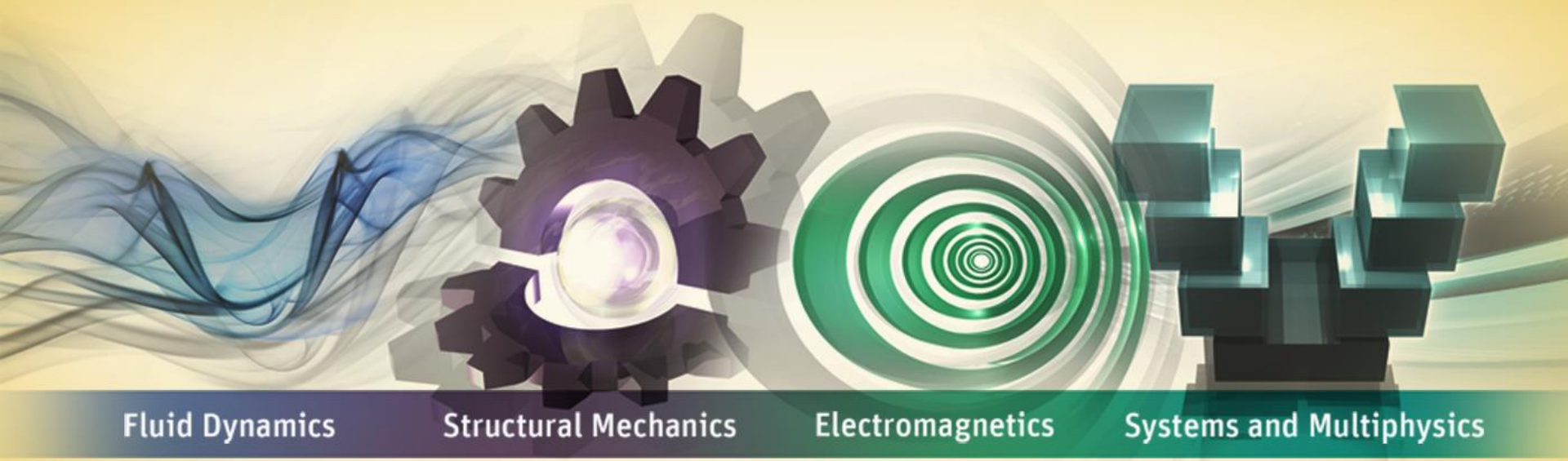
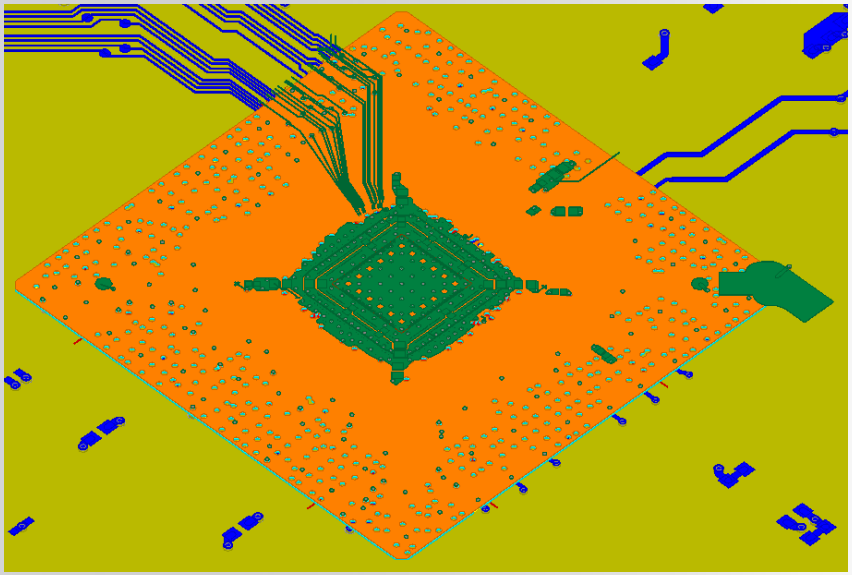
Merging Package on Board



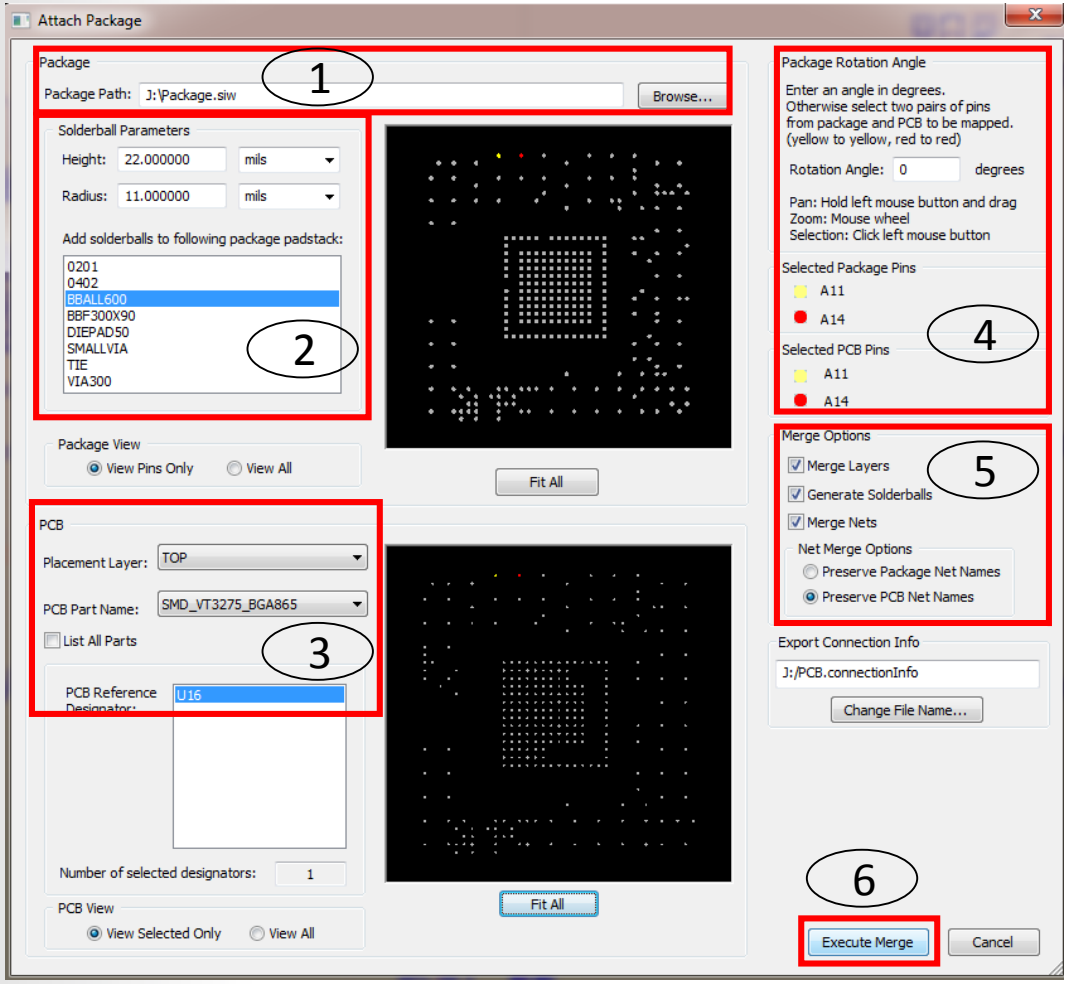
Connect a package onto a PCB

- **Tools > Attach Package Design…**
- **Some recommendations :**
  - **The project of the board must be opened**
  - **Identify the package location.**
  - **Identify the Part Name, Designator Name of the Package.**
  - **Identify a specific net in the board and package side to know if a rotation is needed.**
  - **Package Padstack**



Connect a package onto a PCB

- Enter the Package Path
- Select the solderballs model and parameters
- Select the PCB Part Name and PCB Reference Designator
- Align pins using pins selection
  - Automatic
- Select Merging options
  - Merge Layers
  - Merge nets
  - Generate solderballs
- Execute Merge



Workshops

WS06_0_siwave_pkg_pcb_merge.pdf

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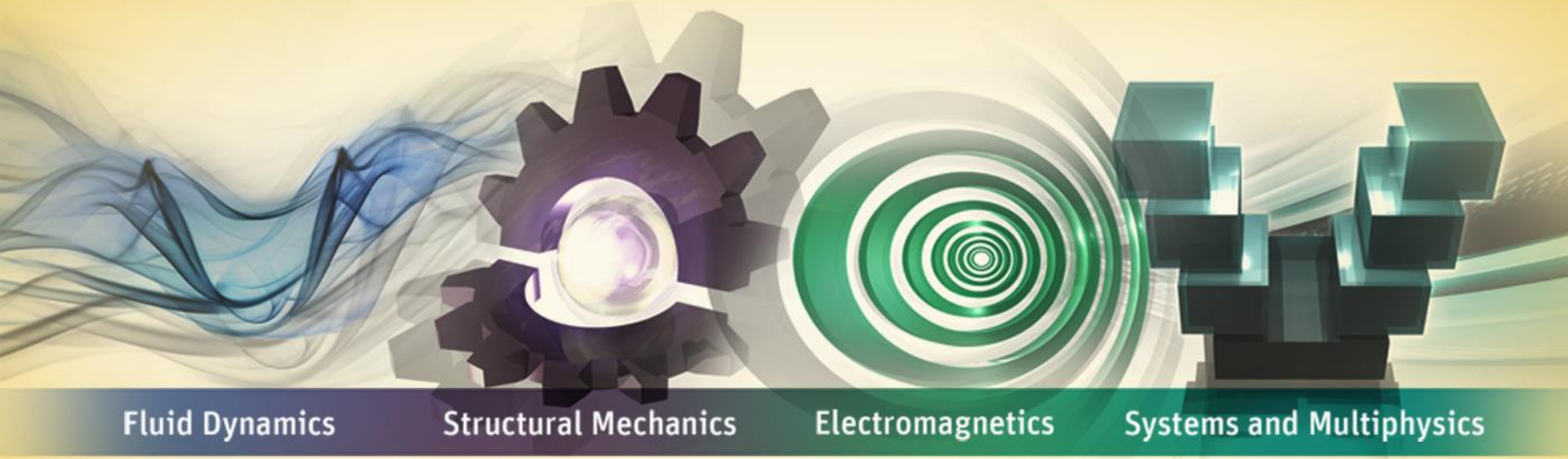
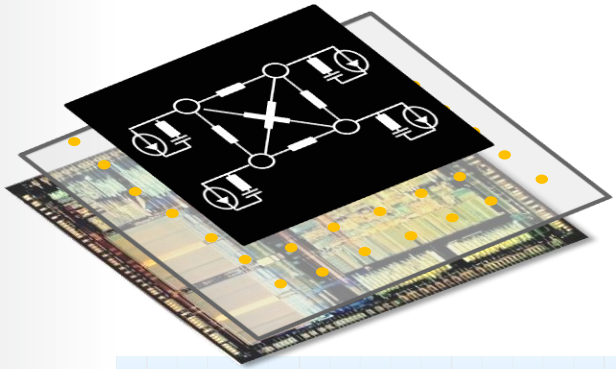
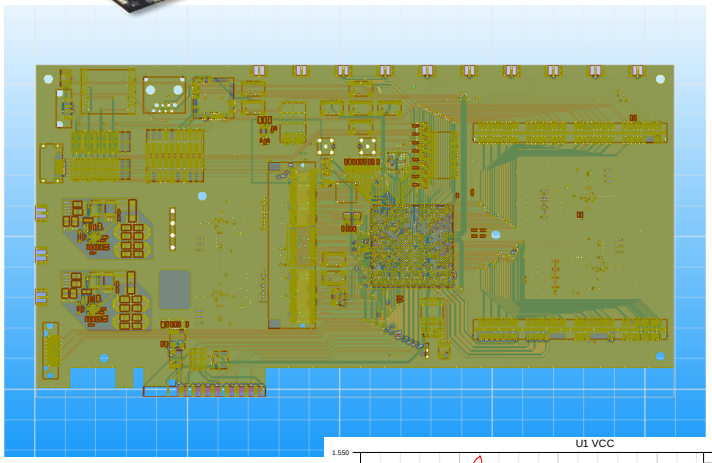
Chip-Package-PCB Co-Design using S-Parameters

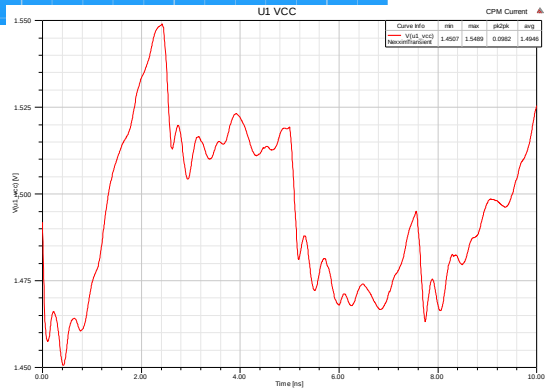


ANSYS Chip-Aware PDN Solution

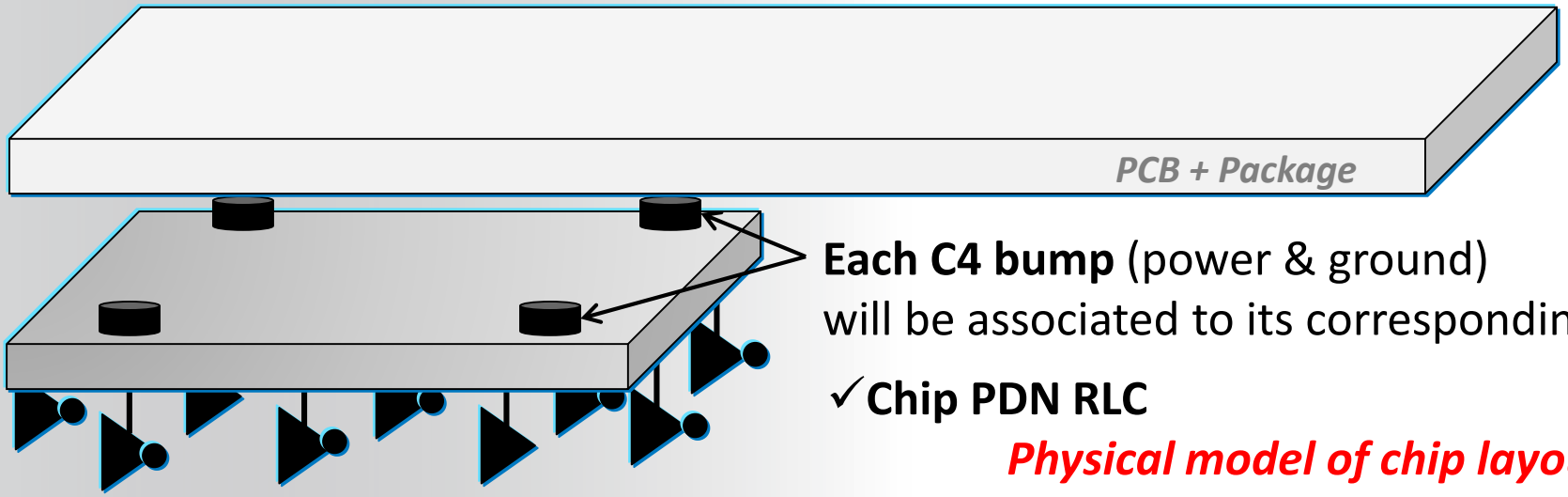
- Redhawk generates a chip power model (CPM) including chip PDN parasitics and switching currents.
- SIwave provide robust extraction of IC packages and boards with broadband S-parameter models.
- PI Advisor optimizes decoupling capacitor selection to meet a target impedance.
- AEDT simulates power noise in the time domain.







What's in a CPM?



Each C4 bump (power & ground) will be associated to its corresponding:

✓**Chip PDN RLC**

Physical model of chip layout

✓**Transistor/cell current /cap/ESR**

Electrical model of chip layout

```
.SUBCKT PowerModel p1 p2
************************************************************
* Apache RedHawk Chip Power Model [Accurate RC reduction]
**********
* Pad name
* DPOWER21
* DGROUND20

* No connec
C0_1 p1 p2
R_1_1 p1 n3
C_1_1 n3 p2
R_2_1 p1 n4
C_2_1 n4 p2
R_3_1 p1 n5
C_3_1 n5 p2
R_4_1 p1 n6
C_4_1 n6 p2
.ENDS
```

```
*****************************************
* Apache RedHawk Chip Power Model [ Ver 1.00 ]
* Version: 10.2     Linux32e3 (Jan 20 00:31:13 2011)
*****************************************
.INCLUDE "PowerModel.sp.inc"

* Begin Chip Package Protocol --->
* die_area 0 0 4920.62 5000.36
* Start Units
*   Length um
* End Units
* DPOWER21      :    (4905.000000 3279.000000)   :    p1    = PAR_0_0_VDD
* DGROUND20     :    (4880.000000 3219.000000)   :    p2    = PAR_0_0_VSS
* End Chip Package Protocol <---

.subckt adsPowerModel p1 p2

Xpdn   p1 p2 PowerModel

Icursig1 p1 p2 pwl(
+ 0.000000ps 0.589435
+ 150.000000ps 0.854897
+ 240.000000ps 0.867186
+ 330.000000ps 0.827372
```

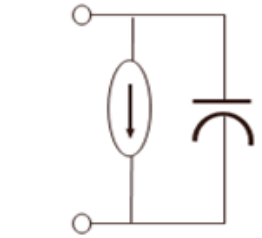
CPM is topological, physical and activity based

Benefits of CPM

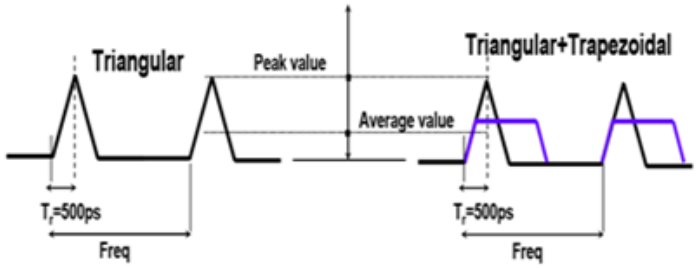
Chip Current

Chip Parasitics

Traditional die model



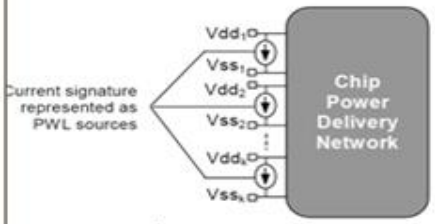
Simplifying assumption of all gates switching at same time



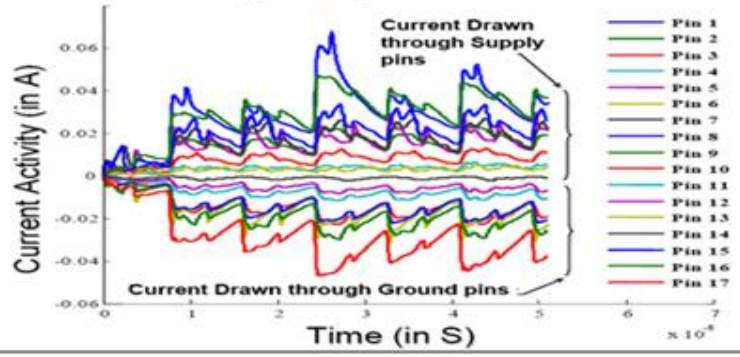
Estimated Cdie
Missing Rdie, Ldie

Single Lumped Model

Apache CPM



Apache CPM: supports both static and dynamic models

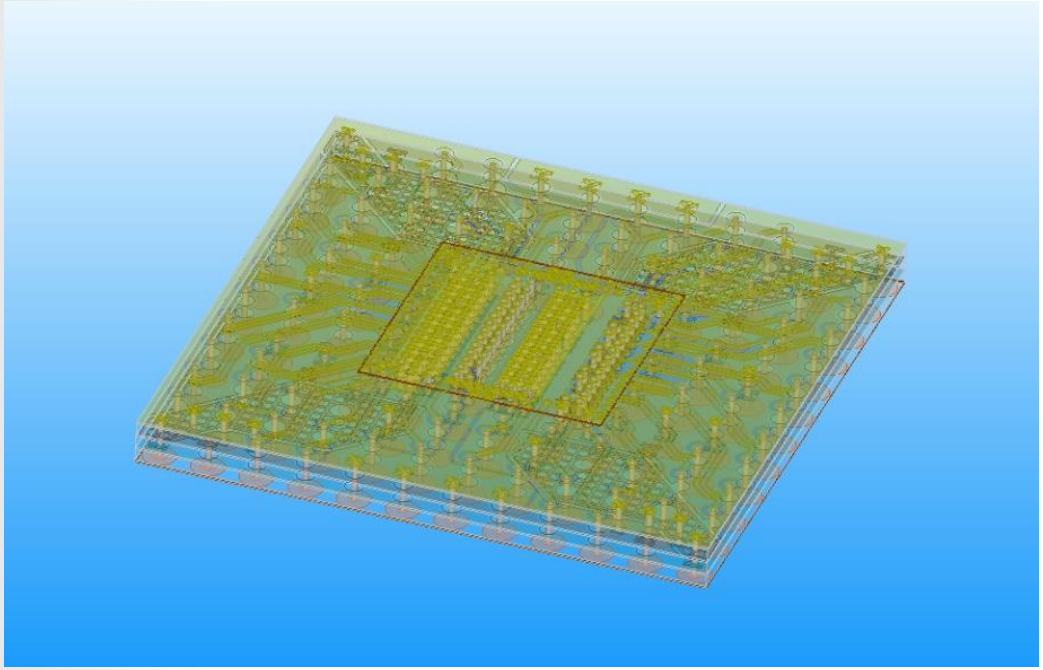


CPM includes all die parasitics

Power-grid RLC
Intrinsic De-cap
Intentional De-cap
Instance Load Capacitance
Well Capacitance

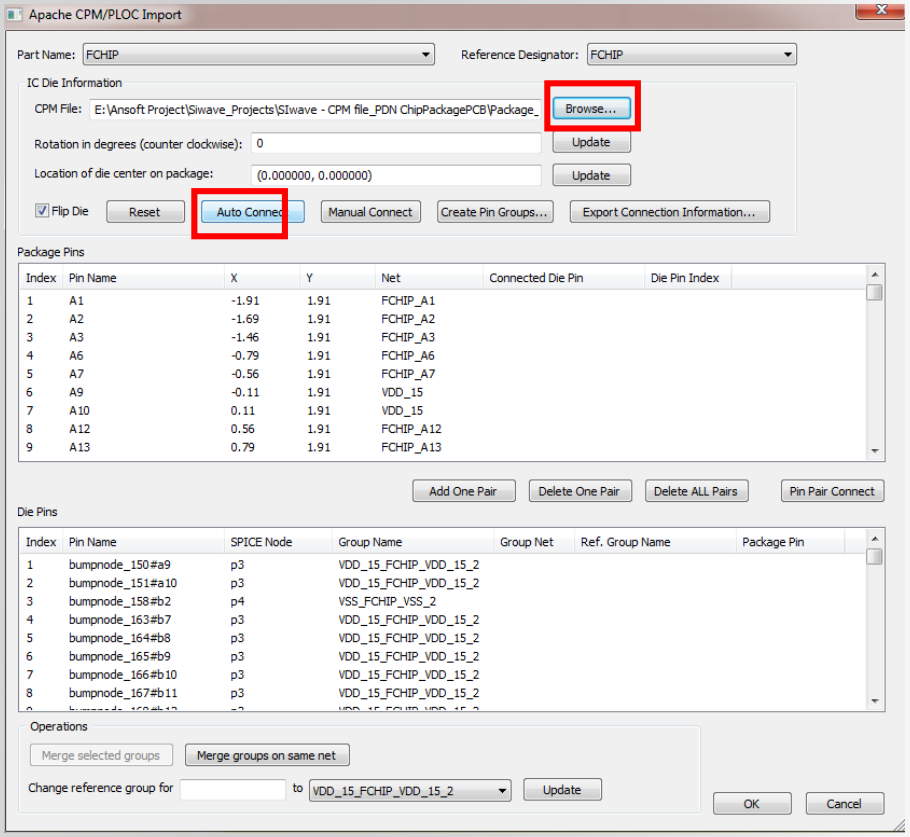
SIwave CPM Integration

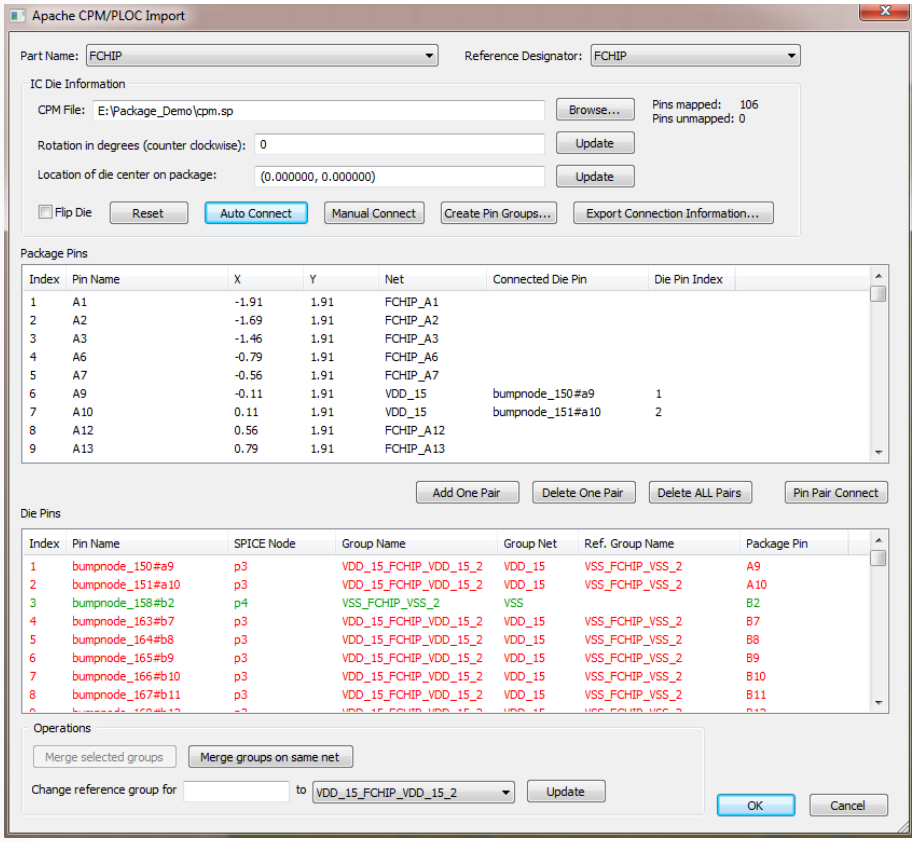
- **SIwave CPM integration includes the following:**
  - **Import of die PDN for inclusion in frequency-domain extractions**
  - **Automatic matching of die pin to CPM pin locations**



SIwave CPM Setup

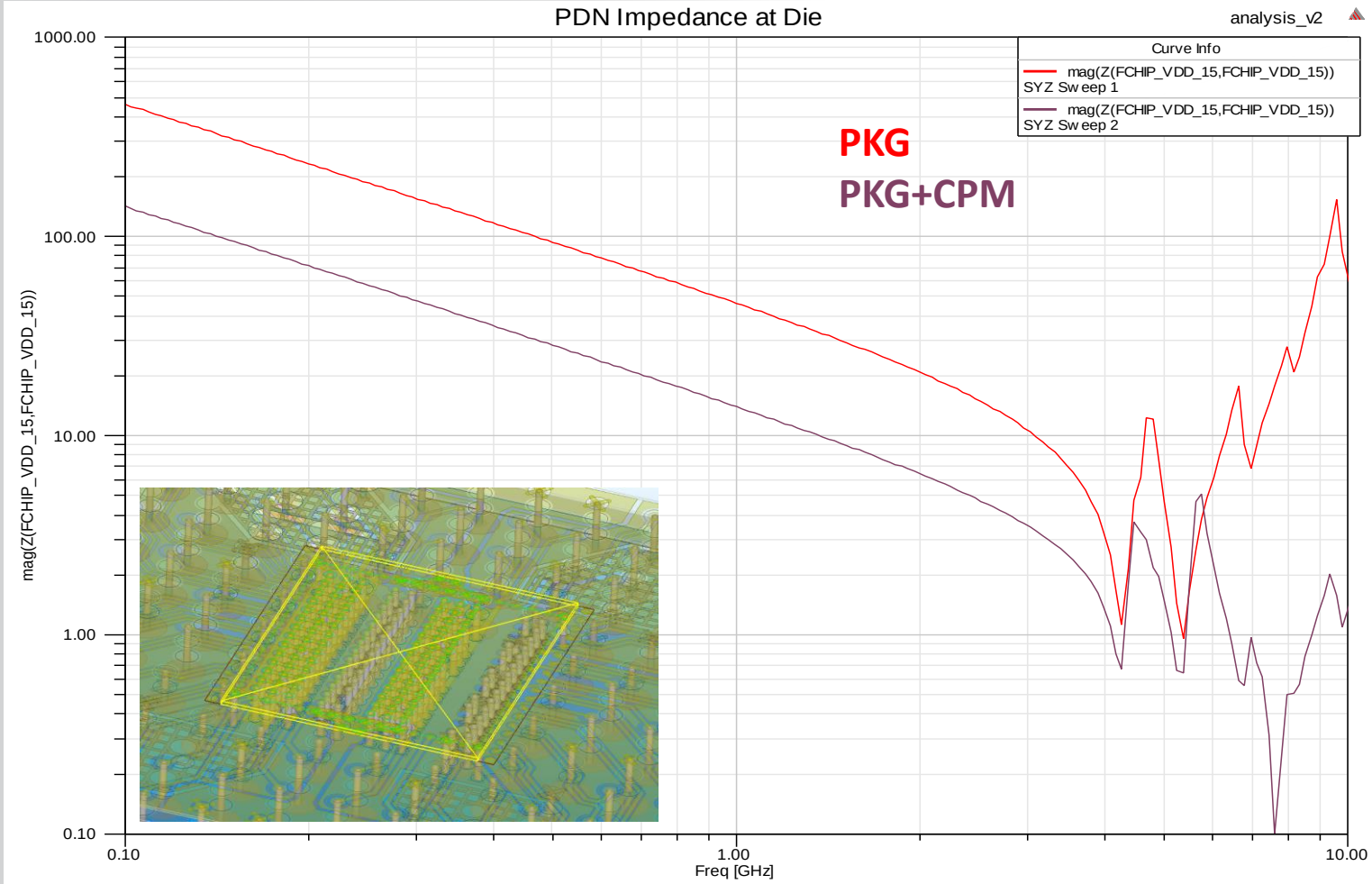
- Select the device footprint in the SIwave layout
- **File > Import > Apache CPM/PLOC file…**
  - Browse to the CPM file
- Click the **Auto Connect** button to attach SIwave footprint pins to the CPM pins.



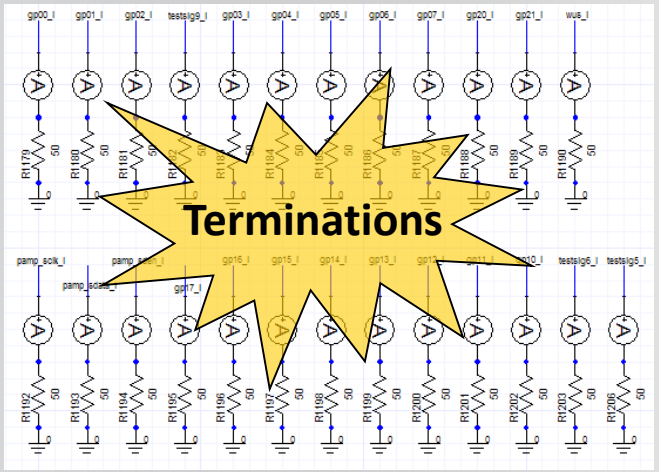


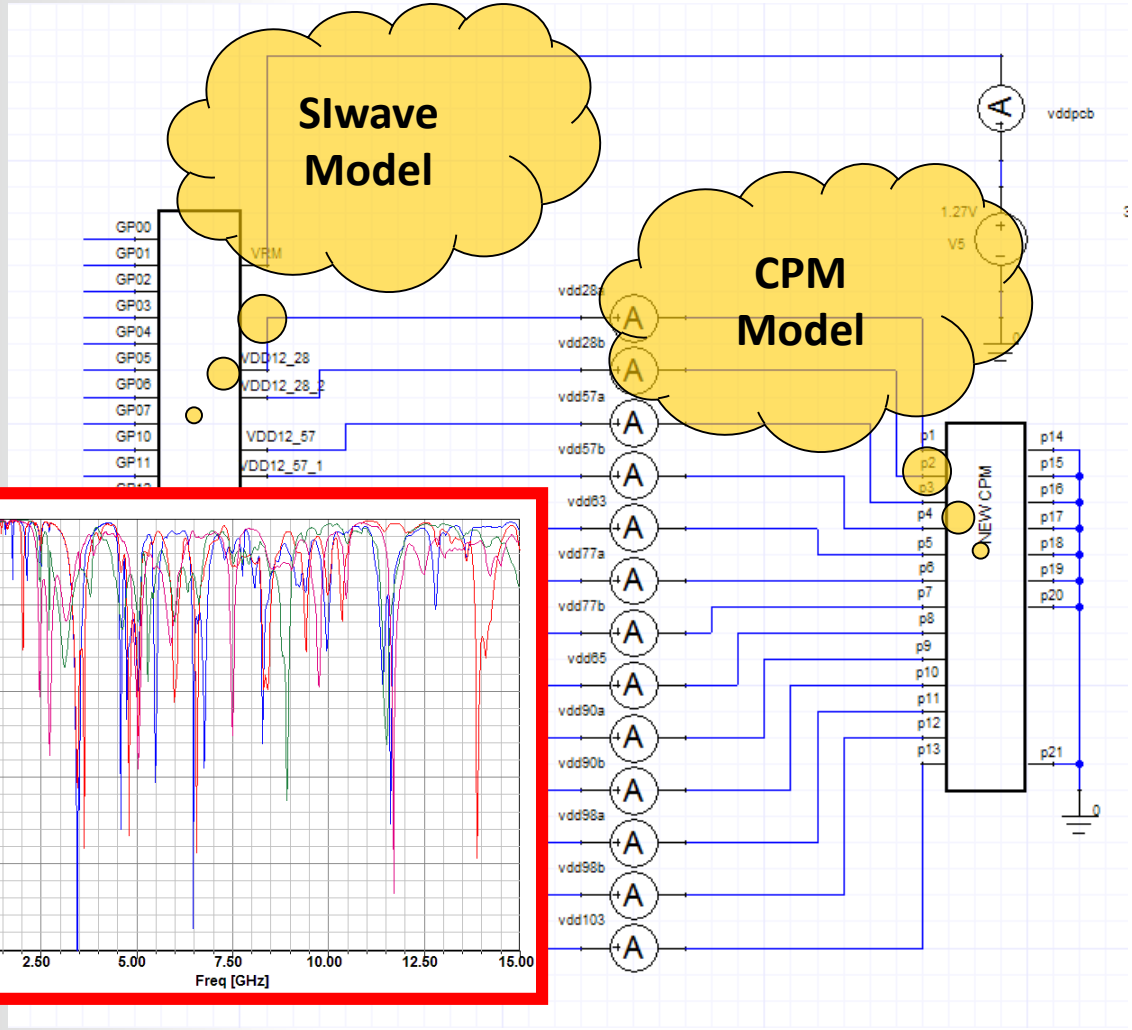
SIwave CPM Setup

- **CPM Impedance Effect**
- There is a significant effect at a broad frequency range due to the high total capacitance present on this chip.



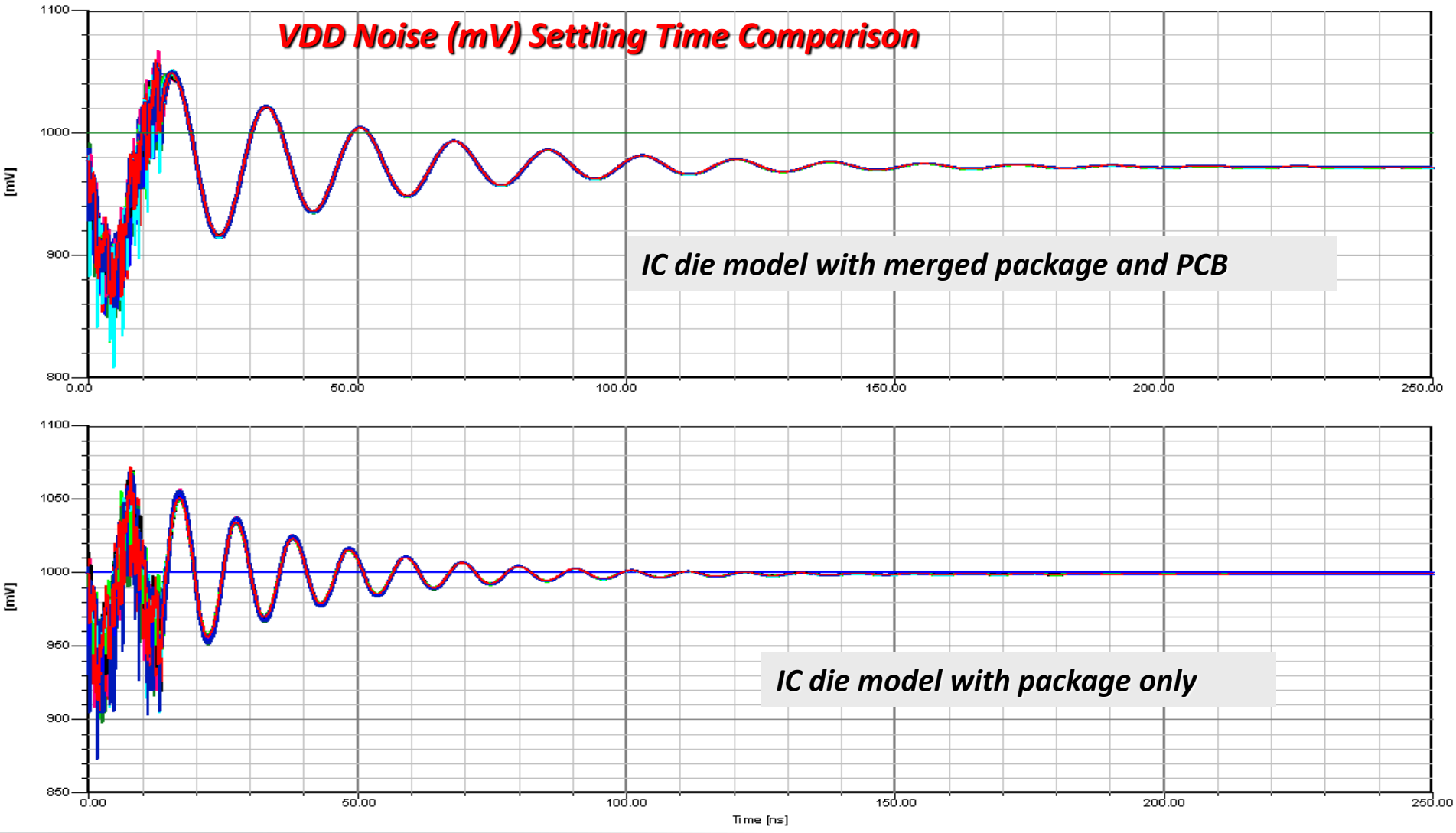
AEDT , SIwave, and CPM





- Drive VDDs with CPM
- Capture coupled high-frequency noise
- Run Near/Far-Field Simulations using tran results

AEDT Transient Results



Simulation approaches

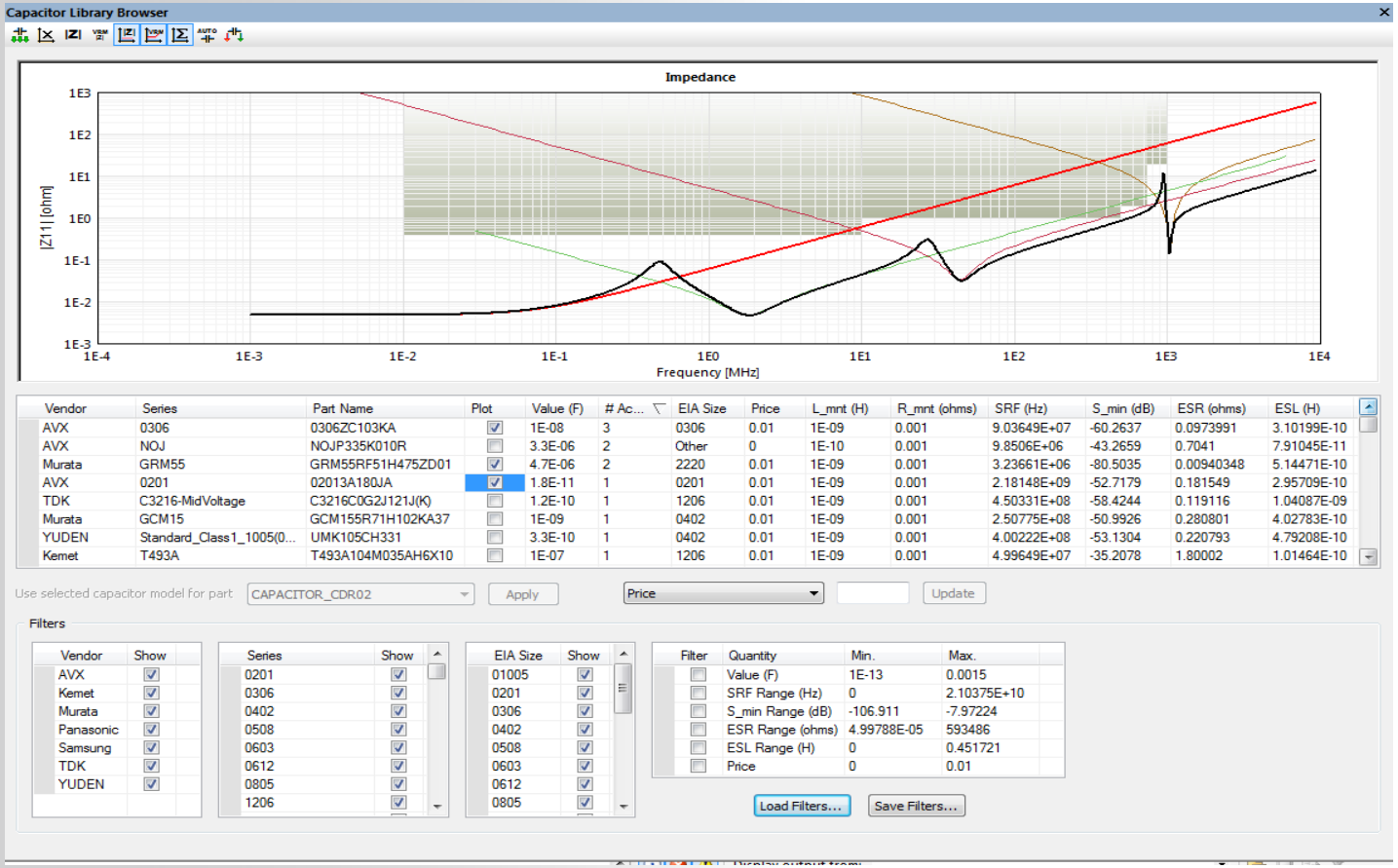
- **The PI methodology is different depending on the needs. We can considered two simulation approaches.**
  - « Free optimization » of a design (The location, mounting style, value, number and type of capacitors are not predefined).
  - « Fixed » optimization of an existing design. The location of capacitors are already fixed (footprint defined as discrete device during database import). The max number of capacitor is also predefined.
    - PI Optimization using SIwave and ANSYS AEDT (Iterative Approach)
    - PI Optimization using PIadvisor (An Automated Approach)

Free optimization of a design

- **Place Probe on different power nets to scan all the frequency range. EM extraction of impedance for critical devices :**
  - SYZ analysis
  - Compare to the defined target
- **Resonances analysis is performed to evaluate problems on power planes and helping the placement of decoupling capacitors :**
  - Resonance and frequency sweep analysis
  - Choose some decoupling capacitors to move the resonances in terms of Impedance magnitude and Resonance frequency
  - Capacitor Library Browser
  - Place them close to the resonance peaks
- **The final step is to simulate in time domain to check for compliance. Look at the Switching Power Noise**
  - Transient simulation in AEDT

The Capacitor Library Browser

- **Explore and plot the impedance of various vendor or imported capacitor components versus frequency and quickly determine the lumped circuit equivalent (Included with SIwave)**
  - Tools > Capacitor Library Browser



PI Optimization using SIwave and ANSYS AEDT (Iterative Approach)

- **A very useful technique for evaluating the effectiveness of the capacitors and there locations is to extract the model into AEDT.**
  - In SIwave, place a port at the IC and replace the capacitors you are interested in optimizing with a port.
  - After, run a SYZ simulation and import the s-parameters into AEDT.
  - Place a port again at the IC terminal and connect the capacitors from the other terminals to ground.
  - Now, when you run a linear network analysis, you can see the same results as in SIwave but it will be much quicker.
  - This allows you to try many different combinations of capacitors and optimize them.

ANSYS

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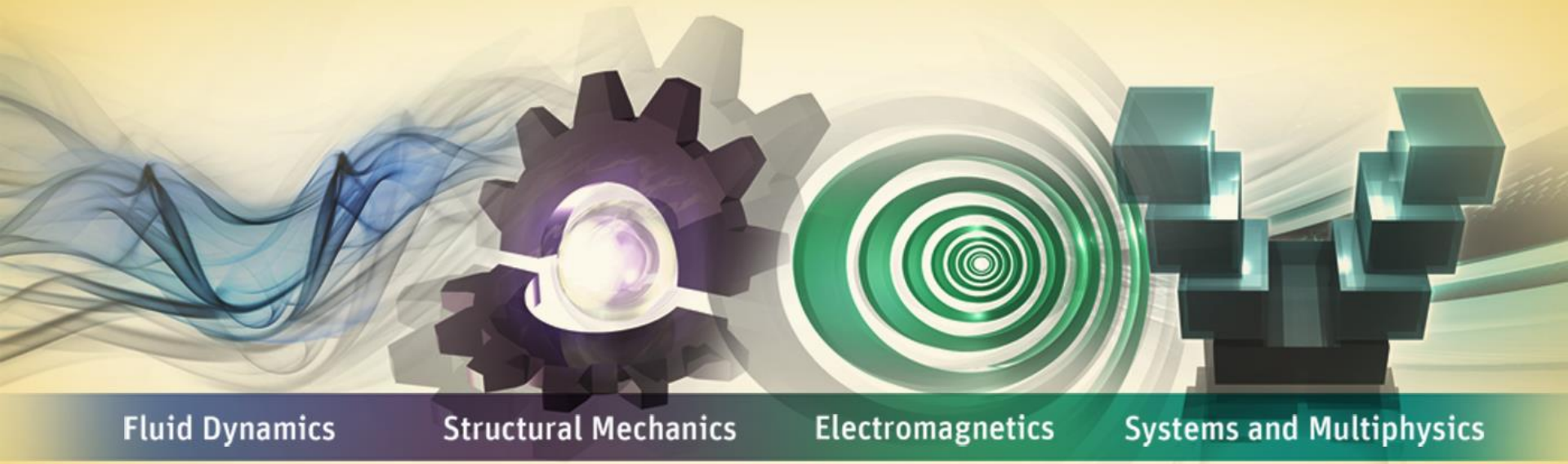
PIAdvisor



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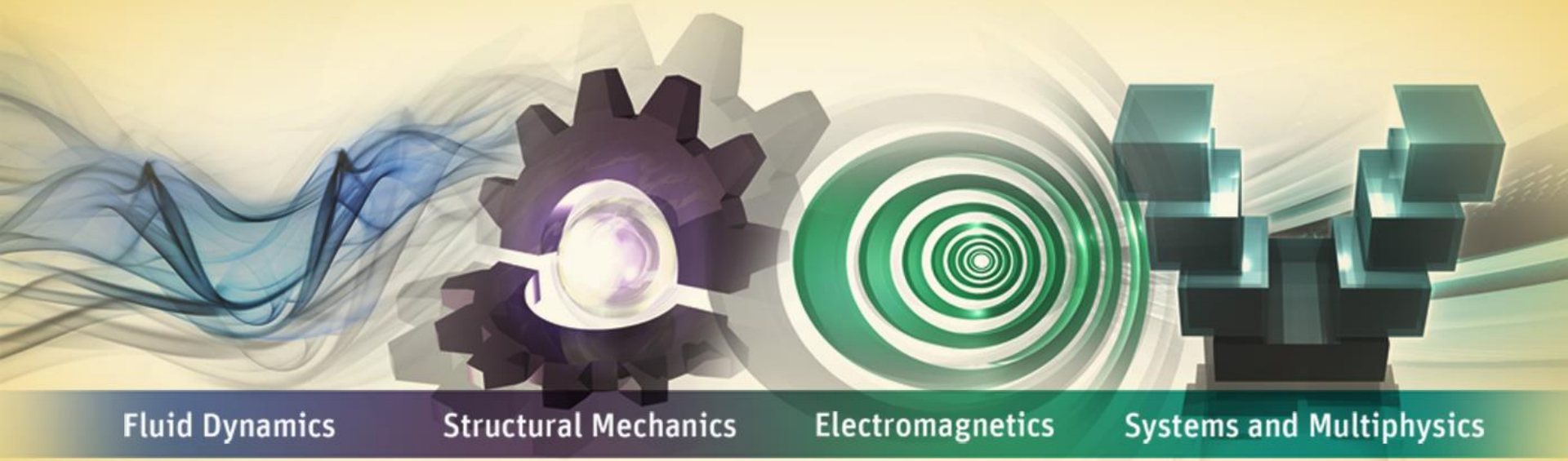
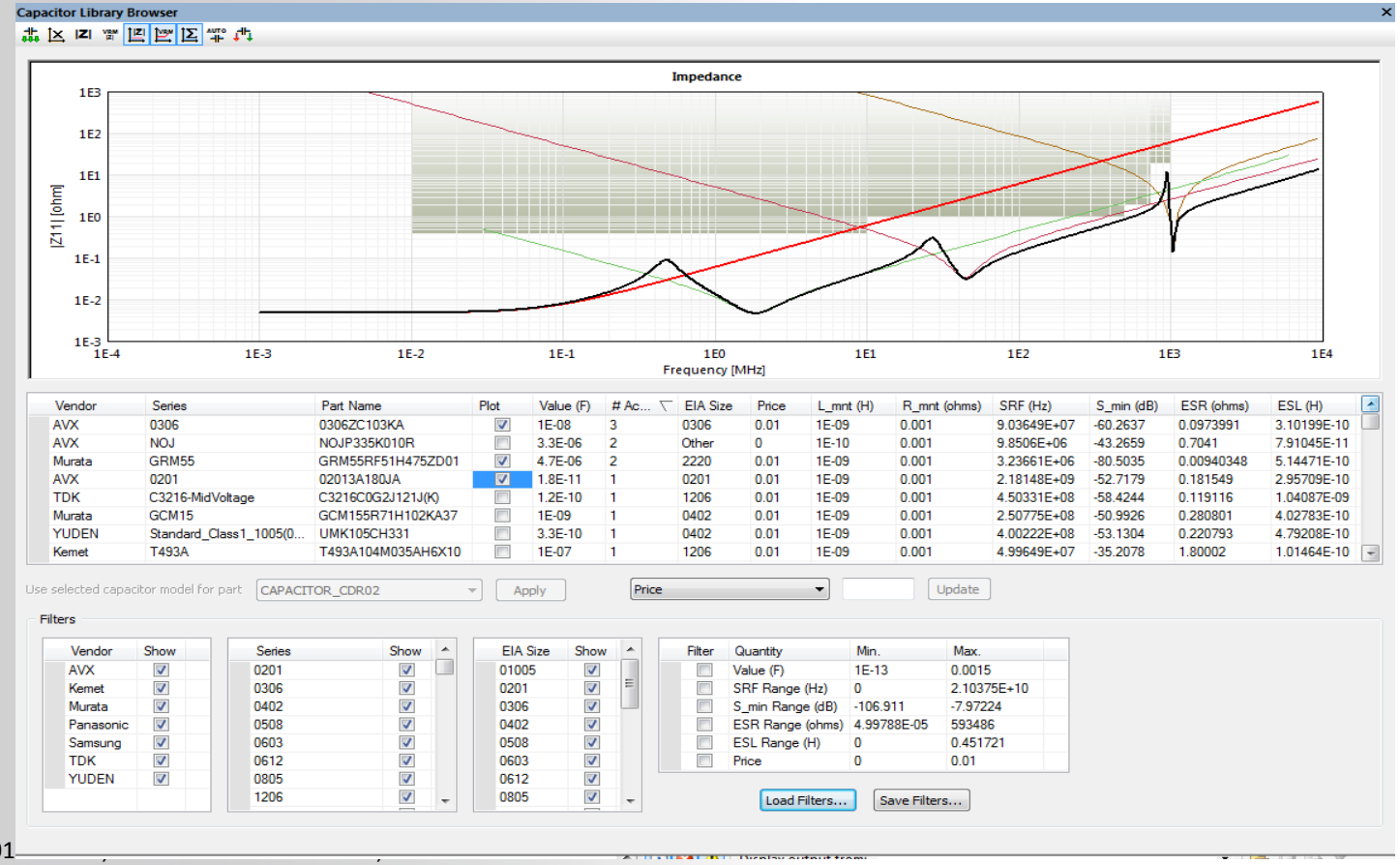
SimplePI using Capacitor Library Browser



The Capacitor Library Browser (1/2)

Explore and plot the impedance of various vendor or imported capacitor components versus frequency and quickly determine the lumped circuit equivalent (Included with SIwave)

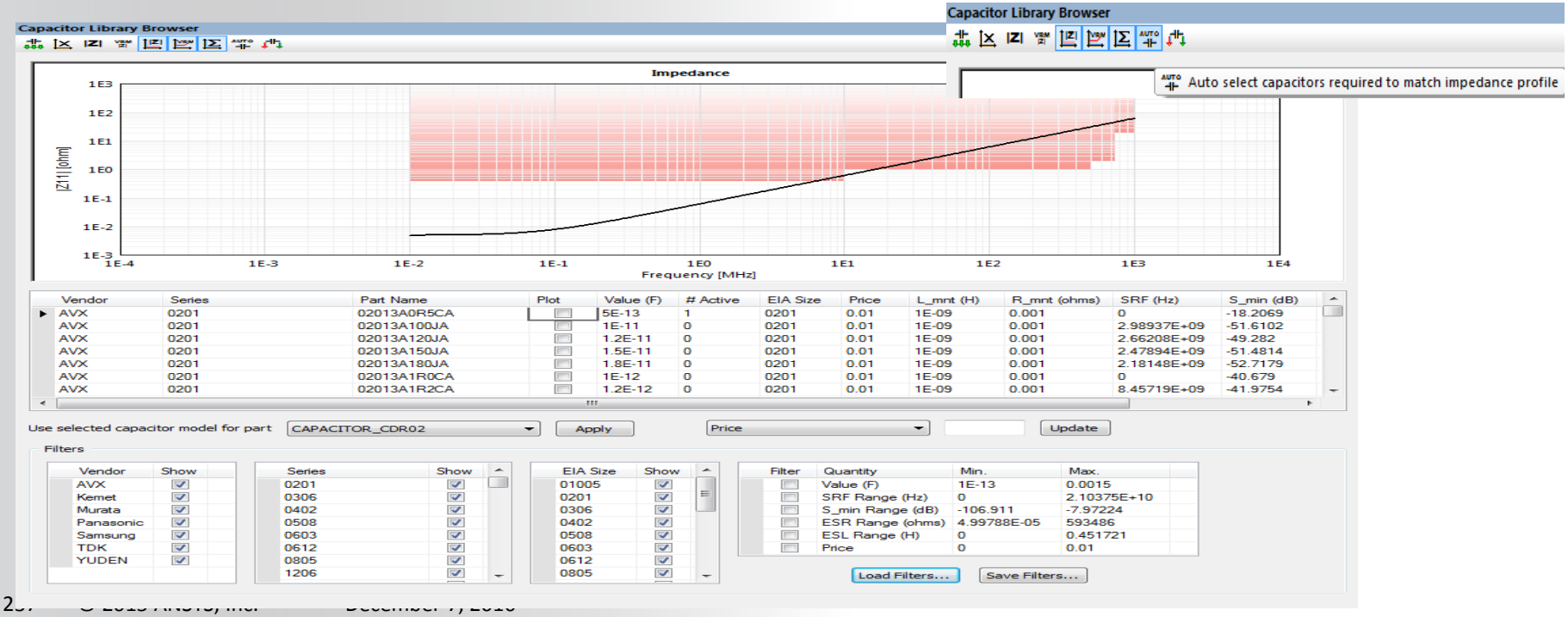
- **Tools > Capacitor Library Browser**



The Capacitor Library Browser (2/2)

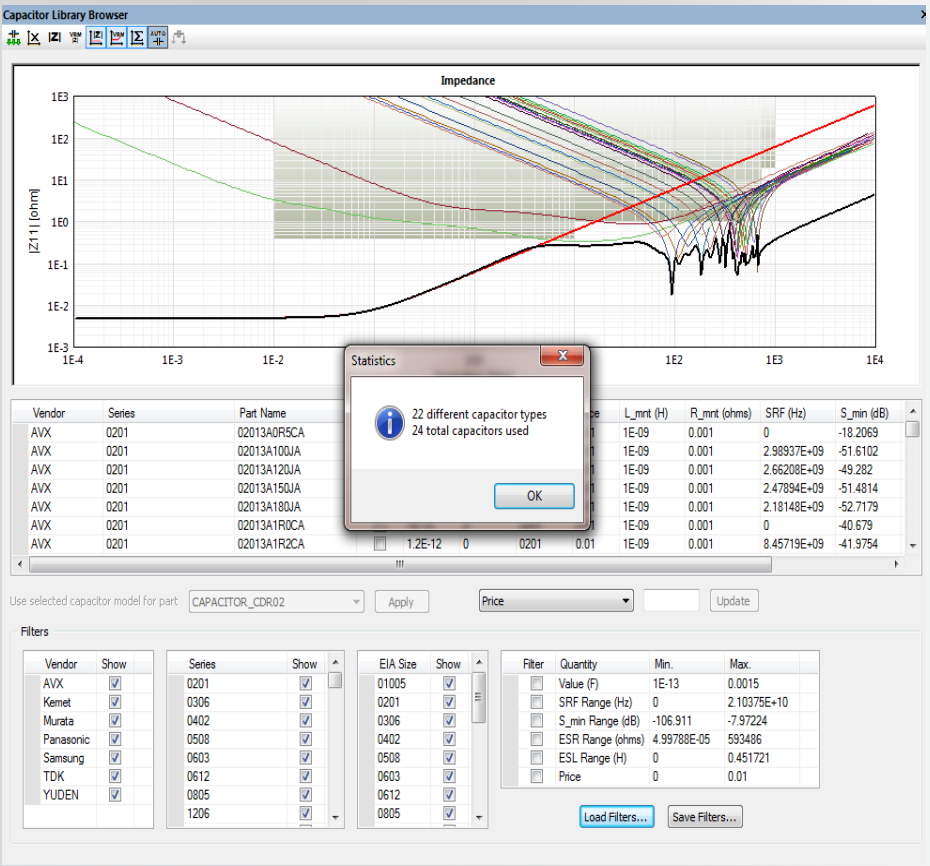
- **Automatically determine the best type and number of capacitors given a frequency dependent impedance mask and mount capacitors at certain user-defined capacitor regions.**
  - **(Pladvisor is mandatory)**

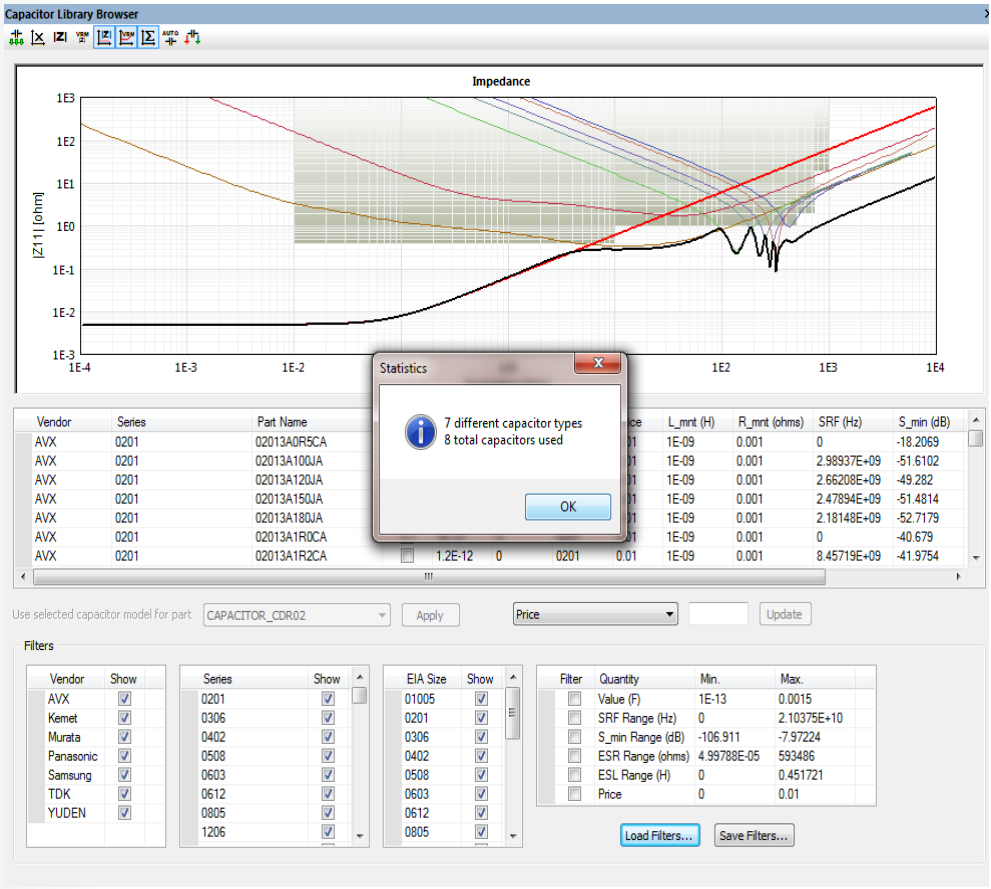
- **Define VRM parameters, Load an impedance Mask and then Run « Auto select capacitors required to match impedance profile »**



Matching process

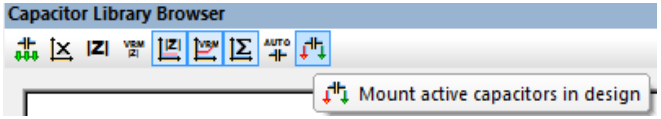
- **Two Statistics are provided, Siwave optimize the numbers of capacitors used and the types.**

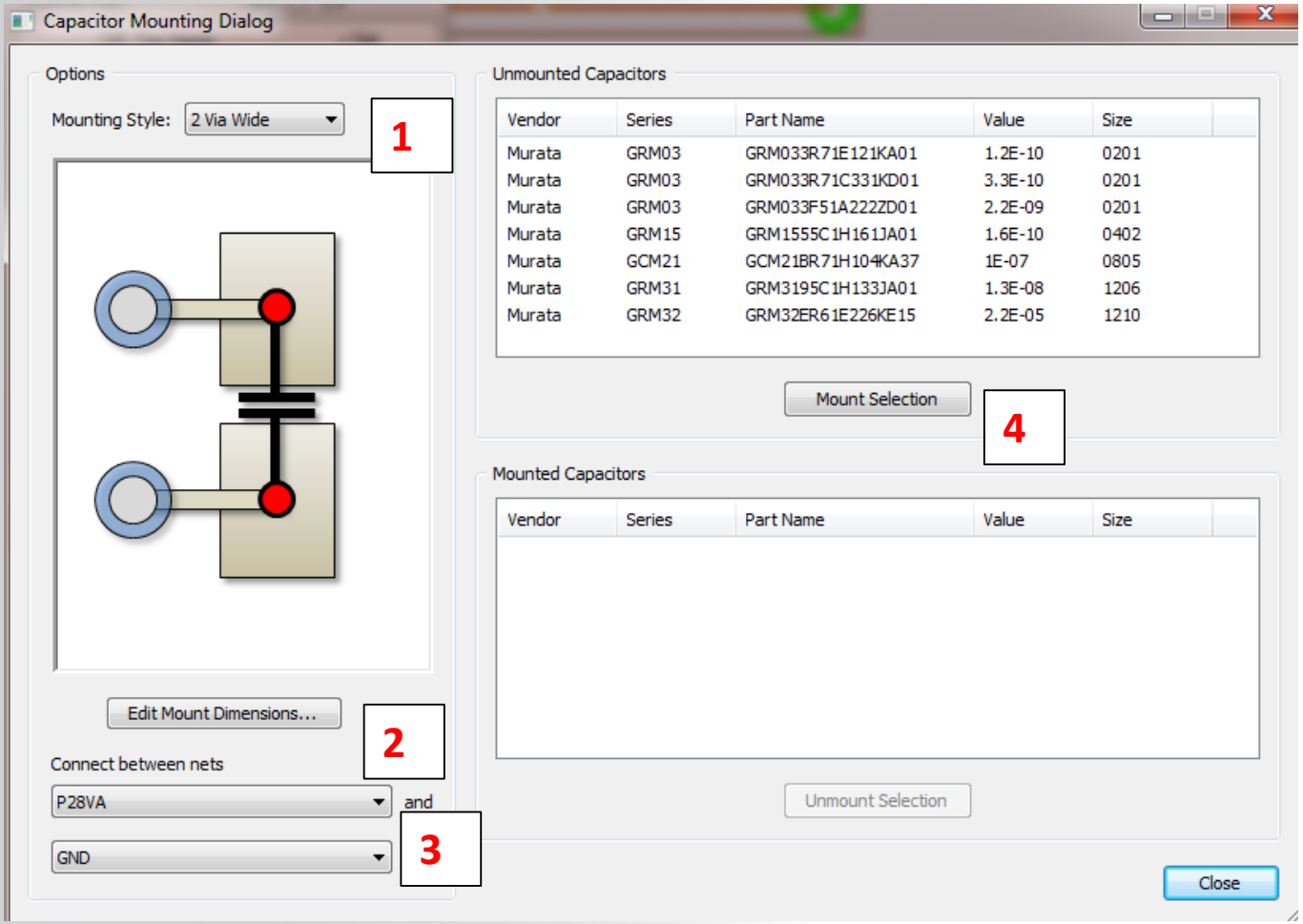




Mount the provided solution in the existing design

- Select « Mount active Capacitors in design »
- 4 steps are required to mount a capacitor.

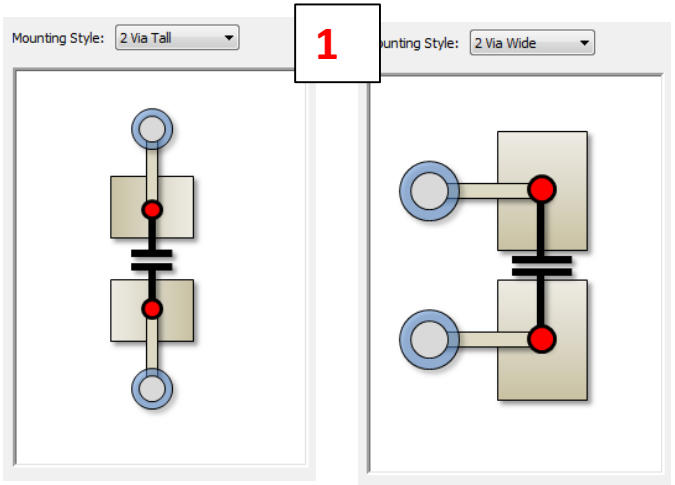


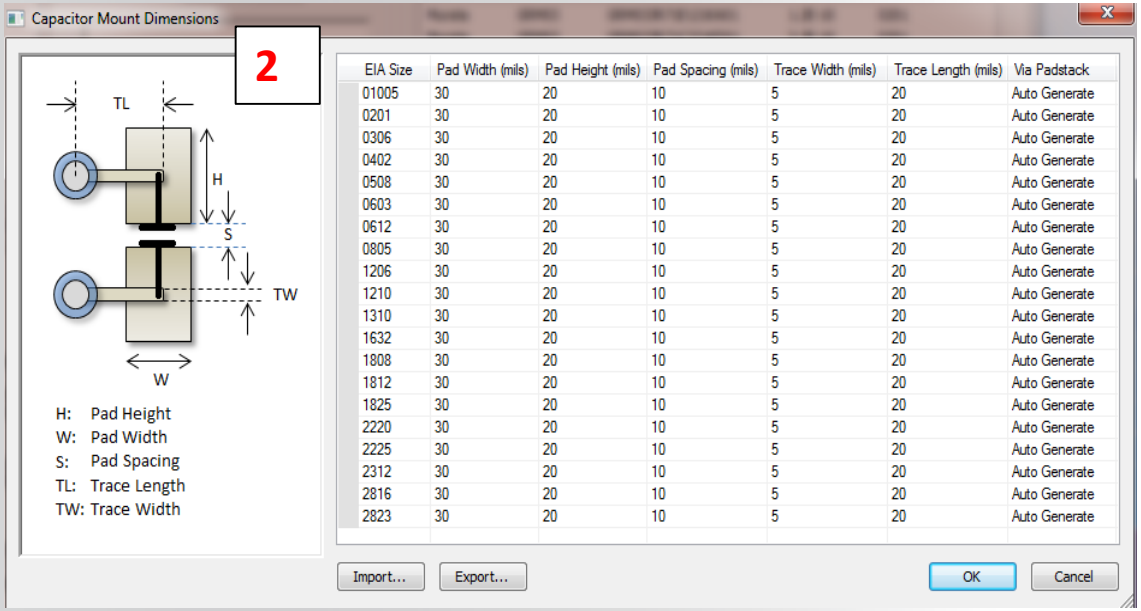


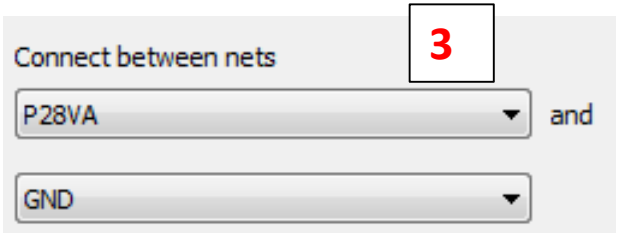
Mount the provided solution in the existing design (3/4 steps)

For each unmounted capacitors, SIwave allow you to choose :

- **The Mounting style (2 via Tall or 2 via Wide)**
- **Define the Capacitors Mount Dimensions**
- **Define the connected nets**



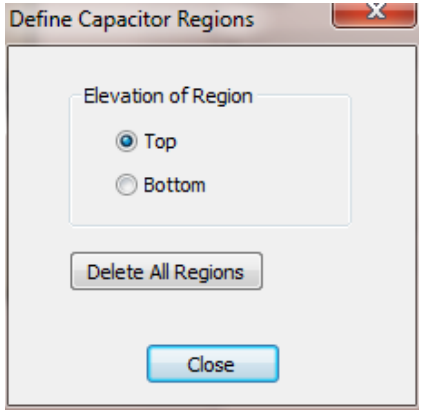




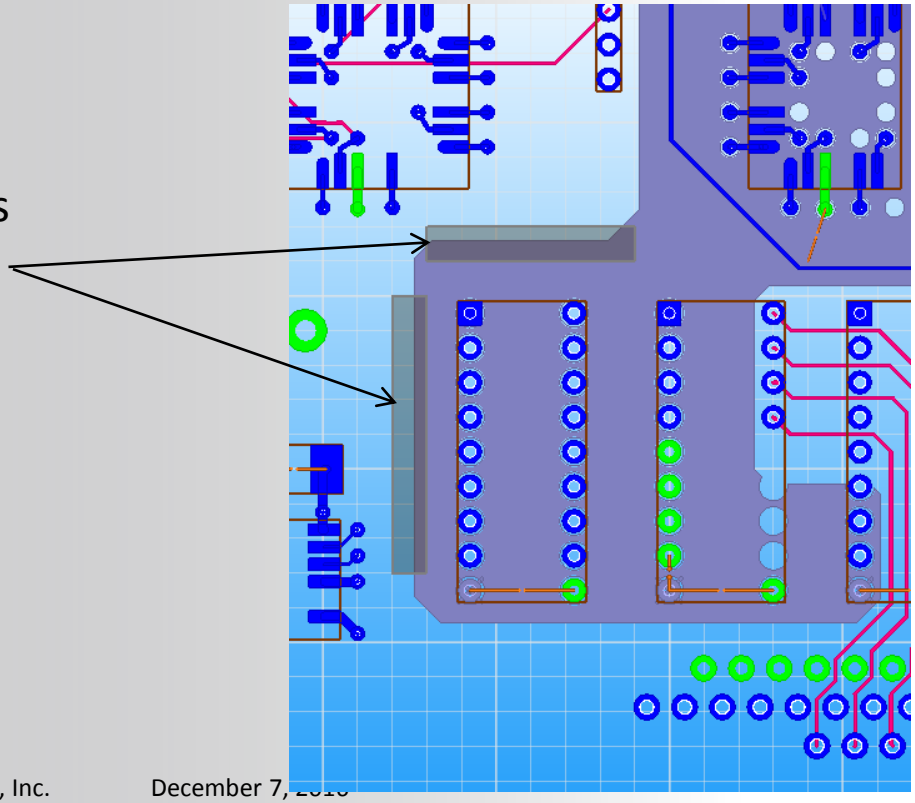
Mount the provided solution in the existing design (4/4 steps)

The last step to allow the mounting is to define a capacitor region on the layout :

- **Draw > Capacitor regions…**
  - **Select the top or bottom region**
- **Use the mouse to draw a rectangle**

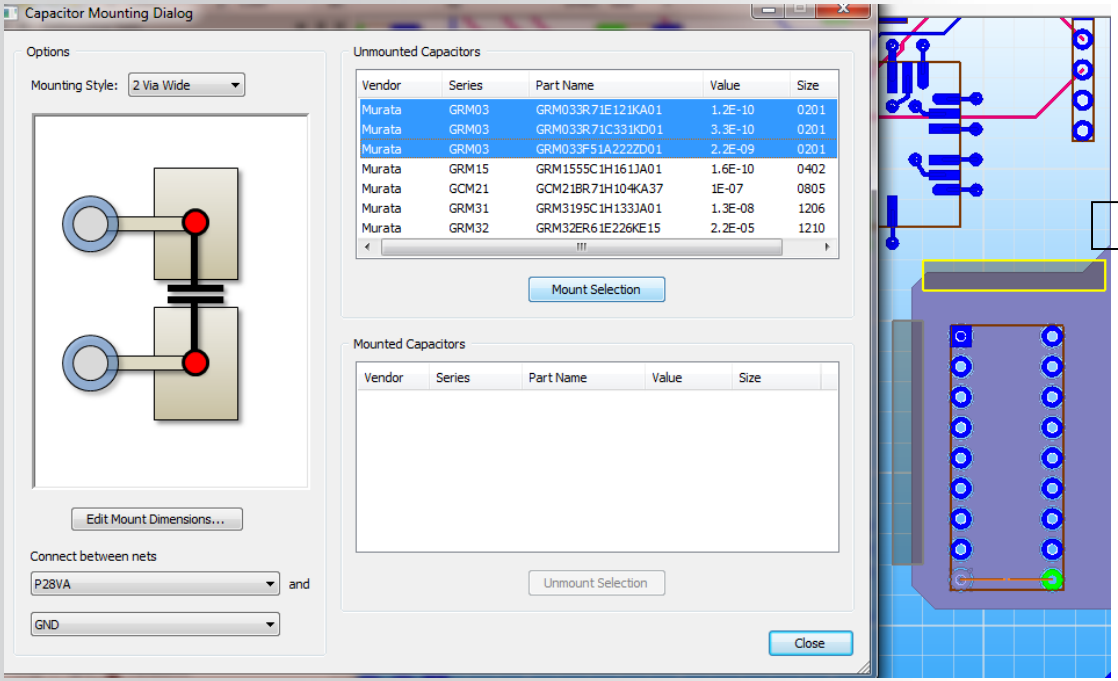


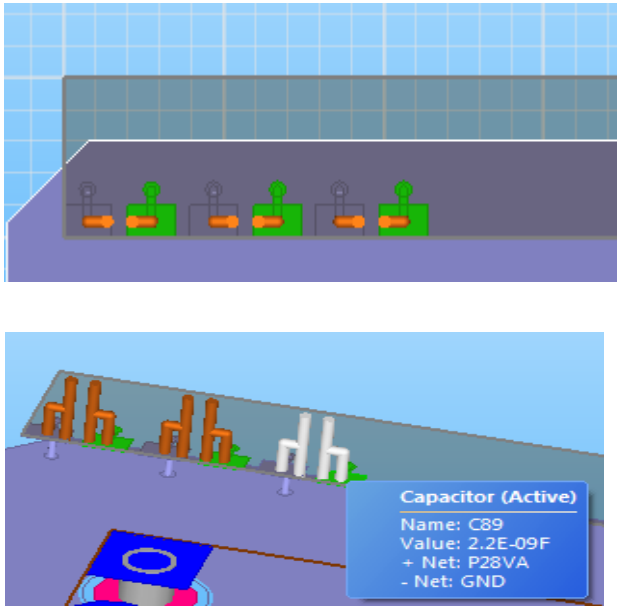
ie : 2 regions



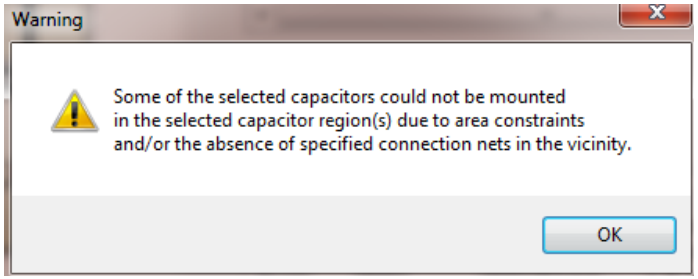
Mount the provided solution in the existing design (Final step)

Select the pre-defined regions and Unmounted Capacitors and click « Mount Selection »





- **Note : If some capacitors can not be mount due to their size / area constraints, the following message appears.**



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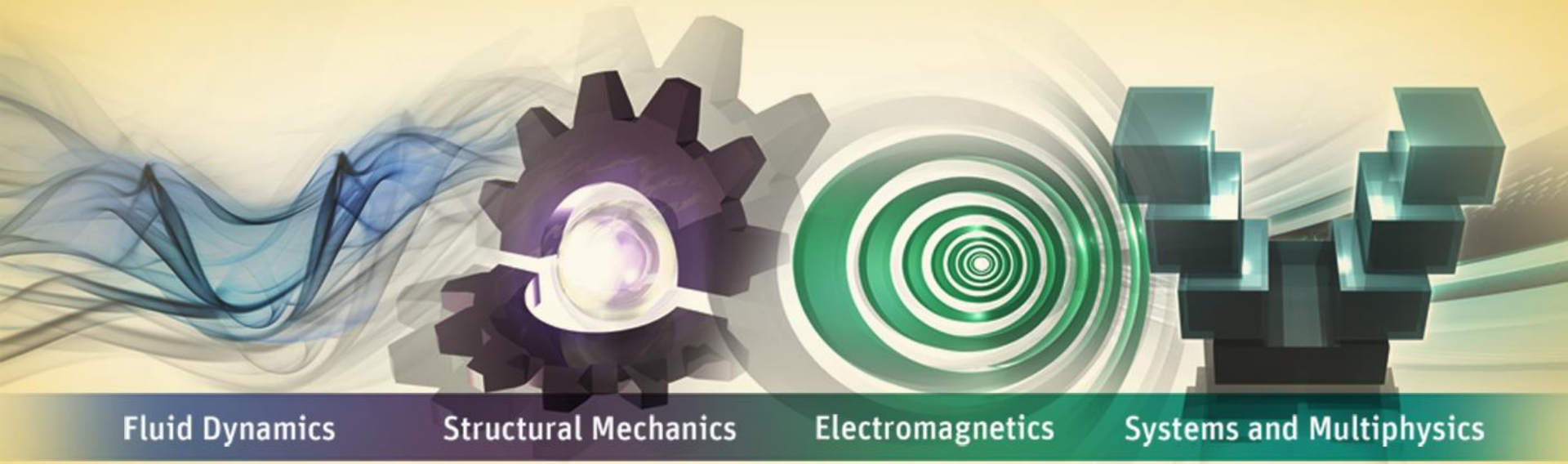
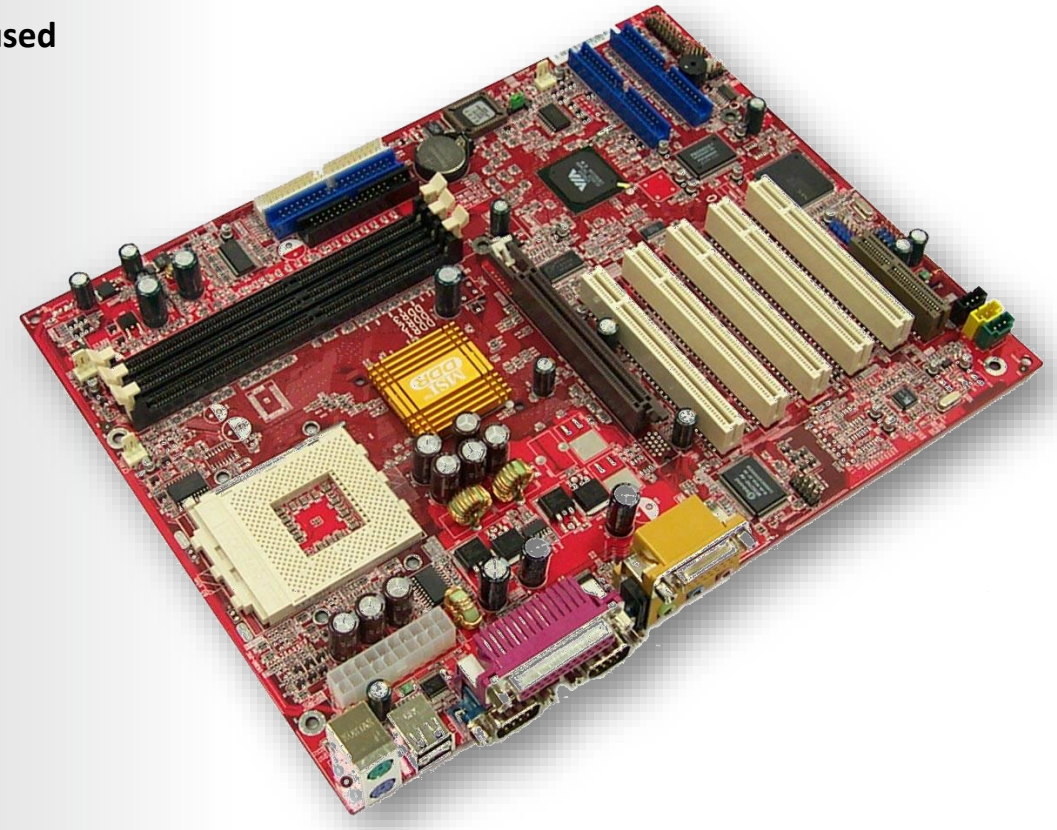
PIAdvisor – PI Optimization



Power Integrity Design

PCB Geometry present

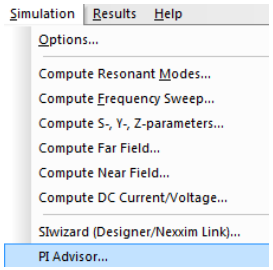
- A functional design, with all decoupling capacitors already placed on PCB
- PI Engineer may want to:
  - Increase capacitor count in order to make design more robust (i.e. overclocking, etc.)
  - Reduce the capacitor count
  - Reduce number of different capacitor types used
  - Redesign using lower cost capacitors
  - Chose appropriate capacitor location



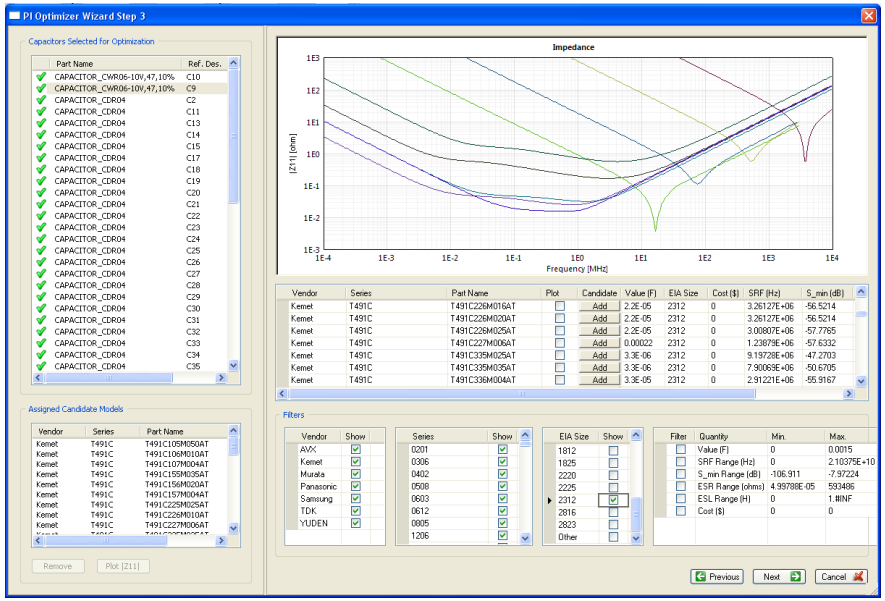
PI Advisor

Automated PI Optimization : An Automated Approach to investigate into Decoupling Analysis.

- Simulation > PIadvisor…



- A functional design, with all decoupling capacitors already placed on PCB



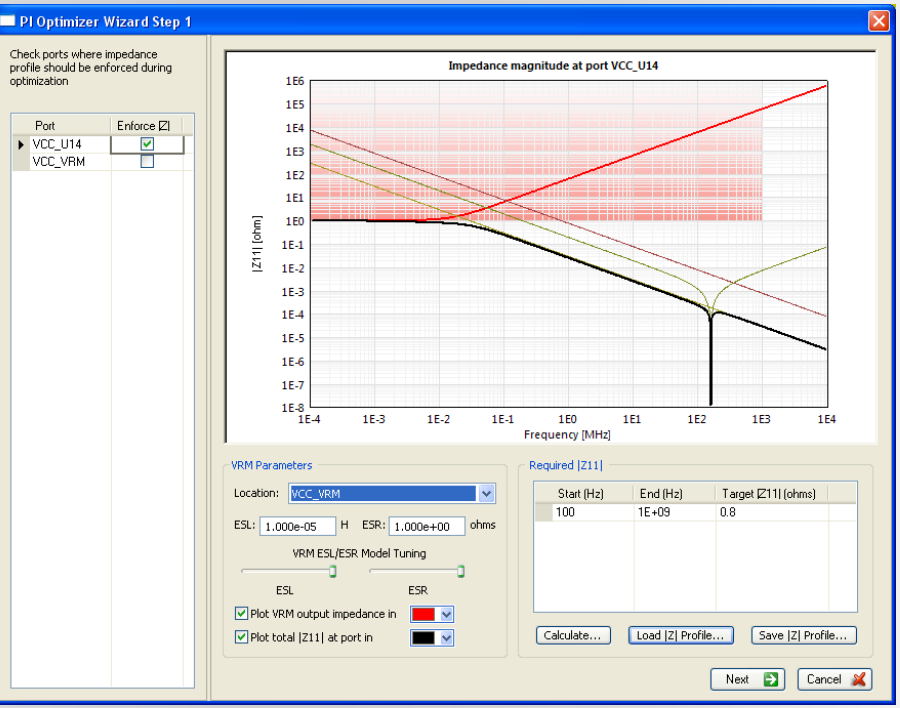
- PI Engineer may want to:
  - Increase capacitor count in order to make design more robust
  - Reduce the capacitor count
  - Reduce number of different capacitor types used
  - Redesign using lower cost capacitors
  - Chose appropriate capacitor location

Genetic Algorithm Setup

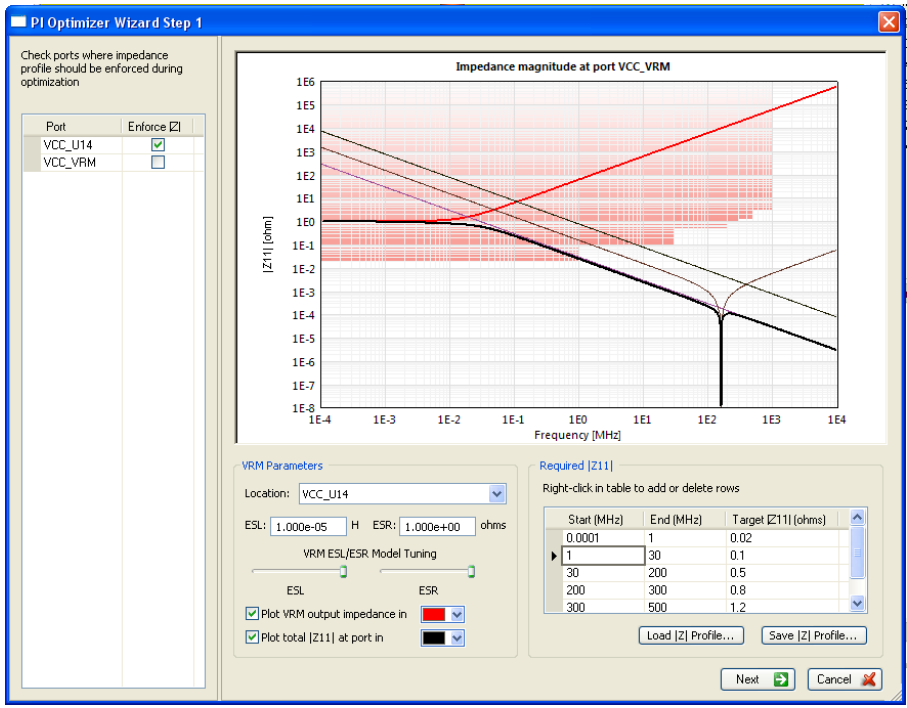
Optimized for Impedance
Optimized for # of Caps
Optimized for Capacitor Types
Optimized for Price

Automated PI Optimization
5 Easy Steps

1. Define Ports and Impedance Targets

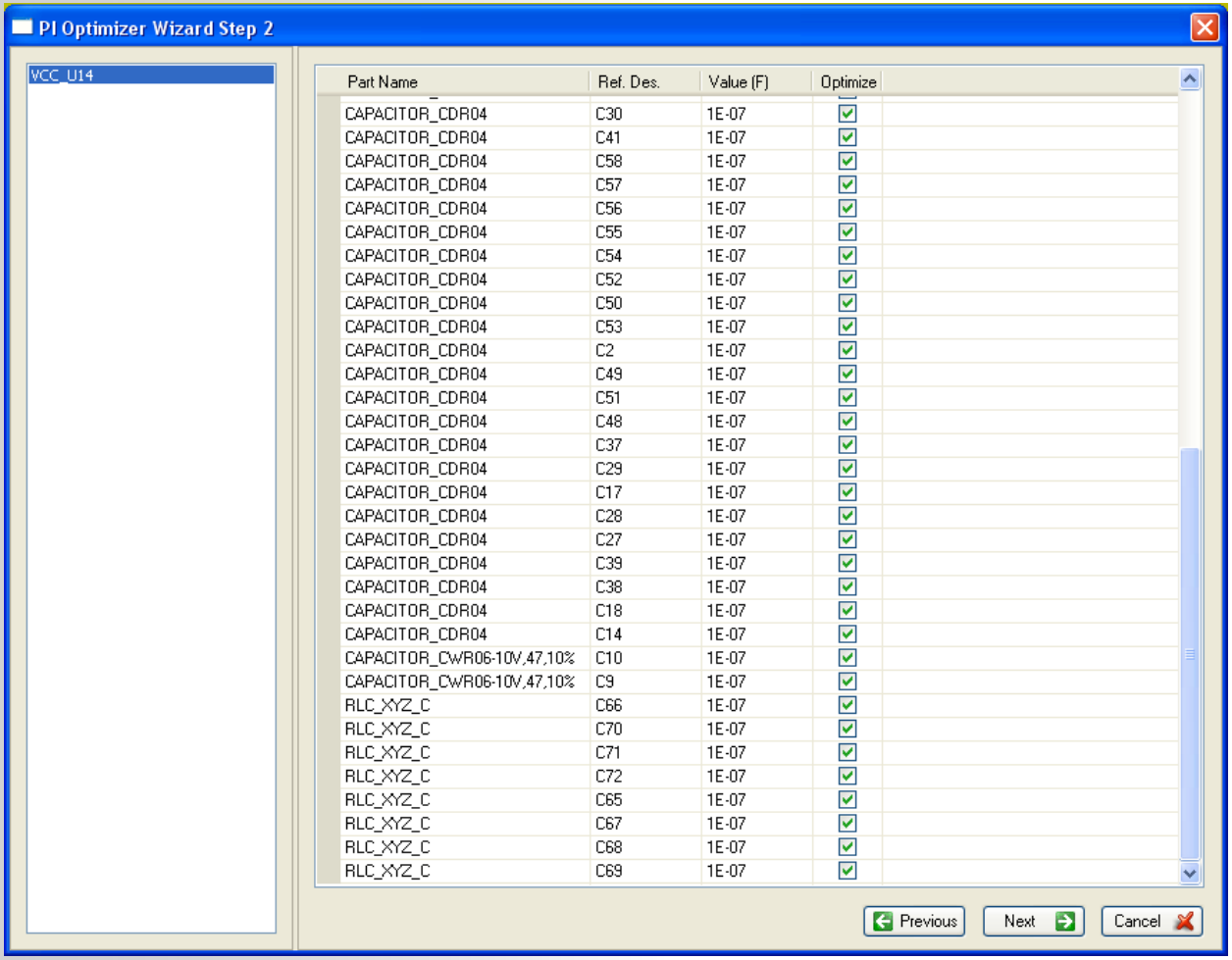


or



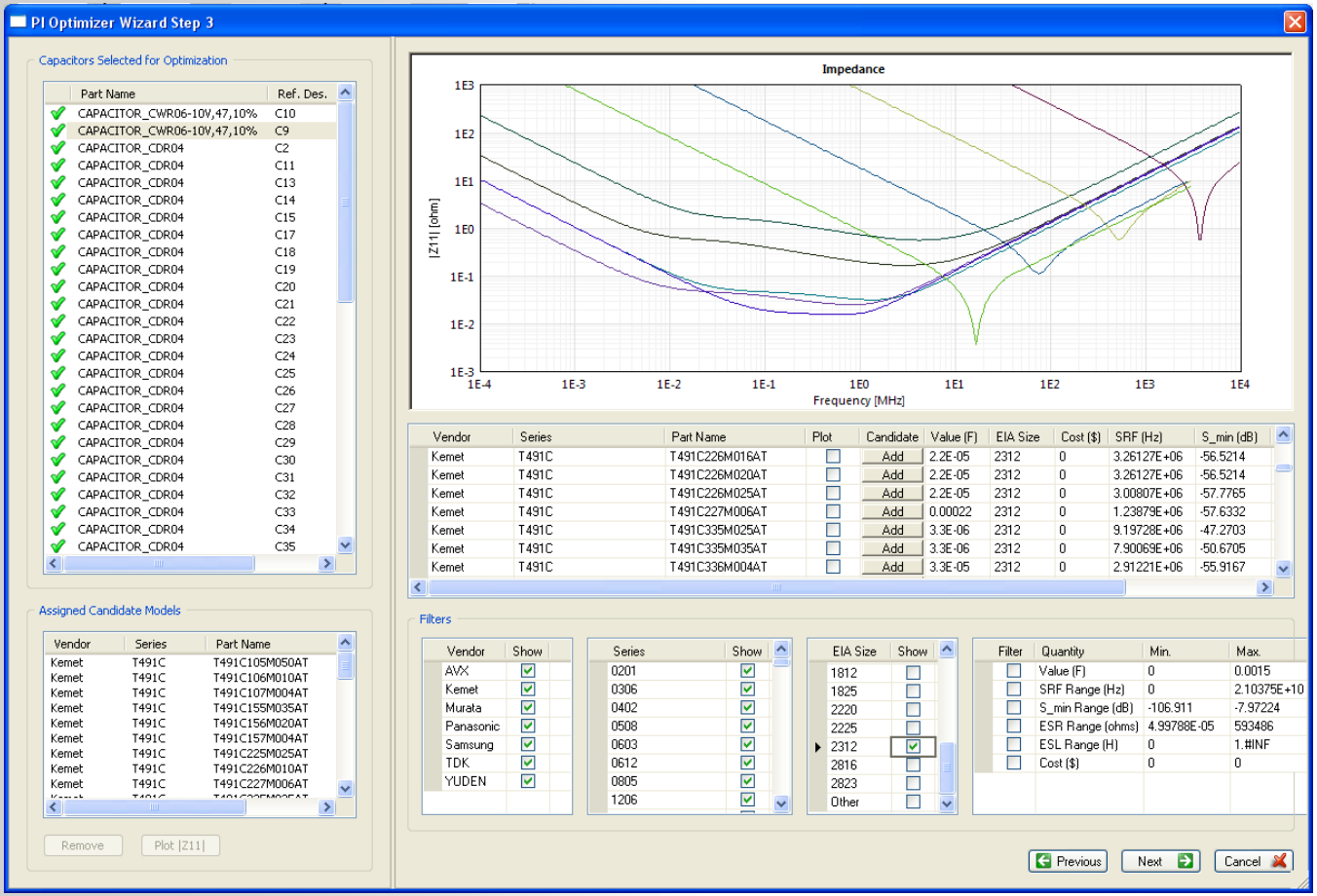
Automated PI Optimization
5 Easy Steps

2. Select Capacitors for Automated Optimization



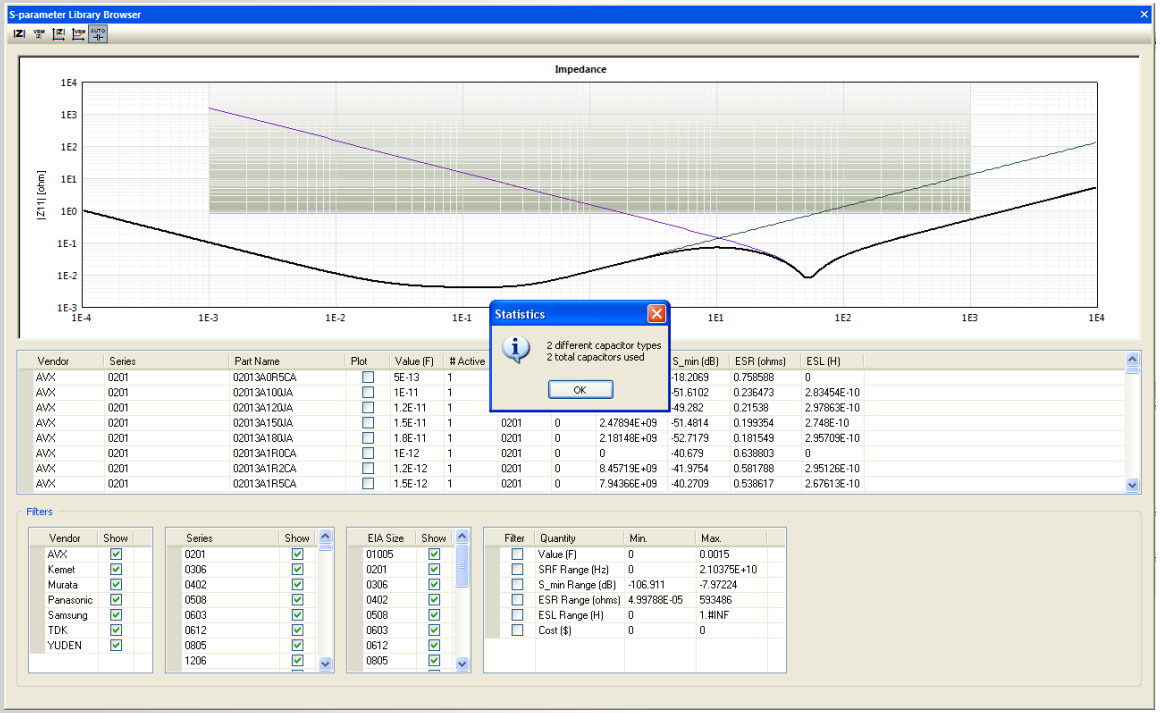
Automated PI Optimization
5 Easy Steps

3. Select Candidate Capacitors for Optimizer



How to Determine Candidate Capacitors

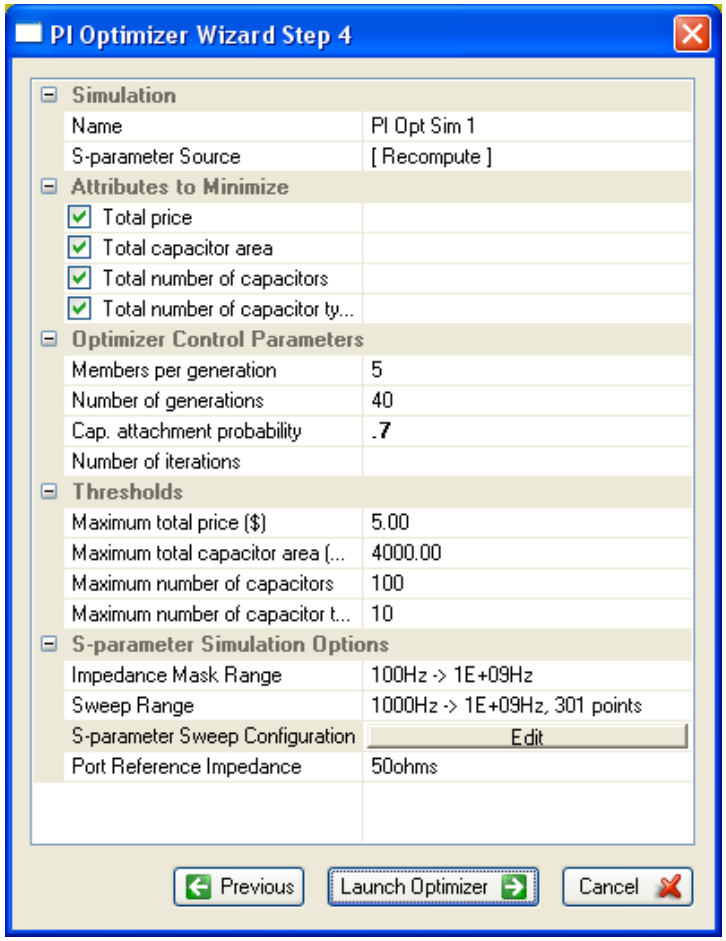
1. User choice based off of BOM
   - Enter capacitor selections
2. User choice based off of filtered selection
3. Automated selection using SimplePI



Automated PI Optimization
5 Easy Steps

4. Setup Optimization Criteria
   - Total Price
   - Total Number of Caps
   - Total Number of Cap Types
   - Total Capacitor Area
   - SYZ Sweep

5. Launch Optimizer and Analyze Results



Optimized Results Without Embedded Capacitance

Time = 15min 7sec

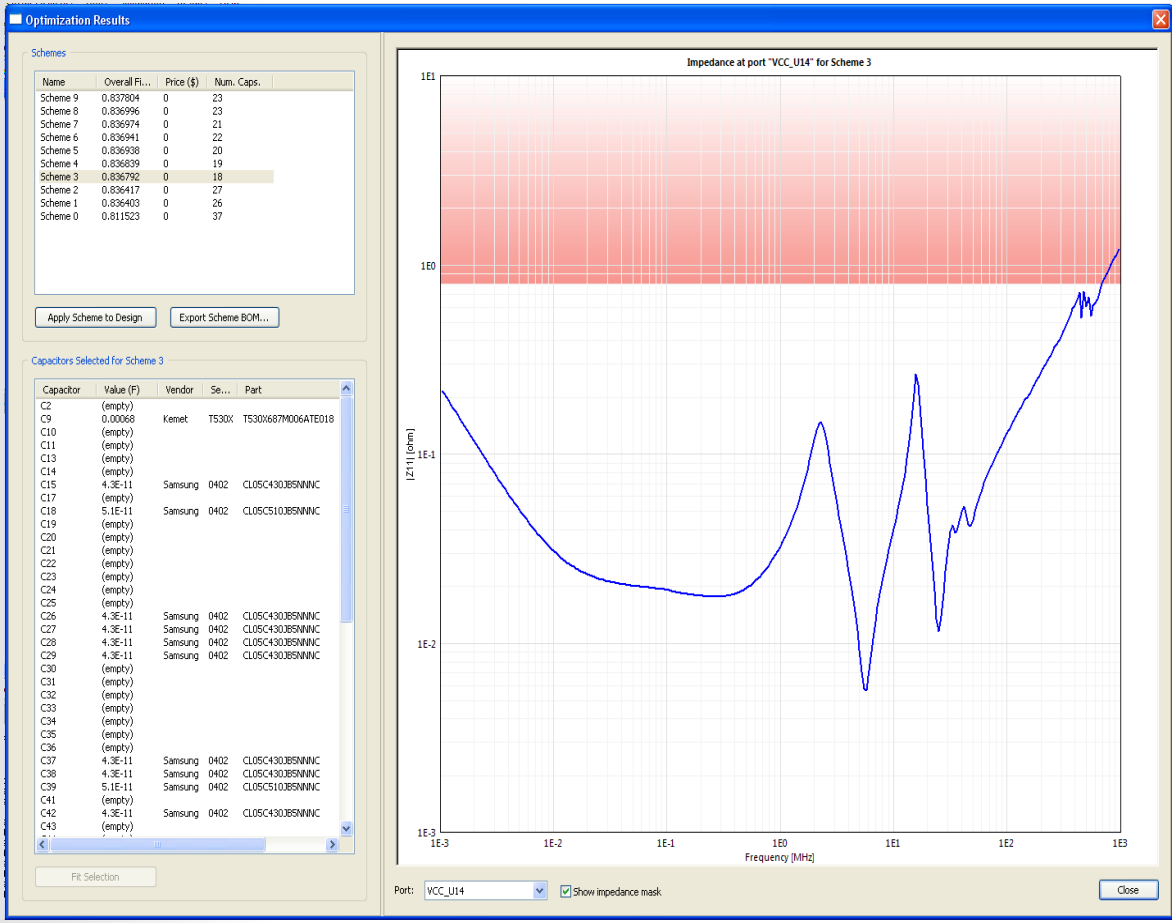
- **Frequency Setup**
  - **1KHz <= f < 1GHz**
  - **50 Points/decade**
- **Genetic Algorithm Setup**
  - **Optimized for Impedance**
  - **Optimized for # of Caps**
  - **Optimized for Capacitor Types**
  - **Optimized for Price**
  - **100 Members**
  - **1000 Iterations**

Original solution

- **Total # Caps: 74**
- **Capacitor types:**
  - **All ideal**

Optimized Solution

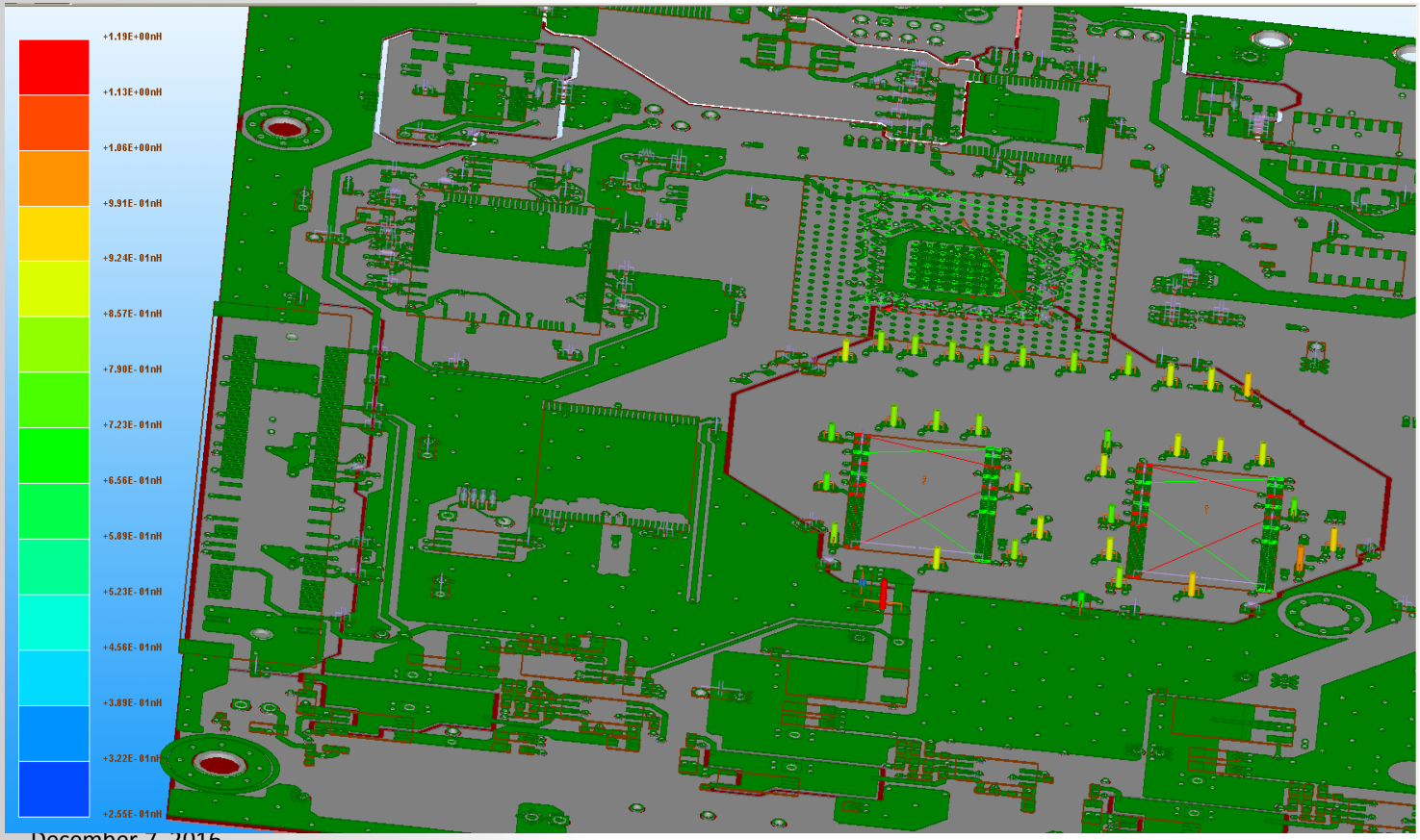
- **Total # Caps: 18**
- **Capacitor Types = 5**
  - **AVX, Samsung, and Kemet**



Loop inductance

After running an optimization in PI advisor right-click the PI Advisor Simulation name in the Results workspace to obtain the loop inductance between each port/capacitor

Provides intuitive plot to analyze capacitor layout thereby minimizing loop inductance



ANSYS

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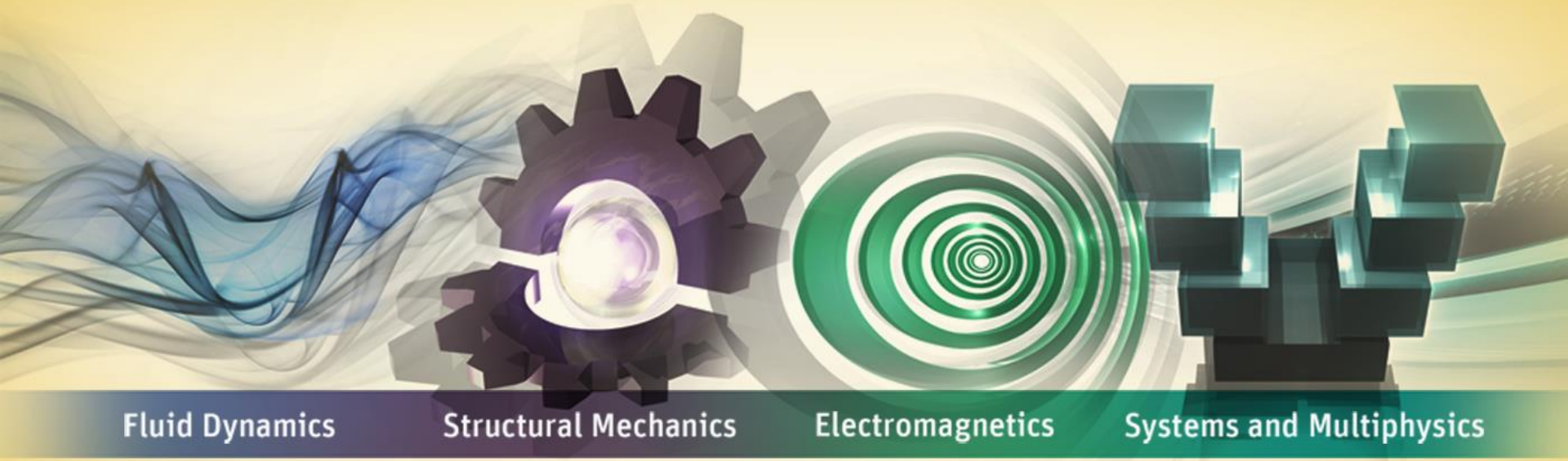
EMI/ EMC simulation Basics



EMC Analysis

First design and optimize PDS

- **Low plane impedance**
- **Minimal resonances**

Perform FFT of transient waveforms

- **Add current/voltage sources at IC locations**
- **Measure Near/Far fields in Frequency band of interest**

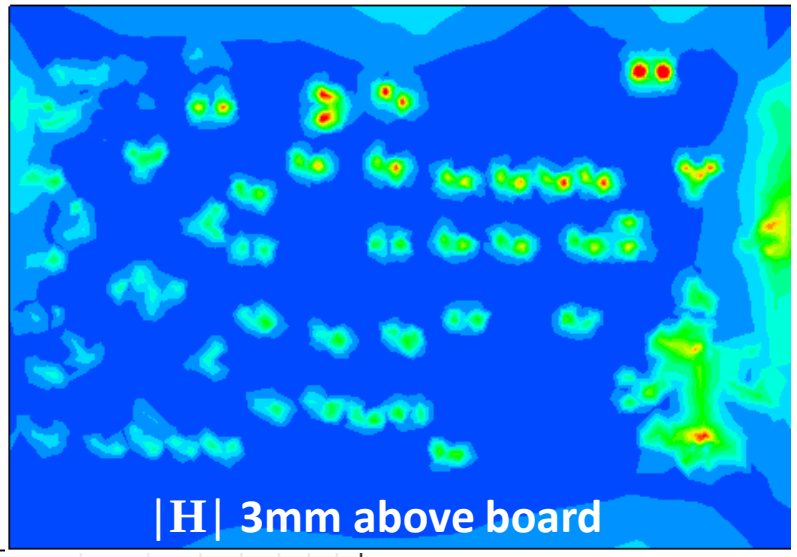
Place PCB/PKG in enclosure model

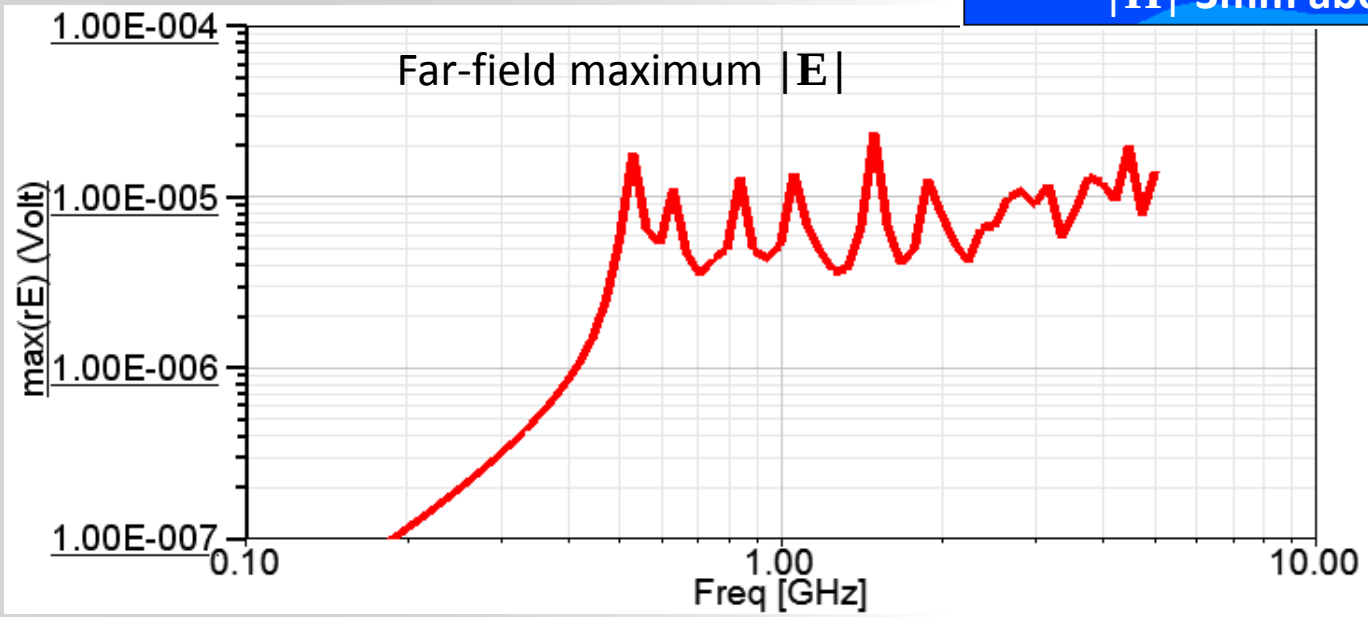
- **Plot fields using HFSS**
- **Measure effects of shielding**

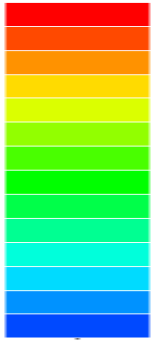
SIwave Analyses

Far/Near-field Calculation

- Explicit field is calculated from SIWave solution
- Far/Near-field Green's function is used to determine fields in all space.







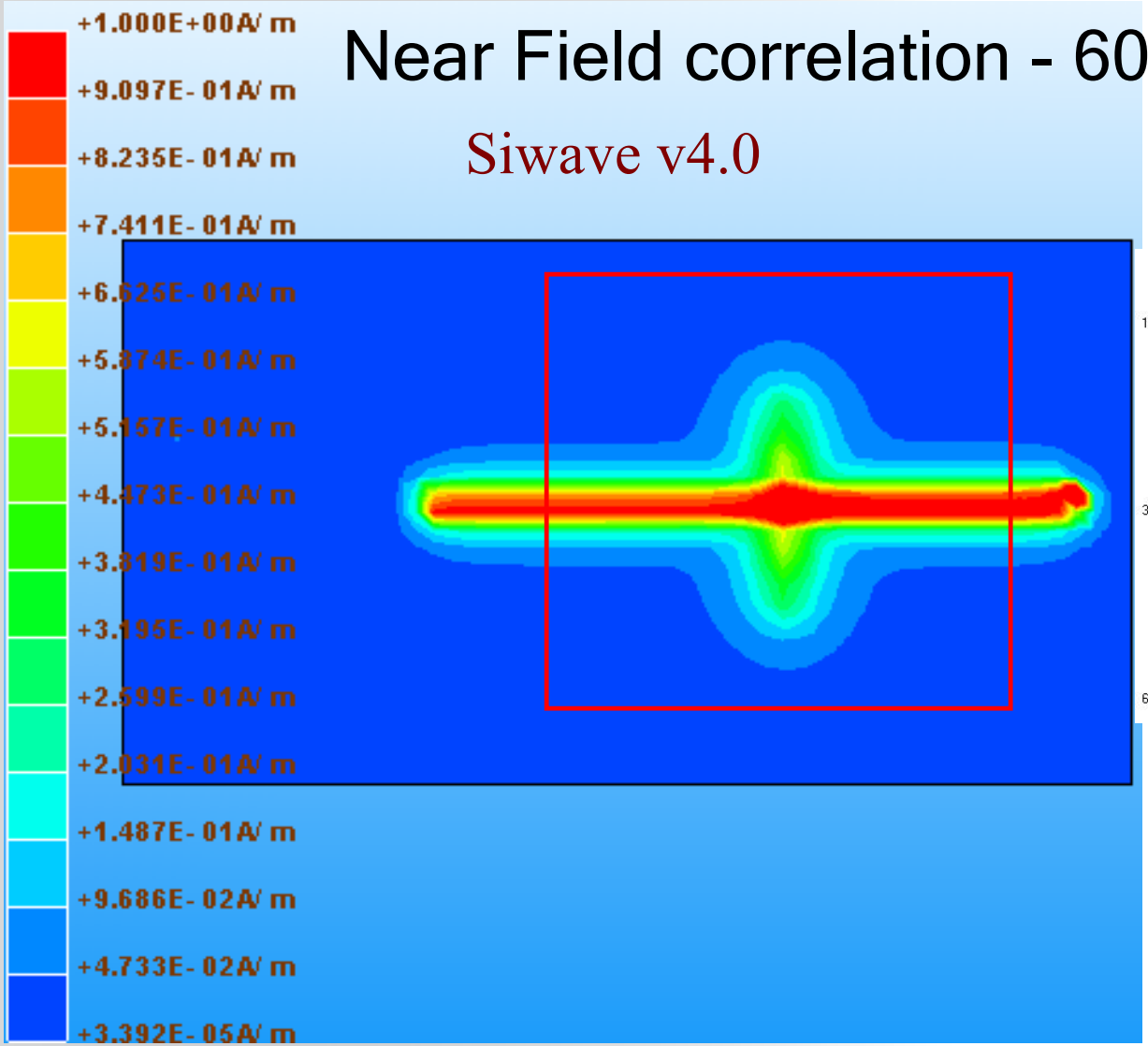
1.0E-5 A/m

1.0E-9 A/m

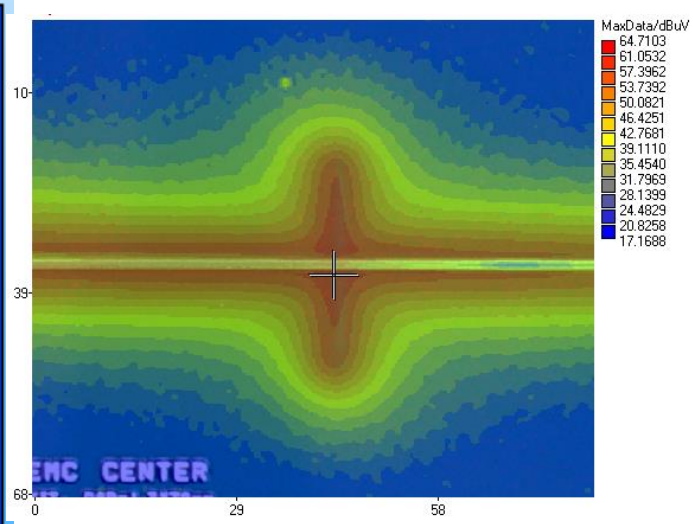
SIwave - Near Fields

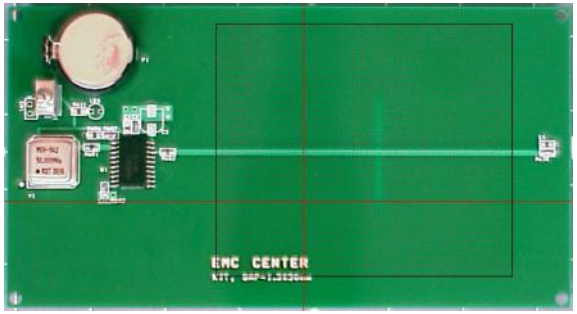
Near Field correlation - 60mm slot length

Siwave v4.0

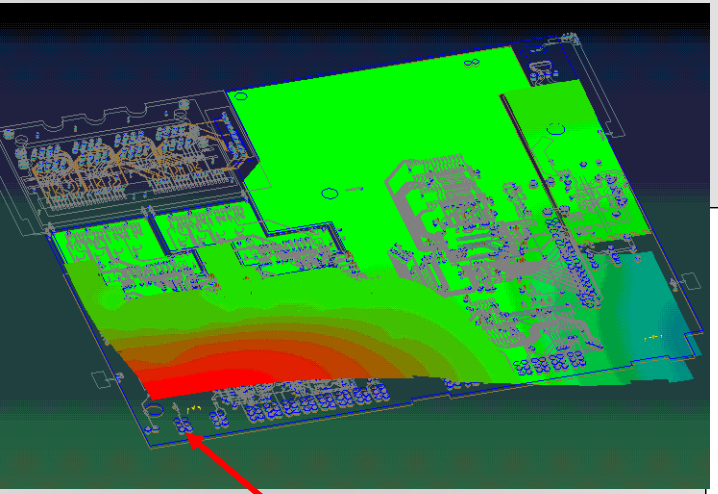


Measurement

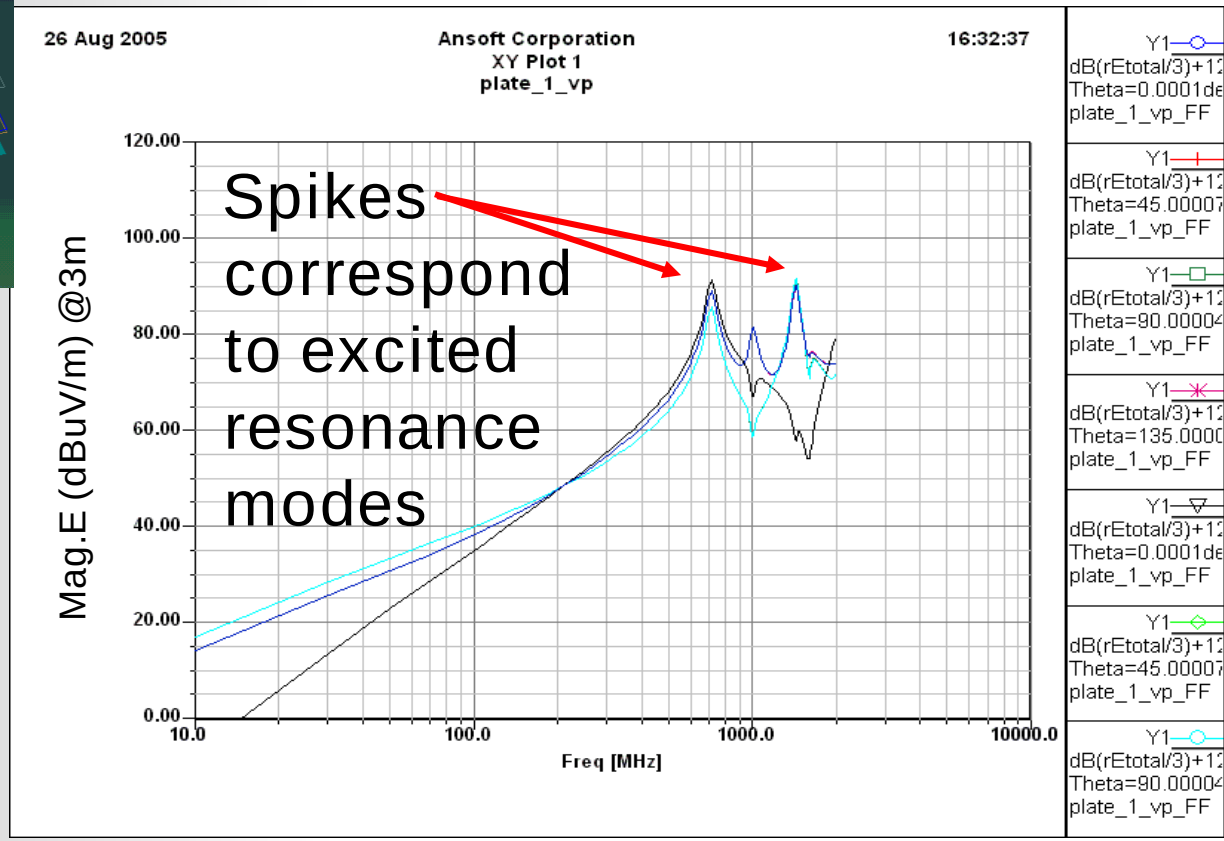




SIwave - Far Field Plotting



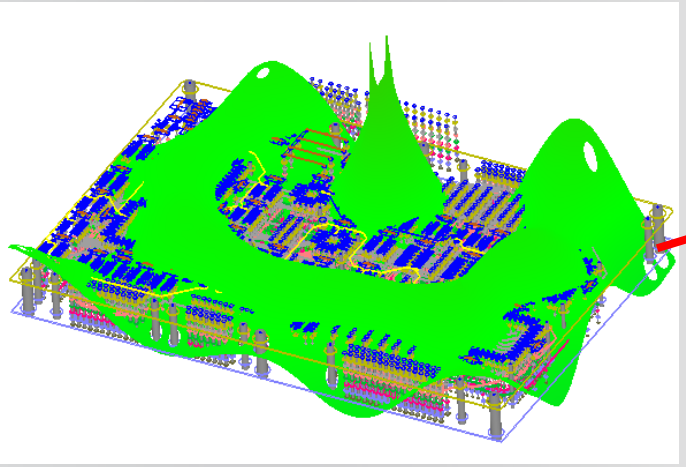
Add sources to physical location of ICS and specify max current draw or voltage

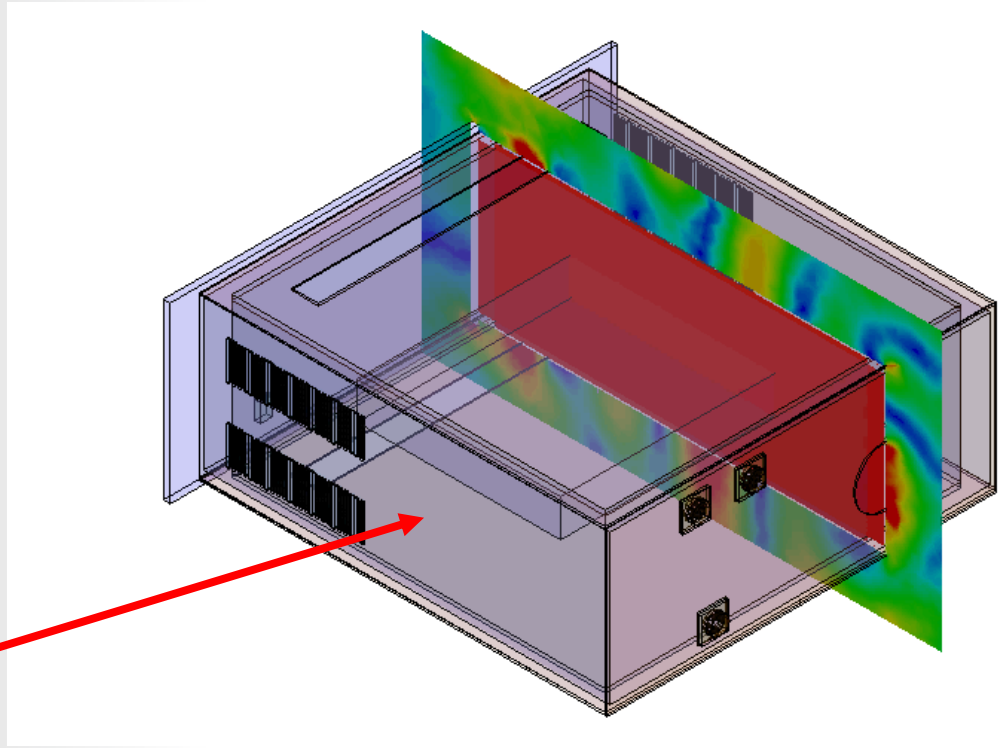


Emission test plot @ 3m

Shielding Analysis

SIwave field solution can be used as a radiation source for HFSS





Dynamically link SIwave to HFSS to plot the field strengths around the enclosure

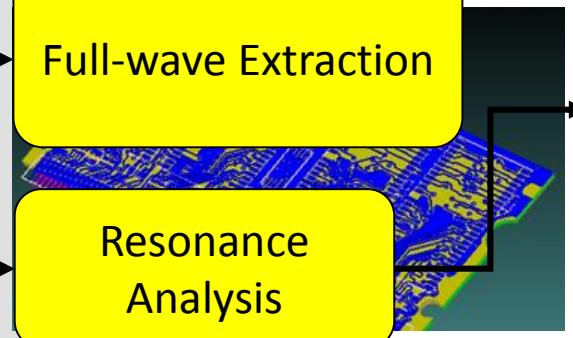
System Analysis (Verification)

- **Design Setup for System Analysis**

Import PCB and Component Definitions from 3rd Party Layout

Full-wave Extraction

Resonance Analysis

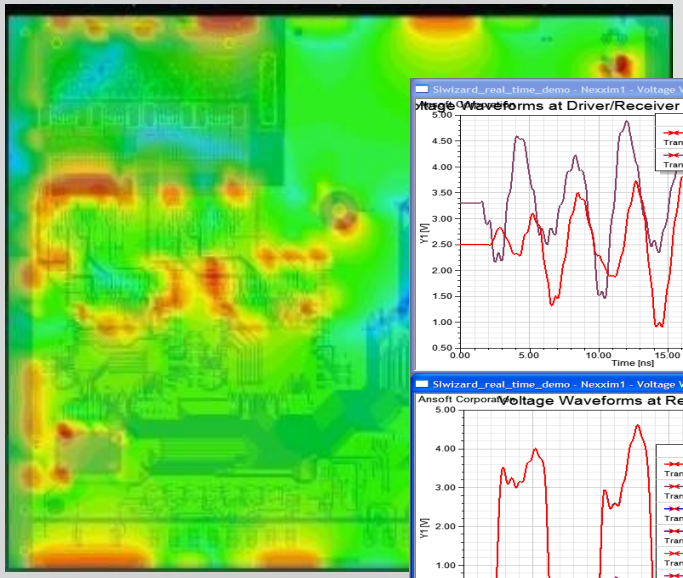


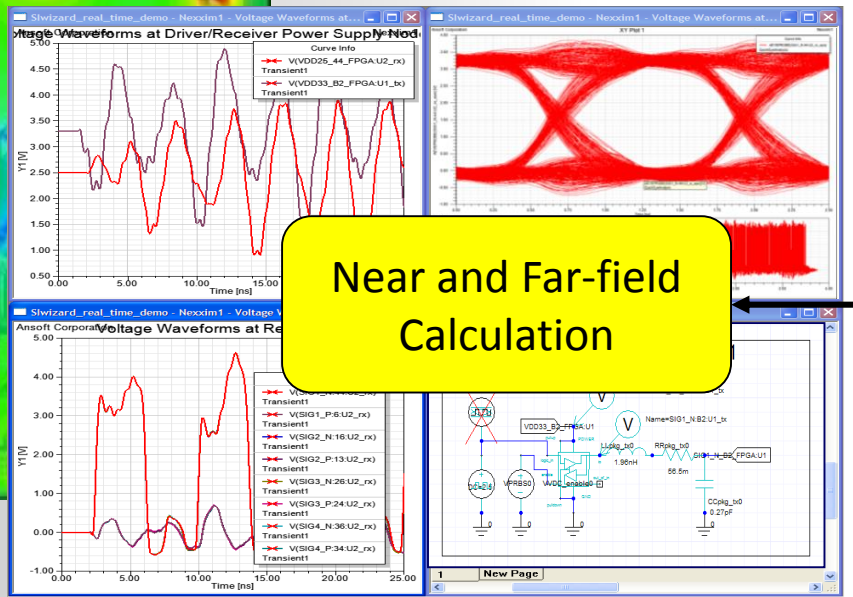
Set up Drivers/Receivers

Schematic generation

Transient circuit analysis

Near and Far-field Calculation





What is a Full System EMI/EMC Methodology

State of the art EMI/EMC simulation method that

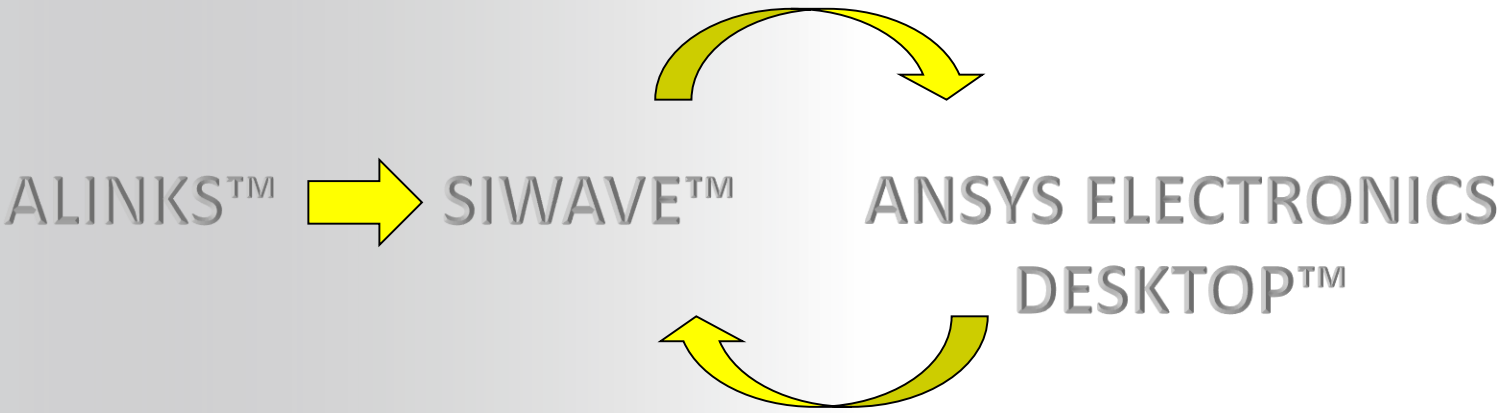
- Utilizes the best in class tools
- Incorporates physical board layouts
- Uses real world transient signals
- Takes into account full 3D enclosures
- Seamlessly combines frequency and time domain simulation tools to predict EMI

What are the tools needed?

- Board analysis > SIwave
- Full 3D enclosure > HFSS
- Realistic clock/timing, and digital signals > AEDT
- CAD links > ALinks

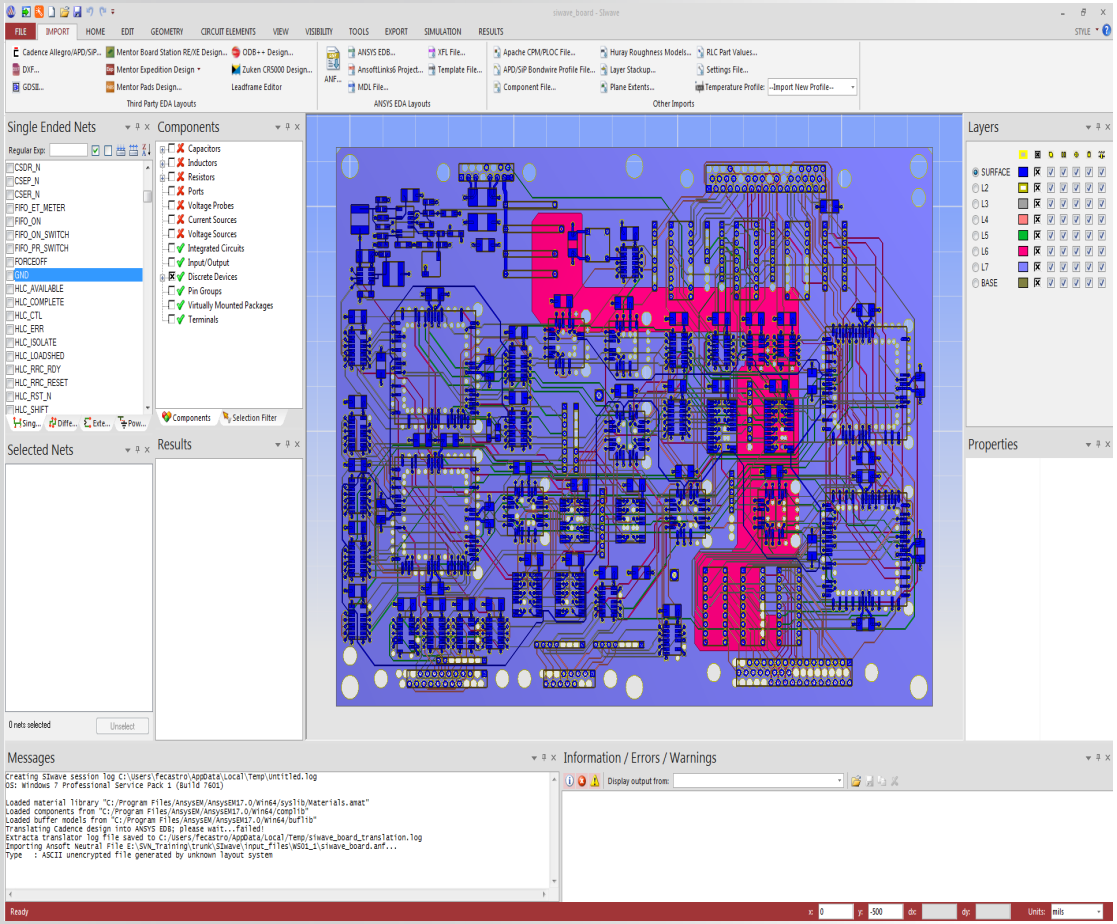
What are the steps ?

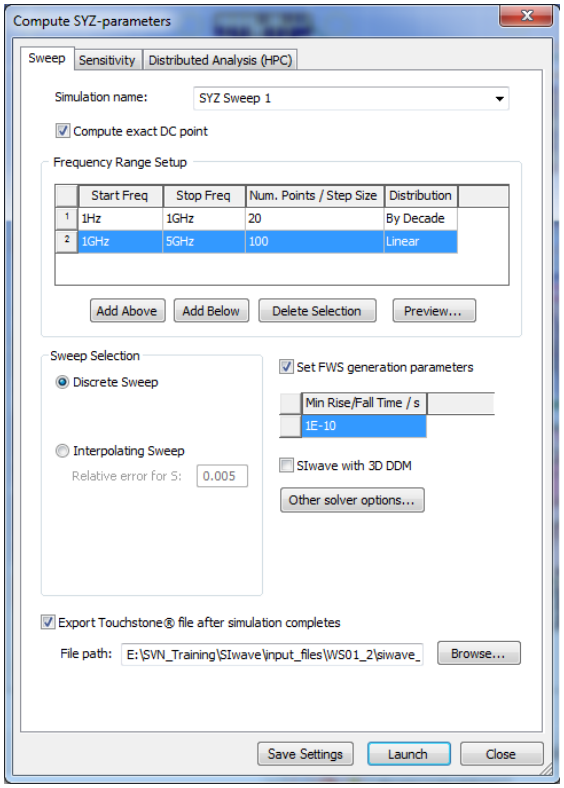
1. Import PCB layout into ALinks or SIwave
2. Perform analysis of PCB in Siwave
3. Dynamically link SIwave results into ANSYS Electronics Desktop (AEDT) – Circuit Design
4. Attach drivers and receivers in AEDT to linked SIwave model
5. Perform a time/frequency domain analysis of entire system in AEDT
6. Push voltage/excitation levels back to SIwave
7. Dynamically link the SIwave model into AEDT – HFSS Design
8. Solve the full system in AEDT – HFSS Design



The SIwave simulation

1) Layout in eCAD tool is imported into SIwave



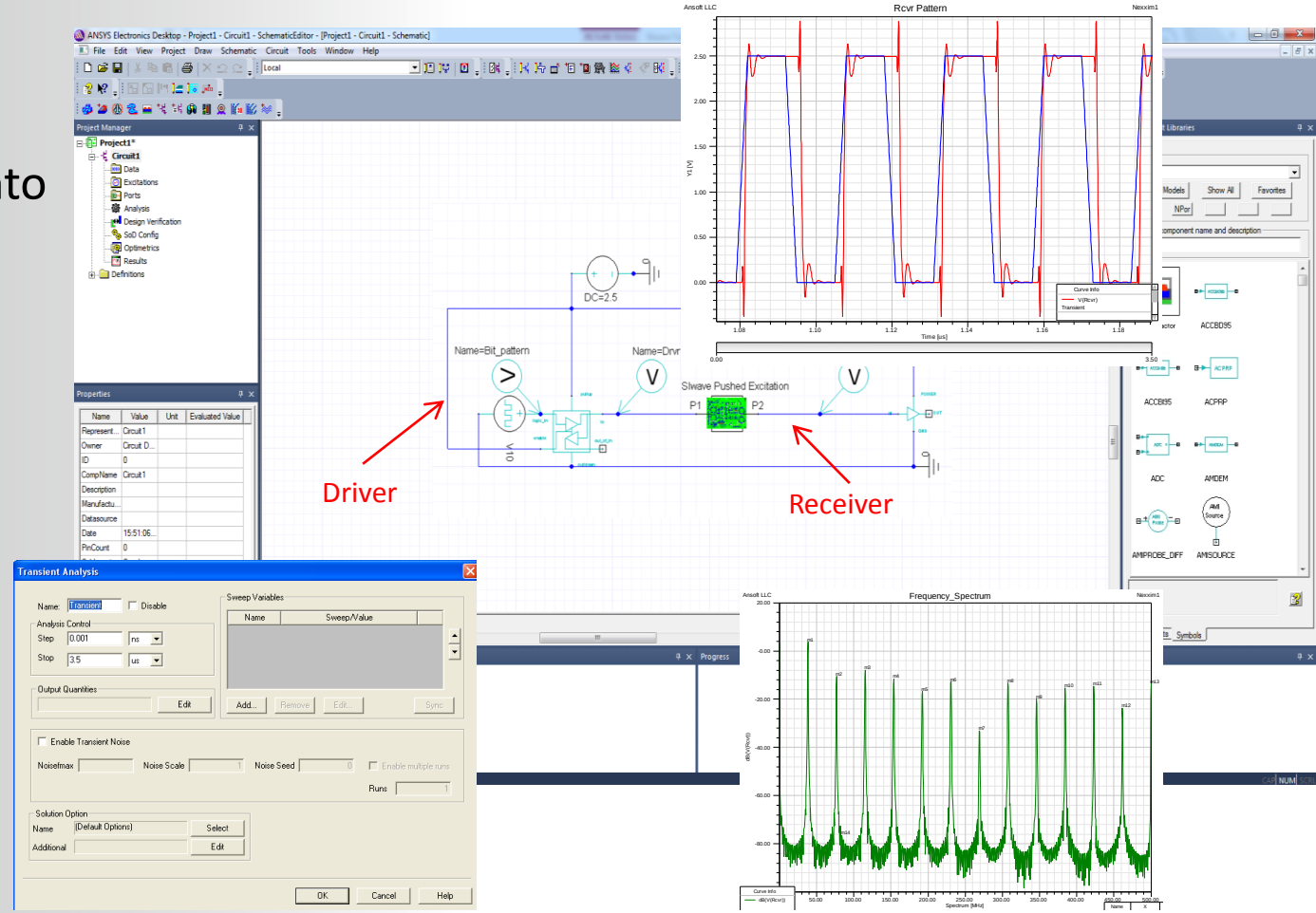


1a) Simulation is setup and run

The AEDT Simulation

2) SIwave model is dynamically linked into AEDT

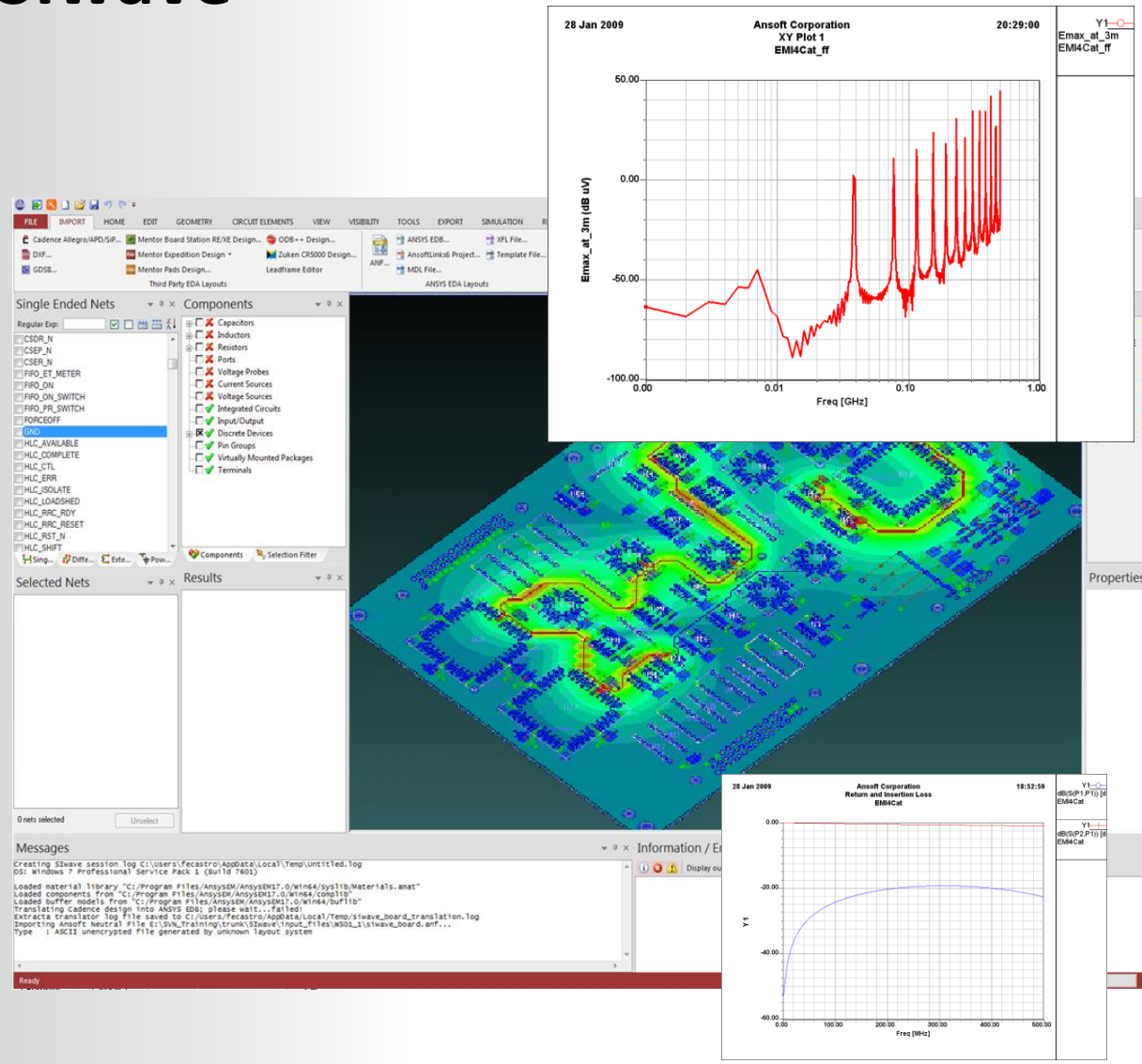
2a) Drivers and receivers are added to the circuit and simulated



Back to SIwave

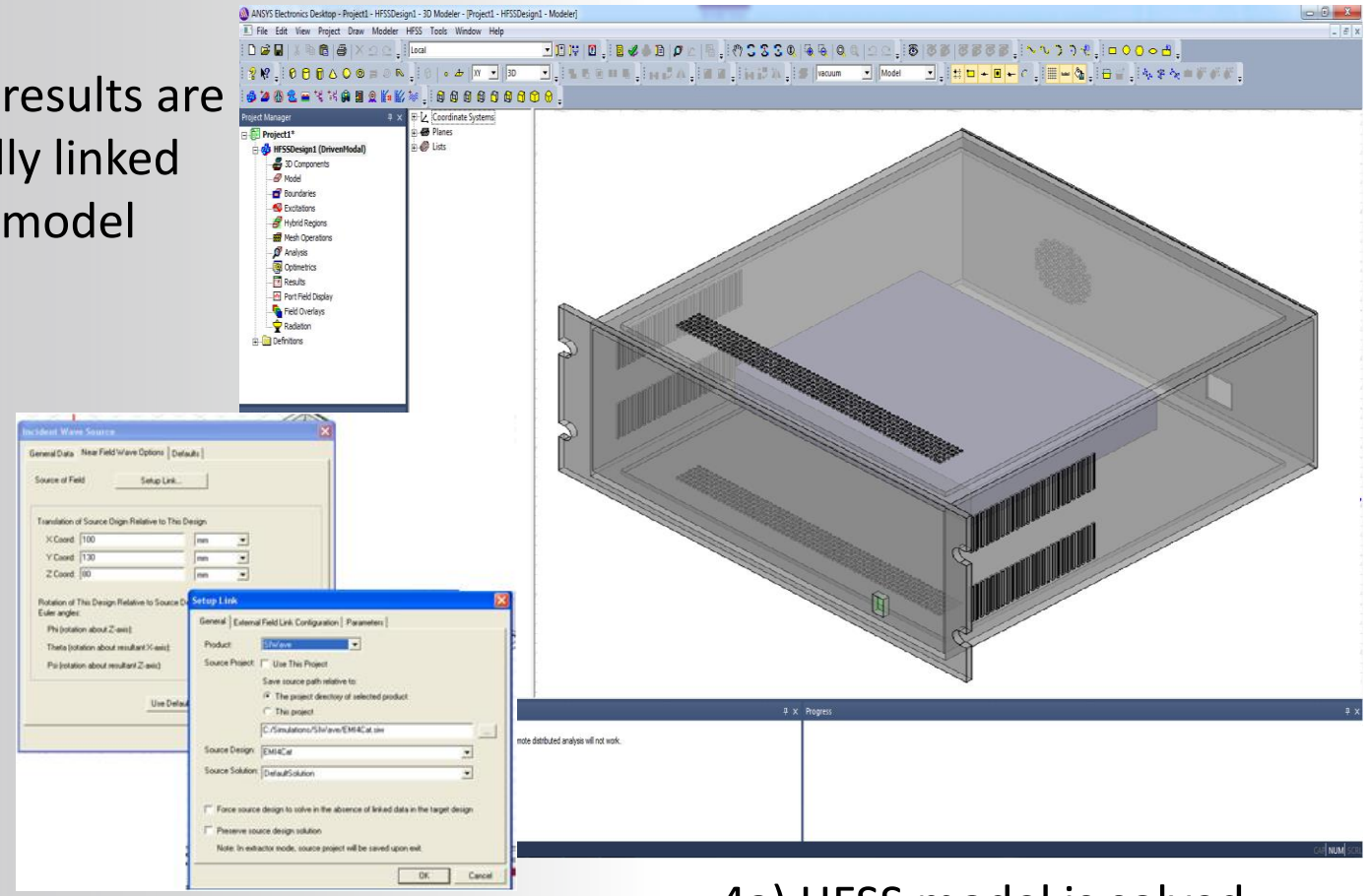
3) Results from AEDT are pushed back into SIwave

3a) Fields near to the PCB are calculated



Linking to HFSS

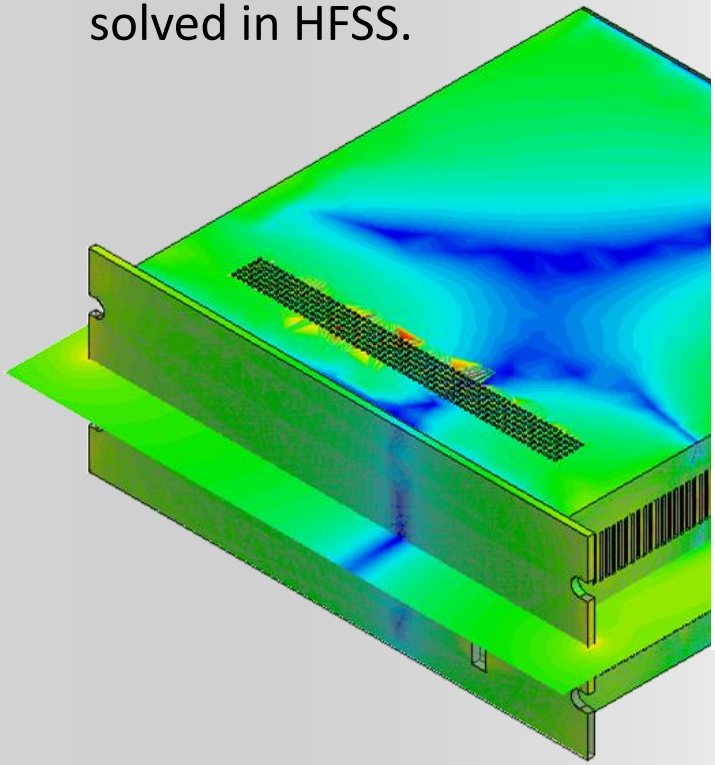
4) Siwave results are dynamically linked into HFSS model

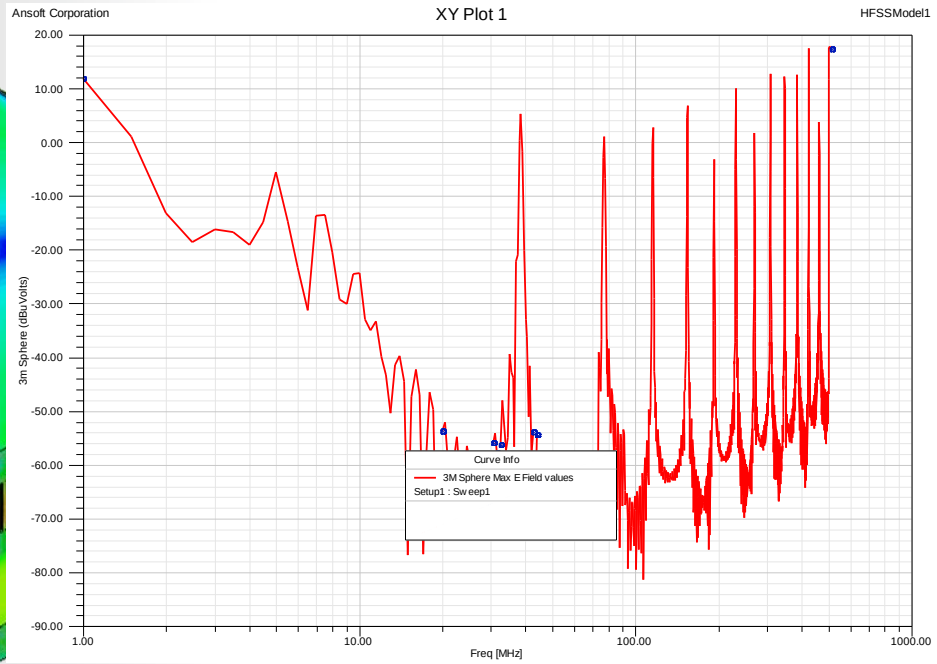


4a) HFSS model is solved

Finishing the System Simulation

5) Entire System is solved in HFSS.





5a) Results are plotted

Workshops

Siwave_radiation.pdf

Siwave_dynamic_link.pdf

Accessing the ANSYS Customer Portal

https://support.ansys.com/portal/site/AnsysCustomerPortal/

Registration and login information can be requested from us