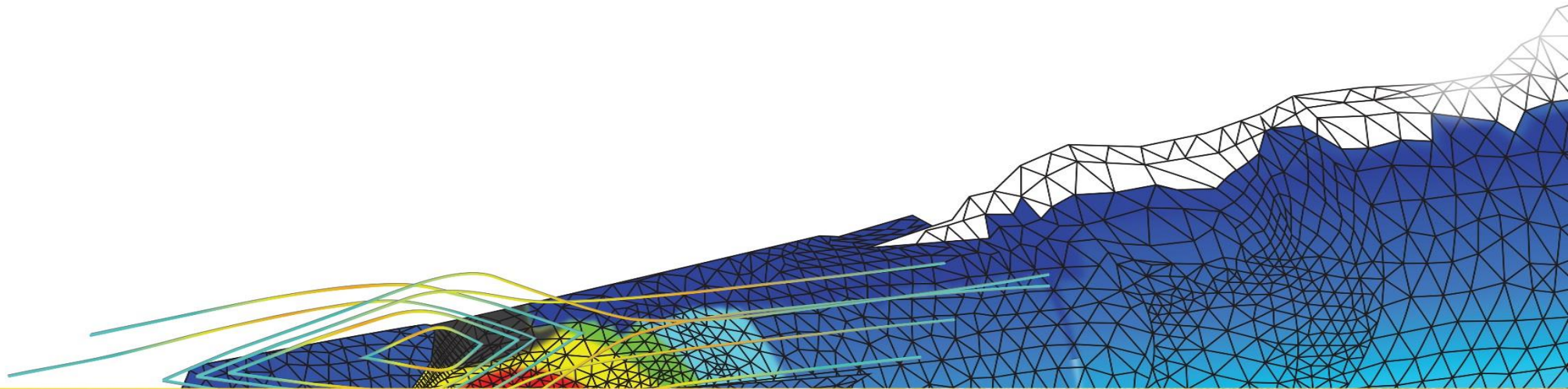


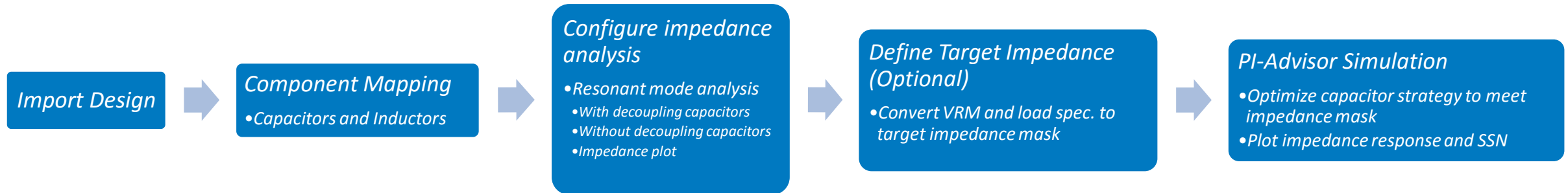


Workshop 03: Advanced Power Integrity Simulation



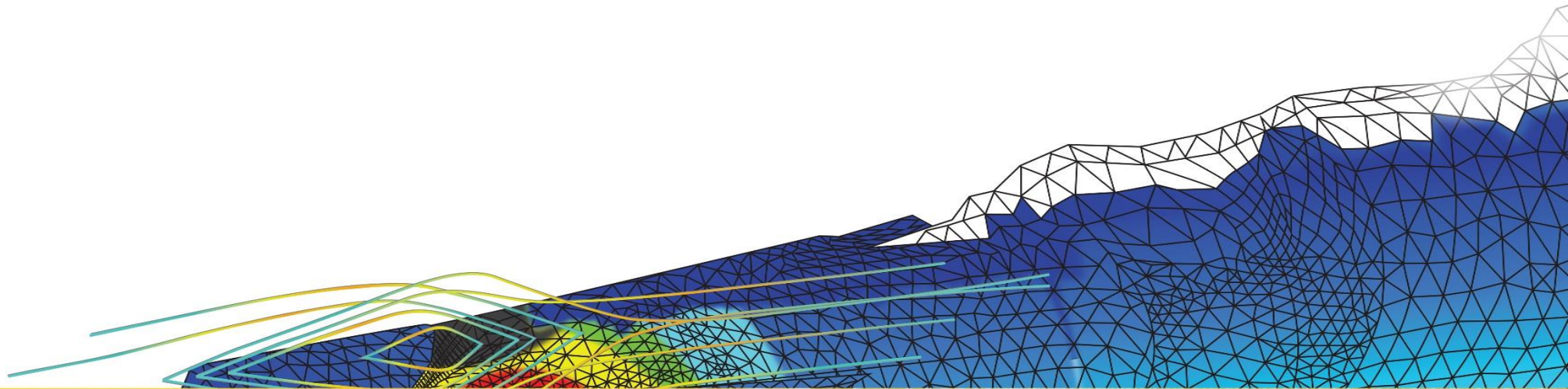
Overview

- This Workshop shows the process of setting up a PI Advisor simulation for a PCB design to validate and optimize the decoupling strategy using ANSYS SIwave



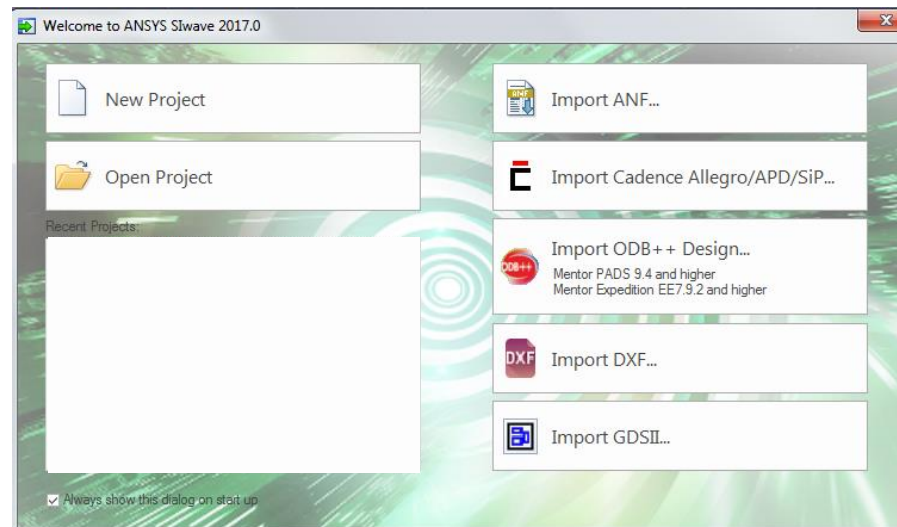


Import Design



SIwave for Impedance Analysis

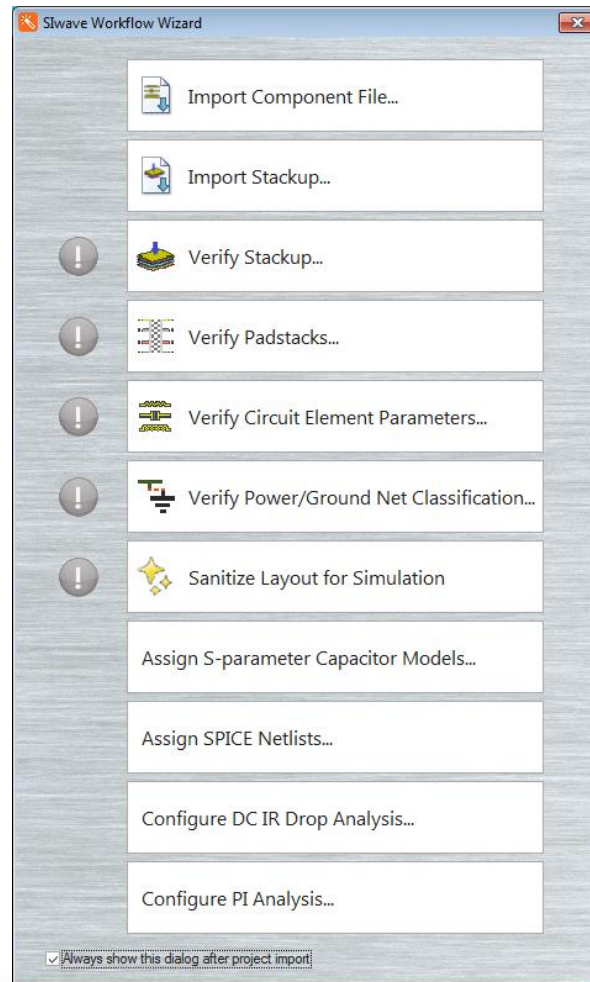
- Starting SIwave
 - To launch SIwave, click the Microsoft Start Button, select: *All Programs → ANSYS Electromagnetics → ANSYS Electromagnetics Suite 18.0 → ANSYS SIwave 2017*
- Load design File
 - Click the **Open Project** box
 - Navigate to the training files and choose: *PI_Advisor_example.siw*
 - Press **Open**



SIwave Workflow Wizard Dialog

- Opening the Workflow Wizard

- In the Common Functions menu, click **SIwave Workflow Wizard** Dialog button



(Optional) Import Settings
from Previous Simulation

**Verify / Modify Geometry,
Materials, and Circuit Elements**

(Optional) Pre-process Overlapping Geometry

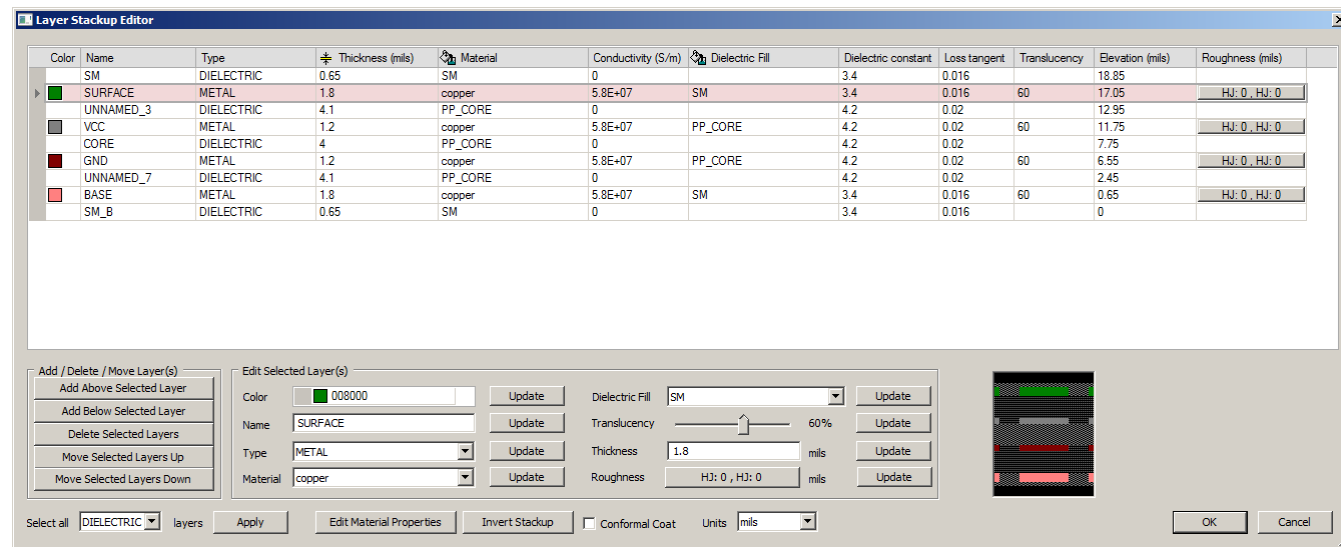
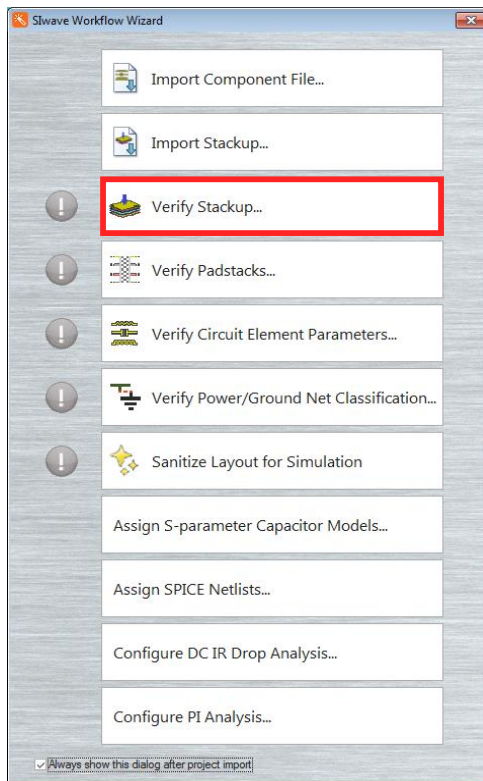
(Optional) Assign Broadband Models

Setup Simulation

Verify Stackup

• Modify Stackup and Material Properties

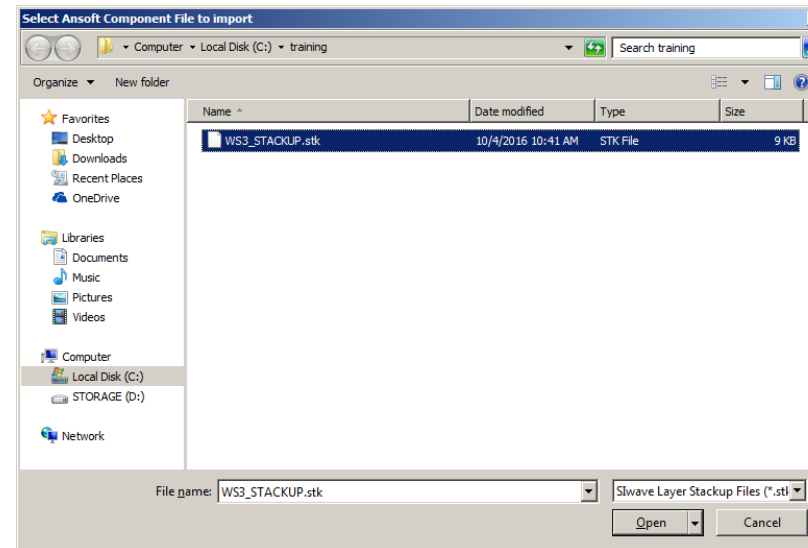
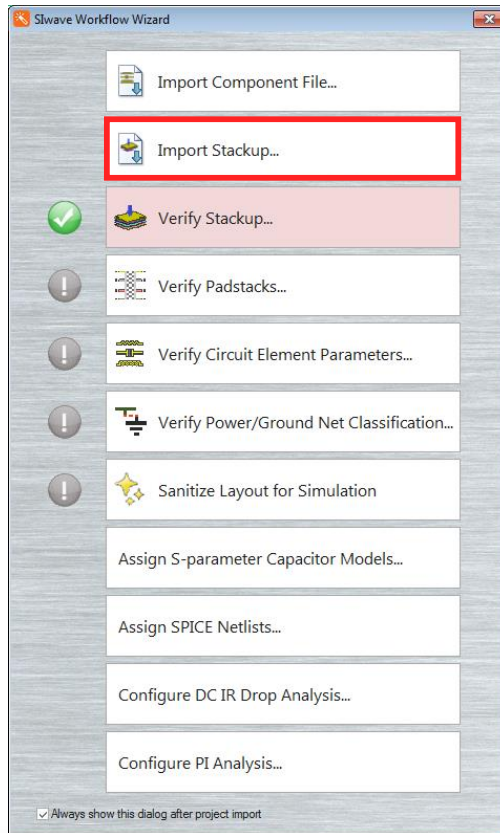
- Click on the **Verify Stackup** button.
 - This is the stackup from the original import. We would like to use a stackup generated from a previous design.
- Click Cancel to close this window.



Import Stackup

- Importing a Stackup from a Previous Design

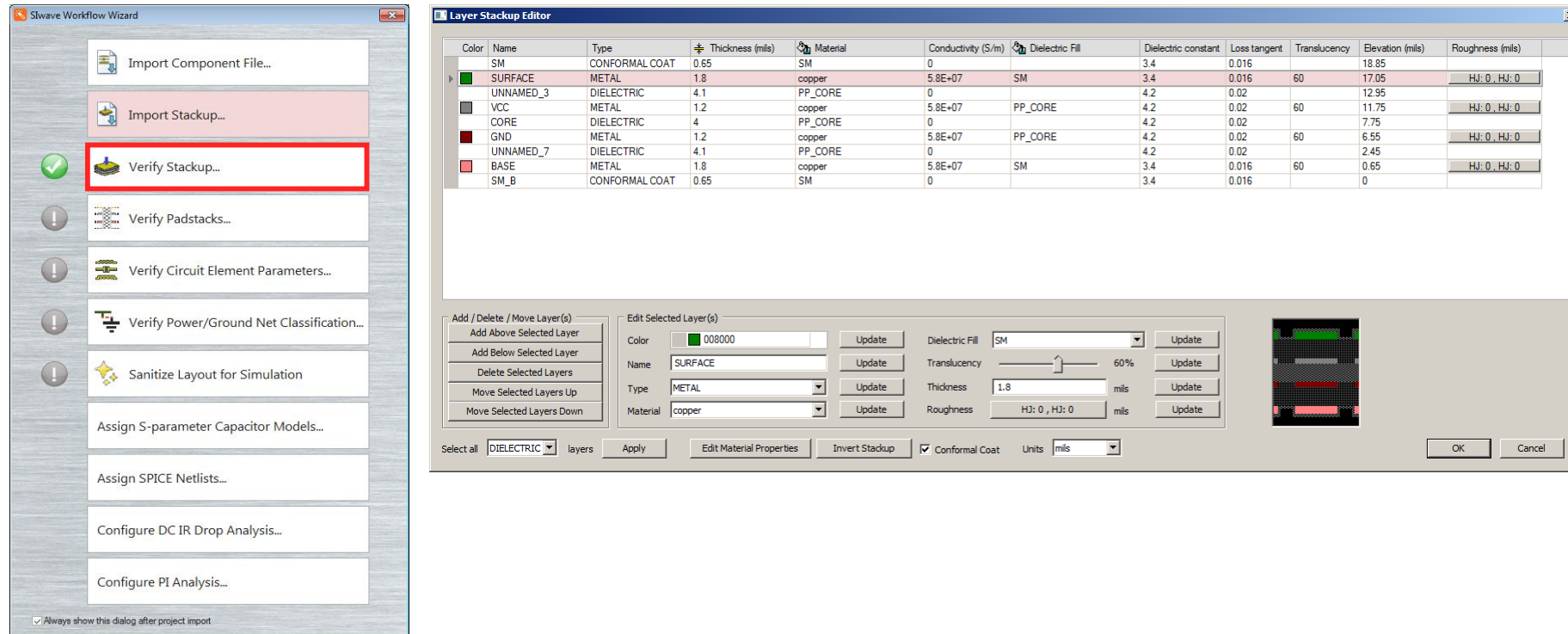
- Click the Import Stackup button.
- Locate **WS3_STACKUP.stk** in the same directory as the Slwave file
- Click Open to apply the stackup.



Verify Stackup

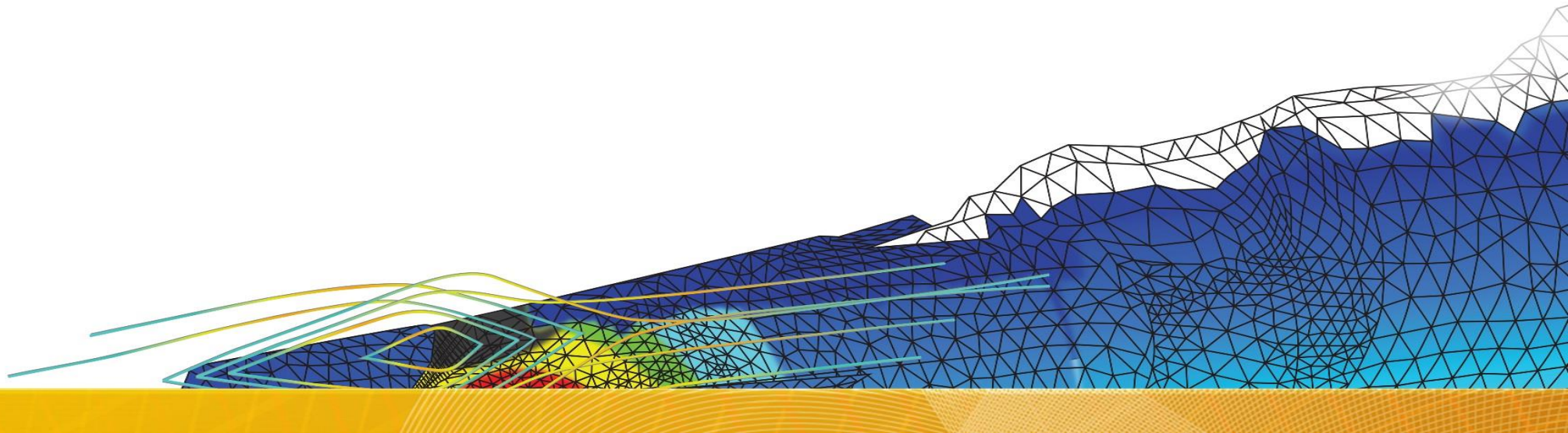
• Verify Imported Stackup

- Click on the Verify Stackup button once again.
 - Importing the stackup from the last step has modified the material for metal layers. Importing the stackup can modify any and all parameters in this window.
 - Verify that the outer dielectric layers are now of type conformal coat.
- Click Cancel to close this window.





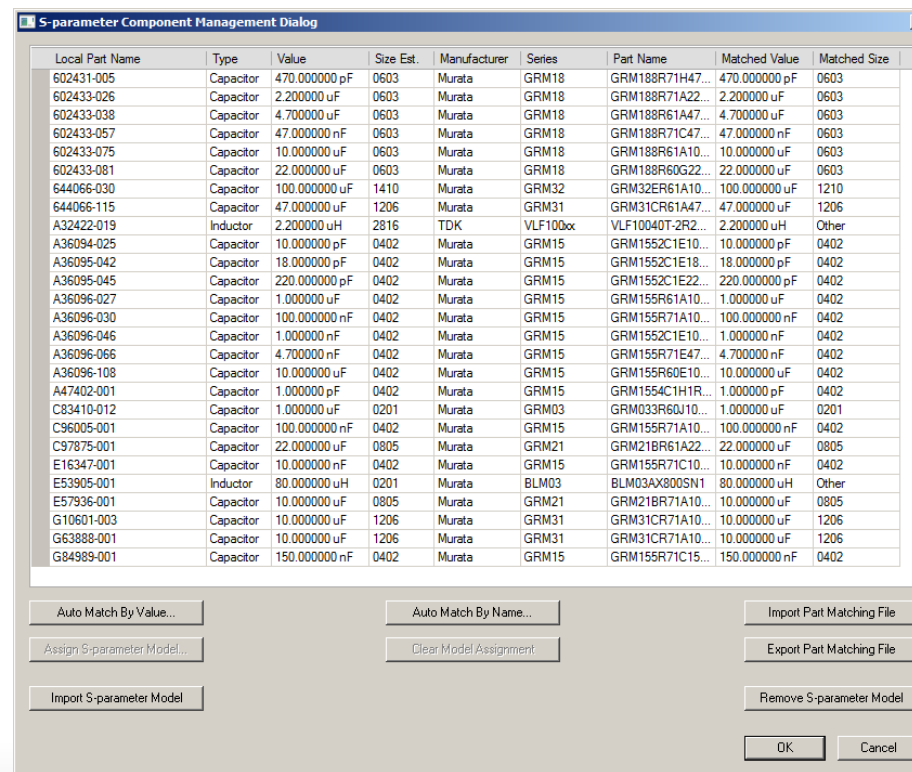
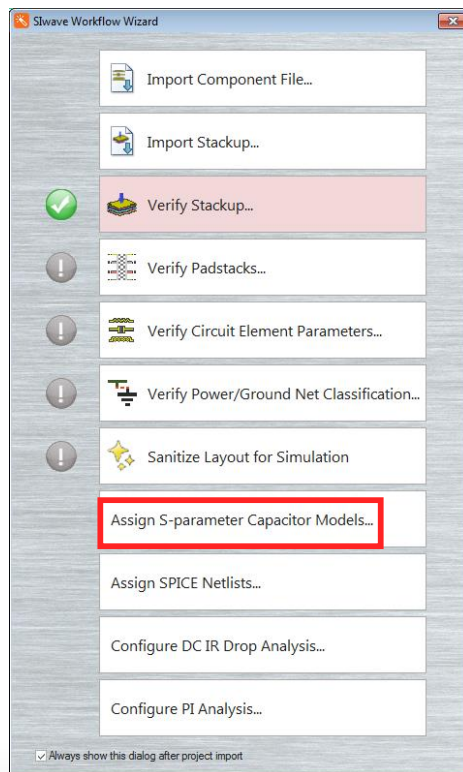
Component Configuration



Verify S-parameter Capacitor Models

- Assigning Broadband Models to Capacitor Locations

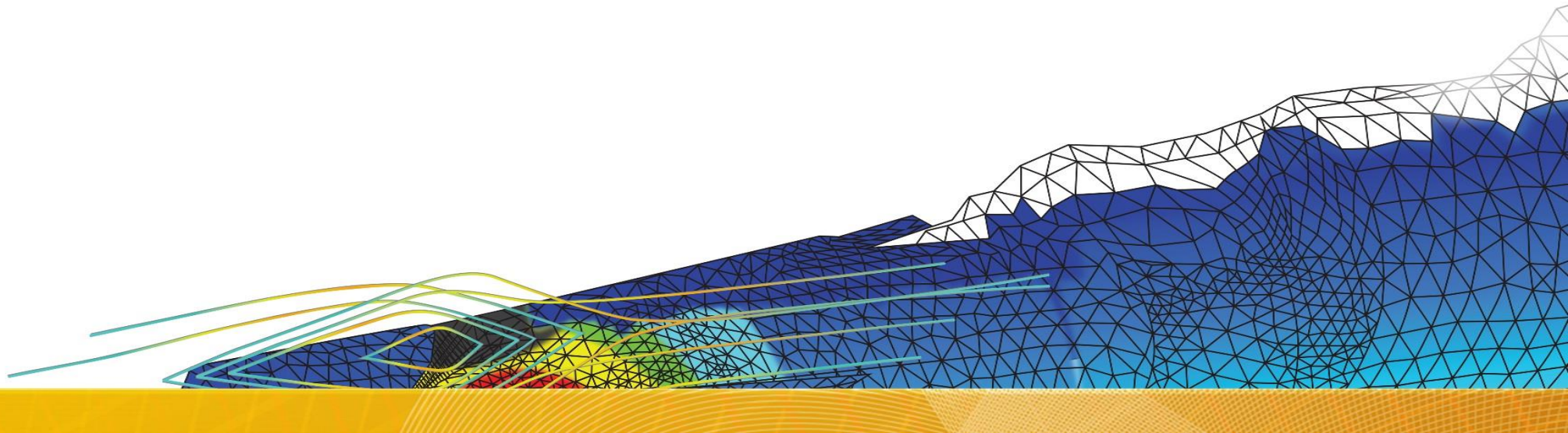
- For this exercise, we will assume that the Padstacks, Circuit Elements, and Power/Ground Net Classification has been handled properly during import.
- Click on the **Assign S-parameter Capacitor Models** button.
- Verify that each local part name has an associated S-parameter model.
 - The **PI_advanced.pmap** file in the workshop files directory maps each local part to a suitable part from Siwave's vendor library. The vendor library includes **over 20,000 capacitor and inductor models** directly from **12 of the major vendors**. The pmap file was exported after manual setup using this dialog.
- Click Cancel to close the dialog.



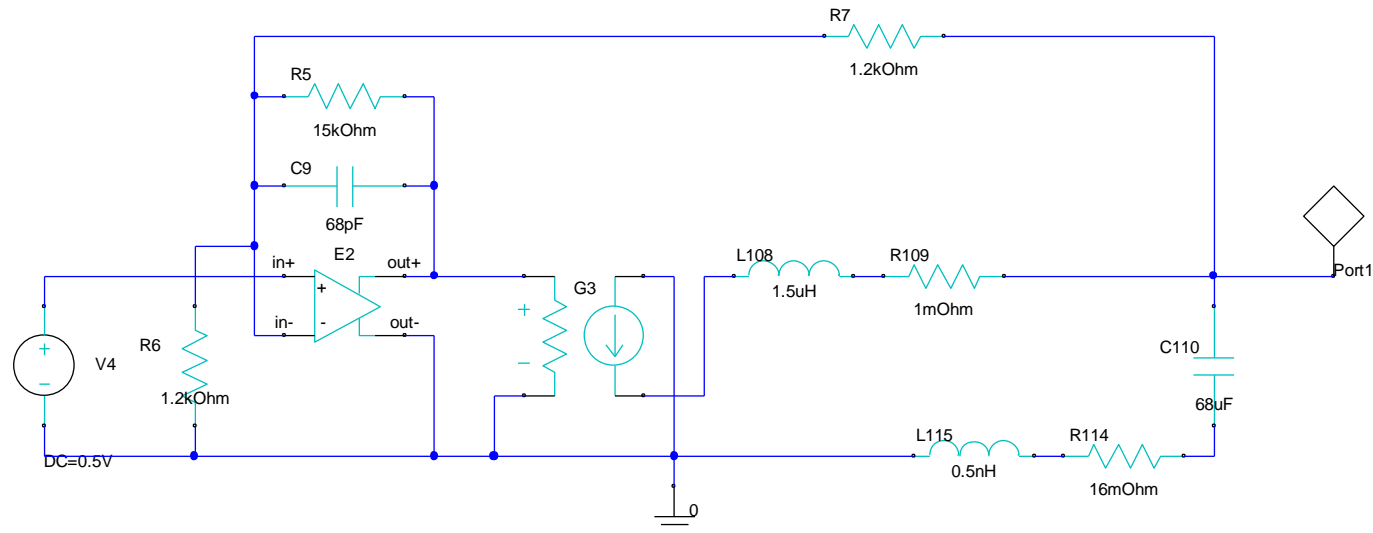


Impedance Analysis

VRM Definition

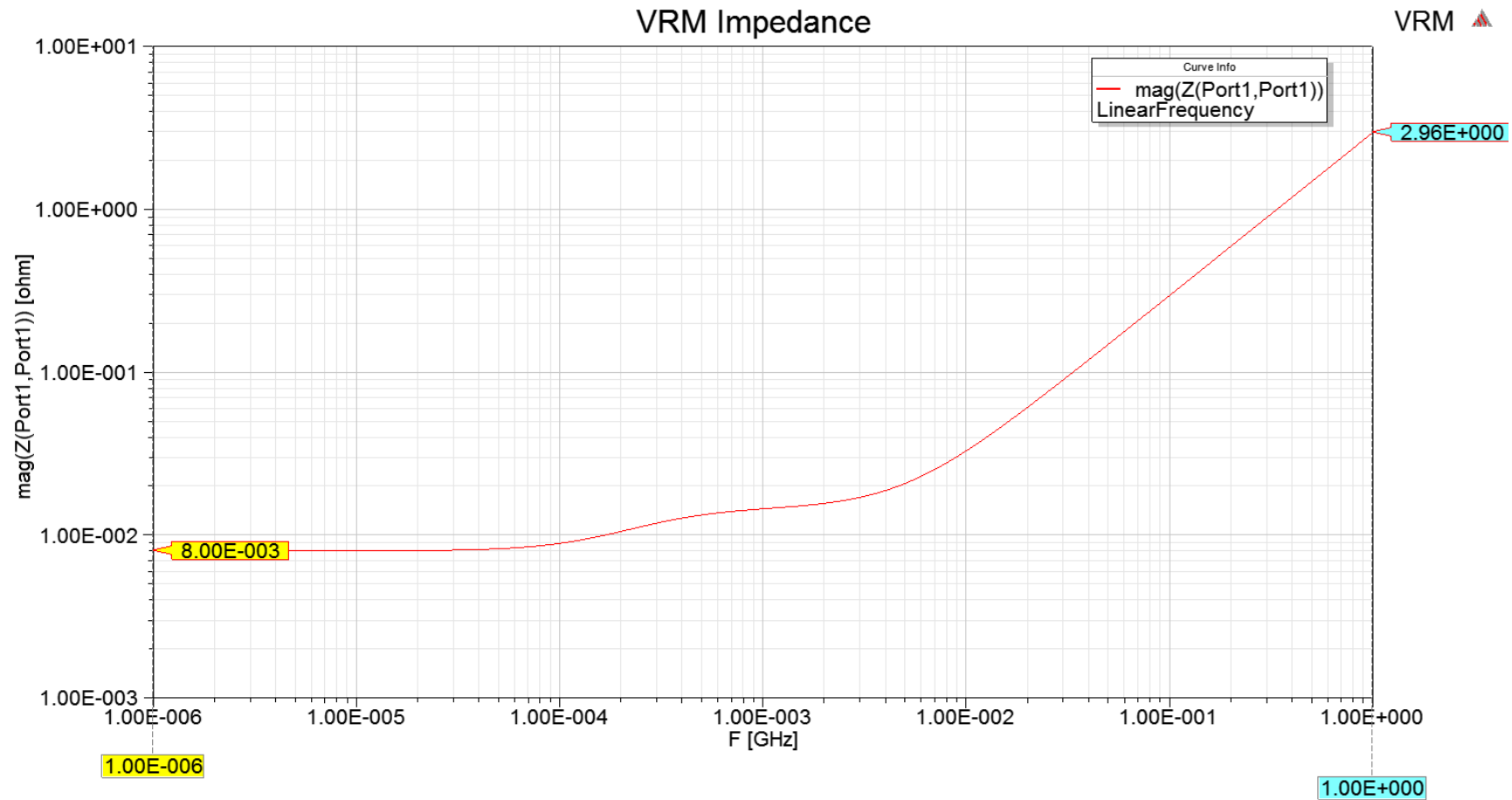


Example VRM Circuit: Target 1V Supply @ 6.25 A with 50 mV Ripple

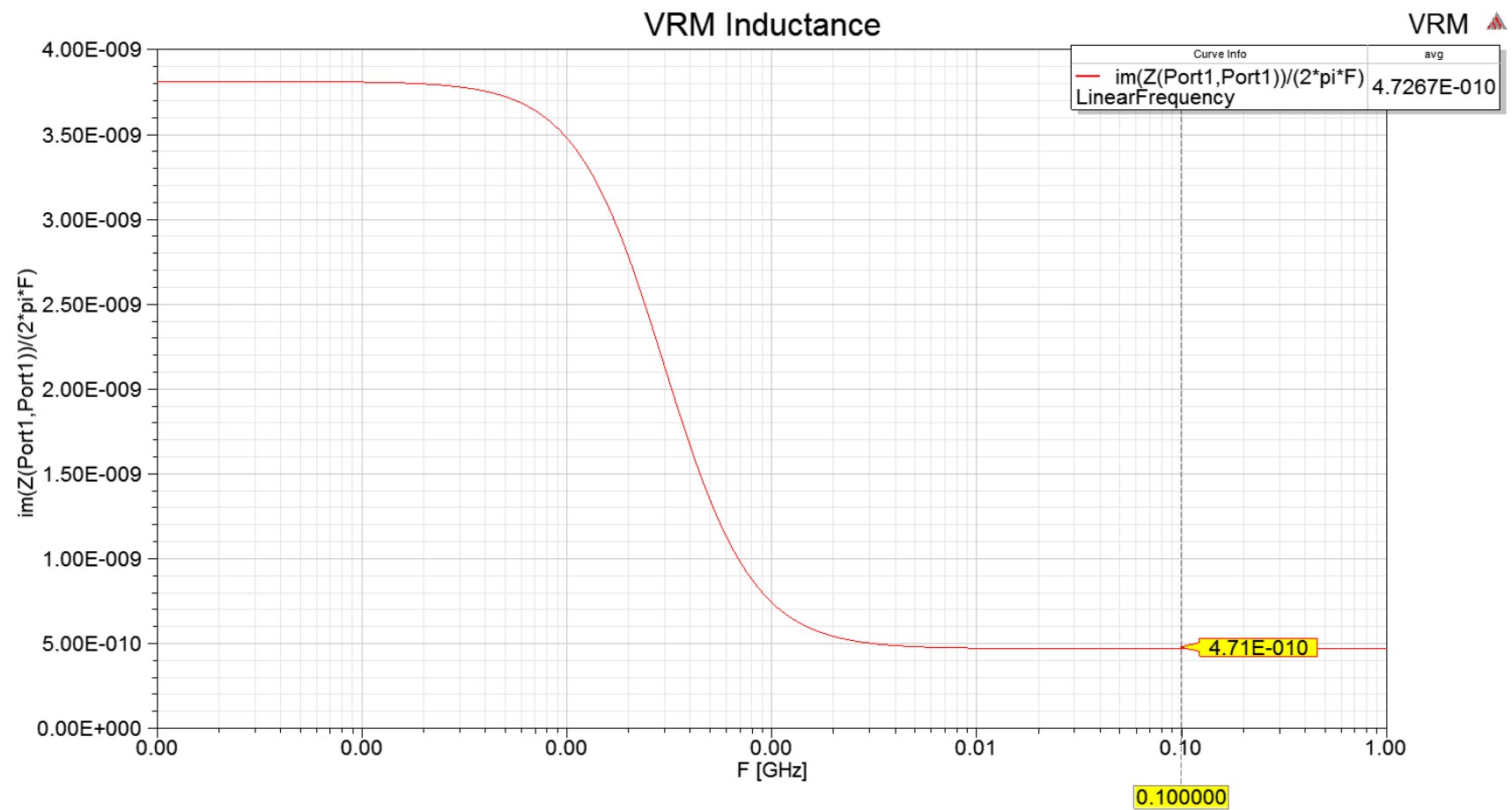


<http://www.edn.com/design/power-management/4440087/Design-a-VRM-with-perfectly-flat-output-impedance-in-5-seconds-or-less>

VRM Output Impedance



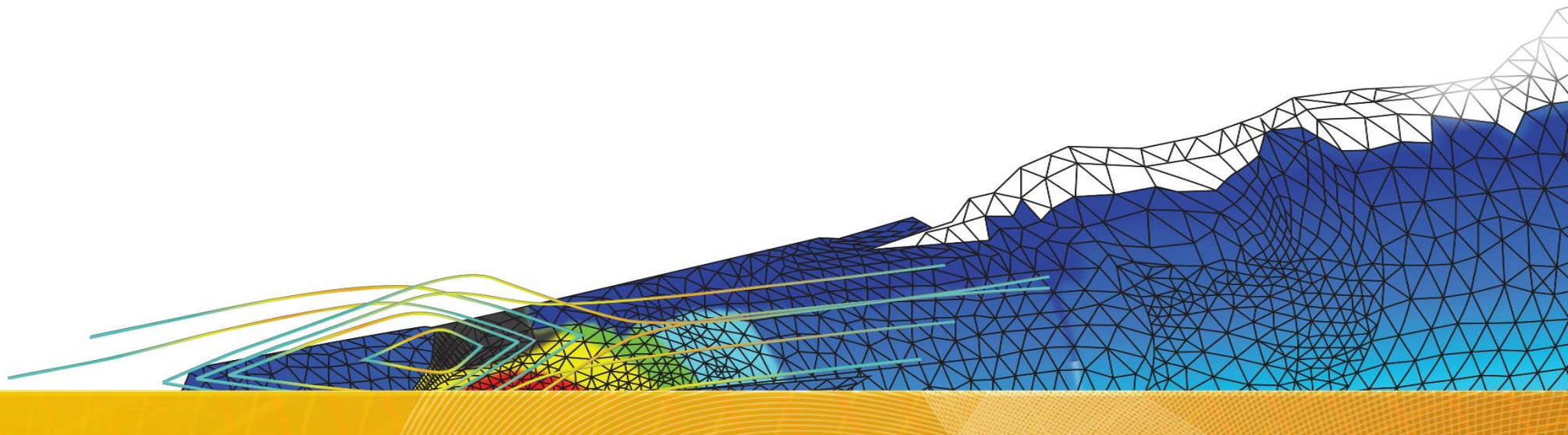
VRM Output Inductance





Impedance Analysis

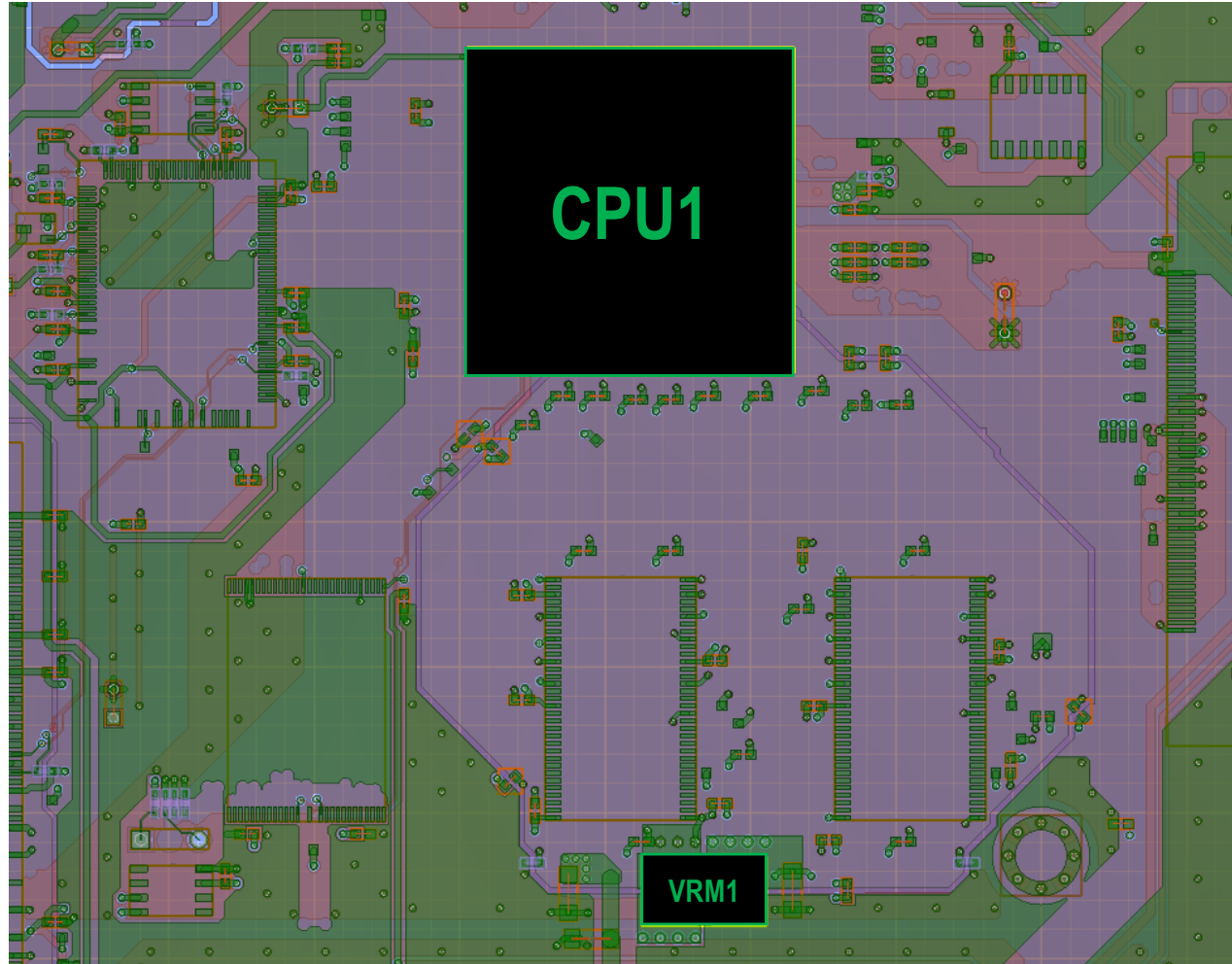
Z11 extraction and Resonant mode analysis bare board



PI Simulation Setup

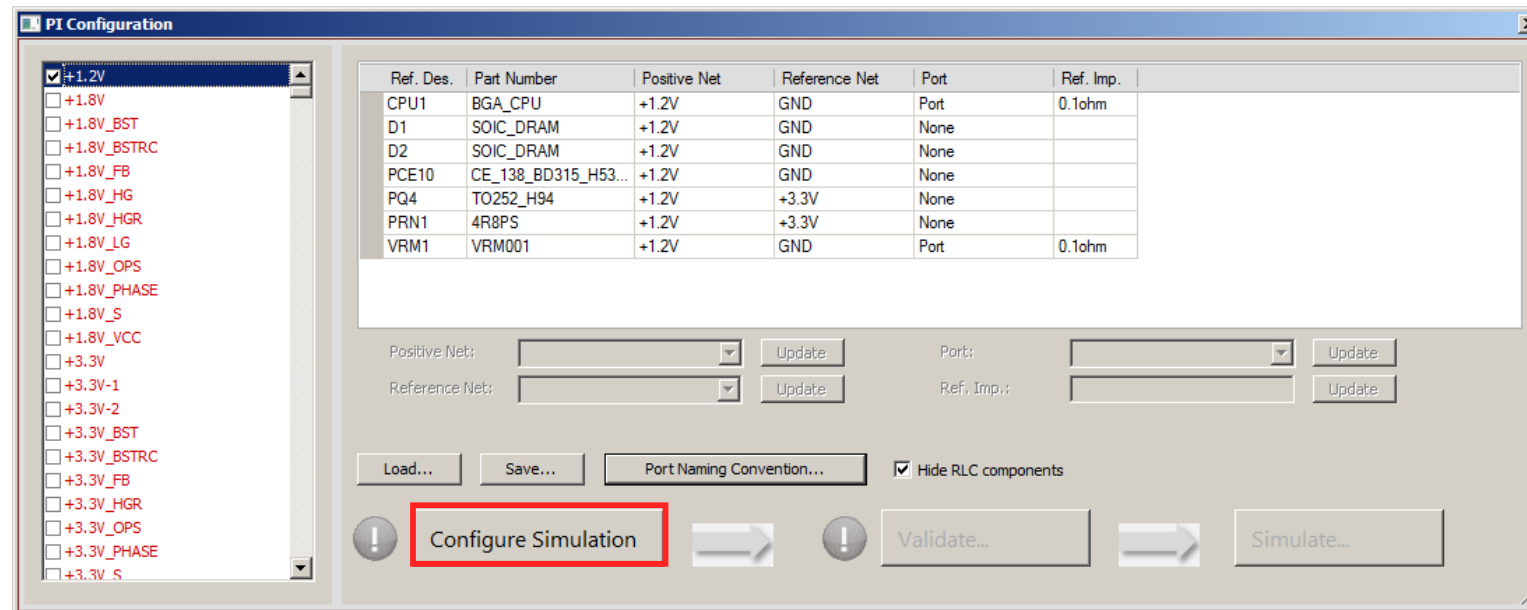
Single active device to simplify simulation results.

Top Layer



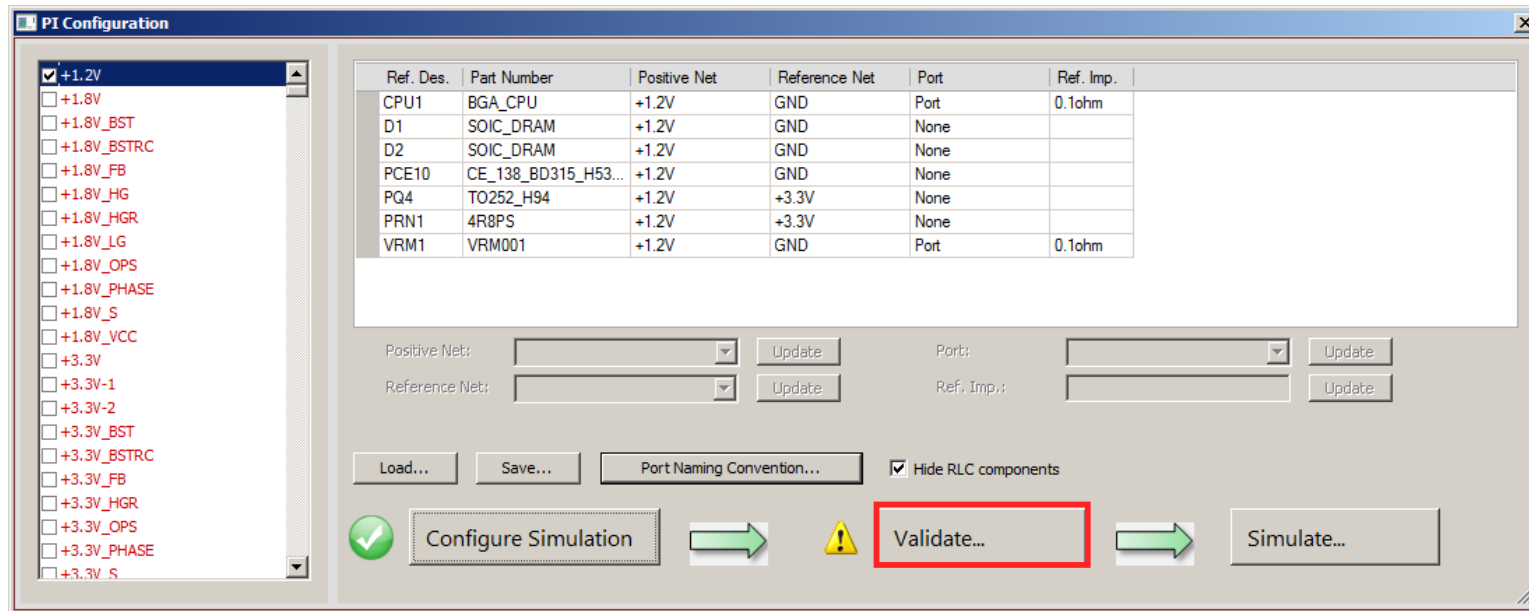
PI Ports Setup

- Click the checkbox next to the **+1.2V** net name to select it for simulation
 - The list of reference designators attached to the +1.2V net is shown on the right
- Change the Port column pull down menus for the **CPU1** and **VRM1** to Port
 - Reference impedance for these ports will be set to 0.1 ohm
- Click the **Configure Simulation** button to create pin groups and ports automatically



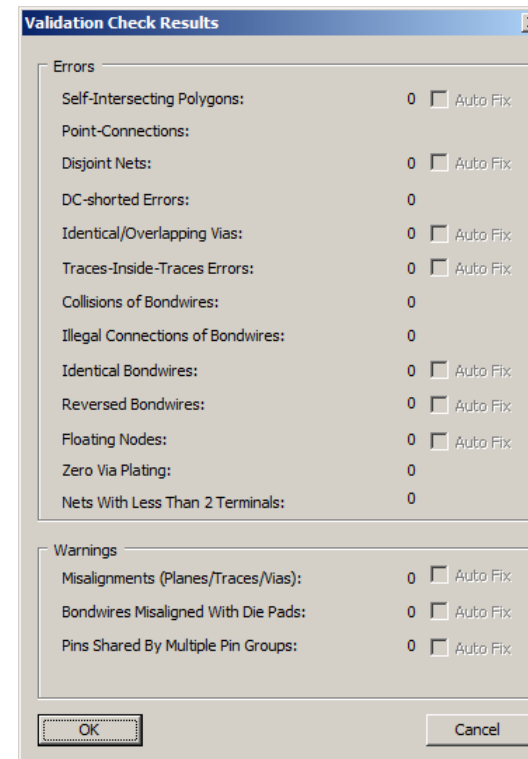
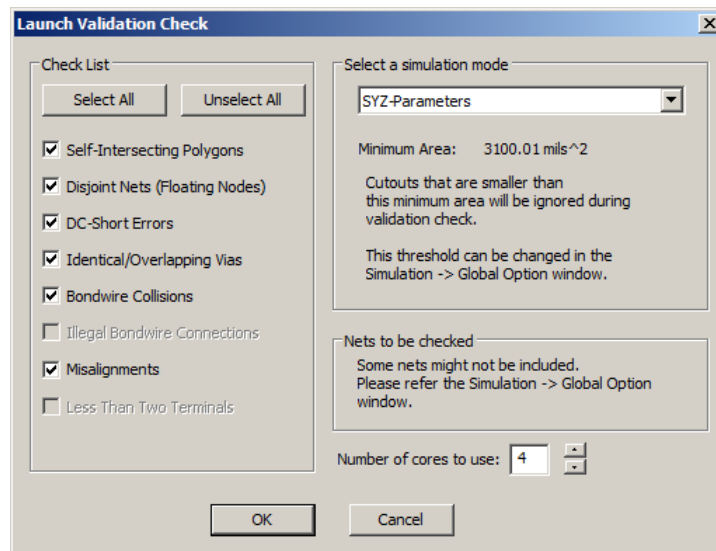
Validate Geometry

- Click the Validate button to open the Validation Check dialog



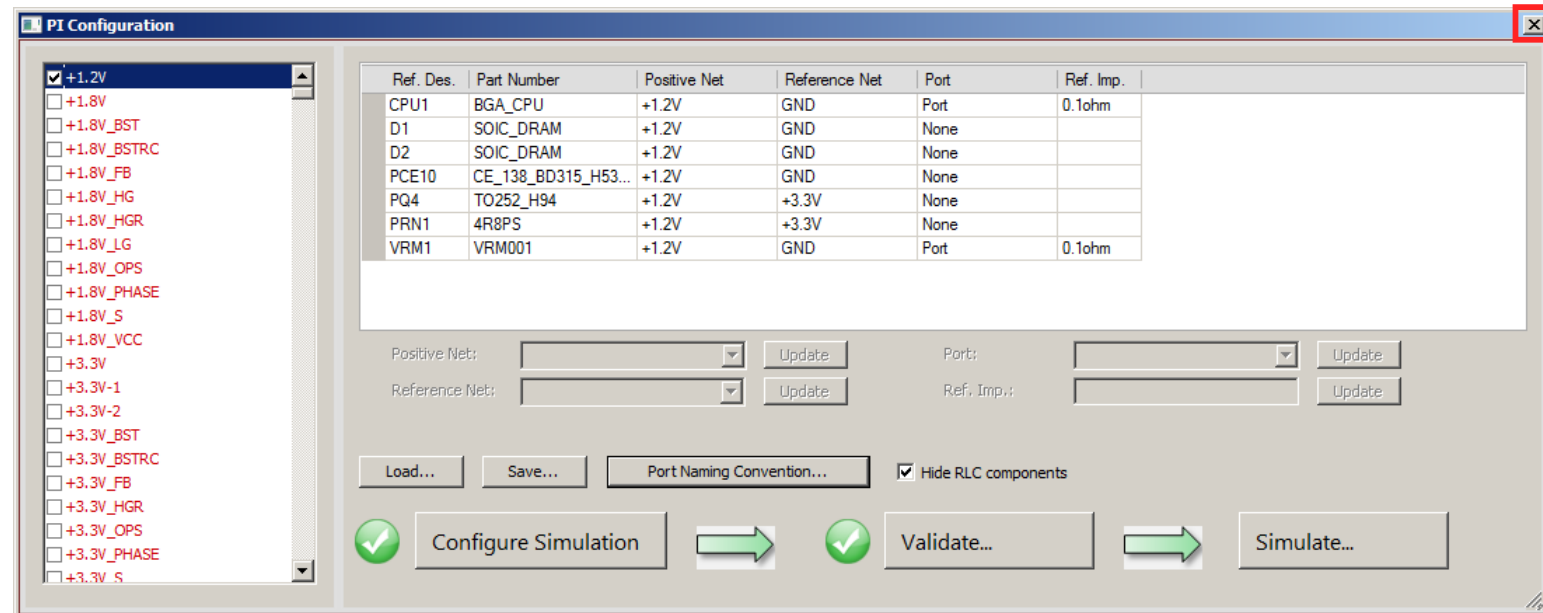
Validation Check

- Click the OK button to run the validation check to check for geometry errors
- Review the list of errors (there should be none) and click OK to close the results dialog



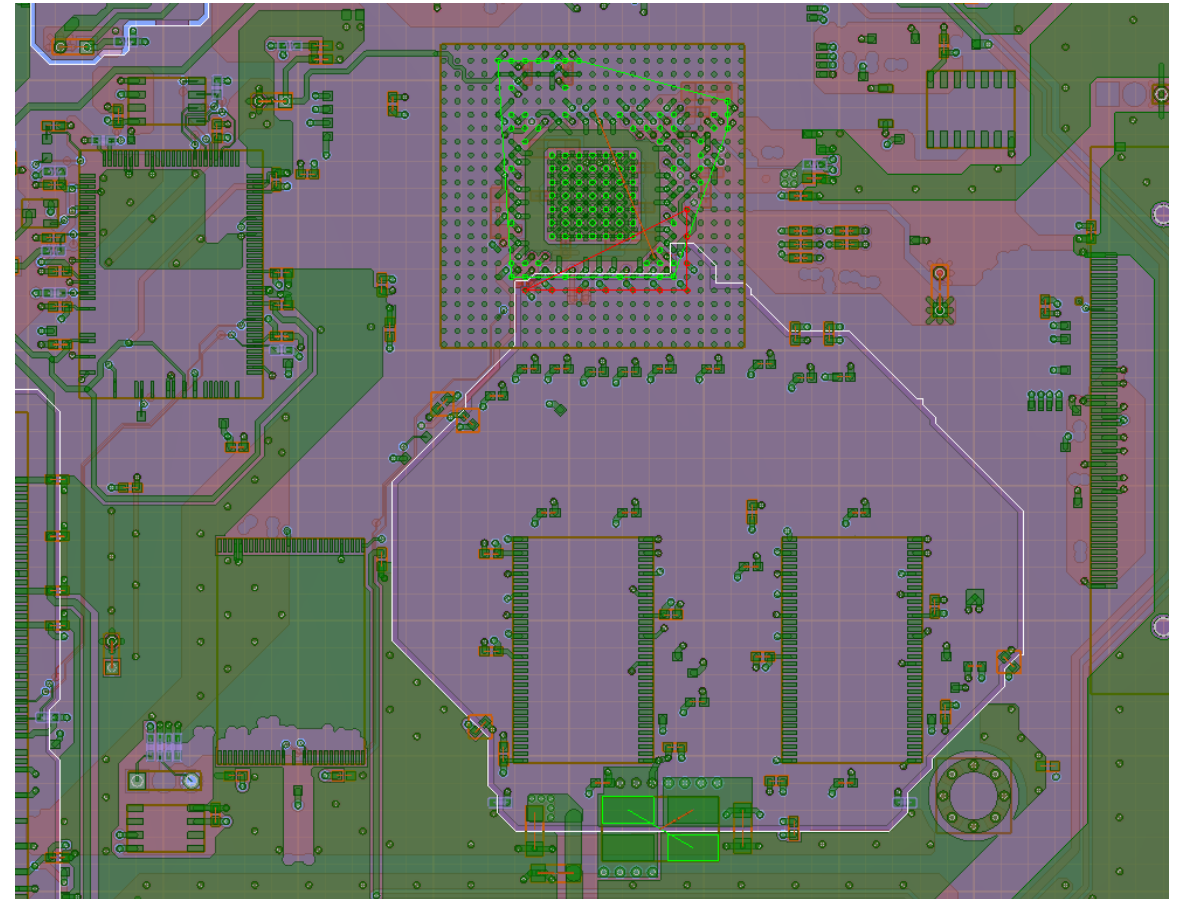
PI Ports Setup Complete

- At this point you could click the Simulate button to set up and run an SYZ sweep simulation, but in this example we will do some **additional setup** so just click the X button to close the PI Configuration dialog



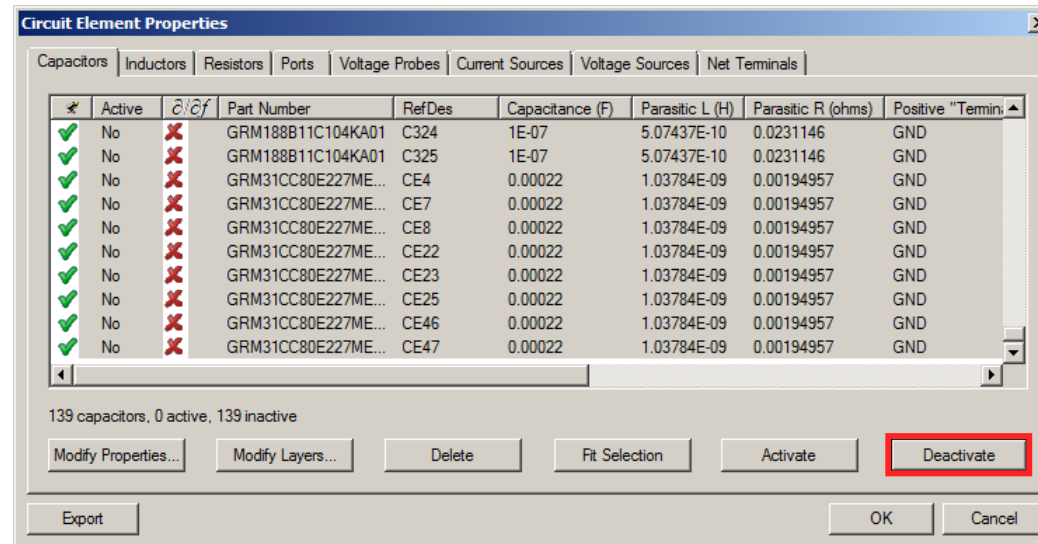
PI Ports

- Examine the ports and pin groups created by the PI configuration tool
- Pin groups are connected sets of pins colored green or red
- Ports connected between pin groups indicate measurement points for S-parameters



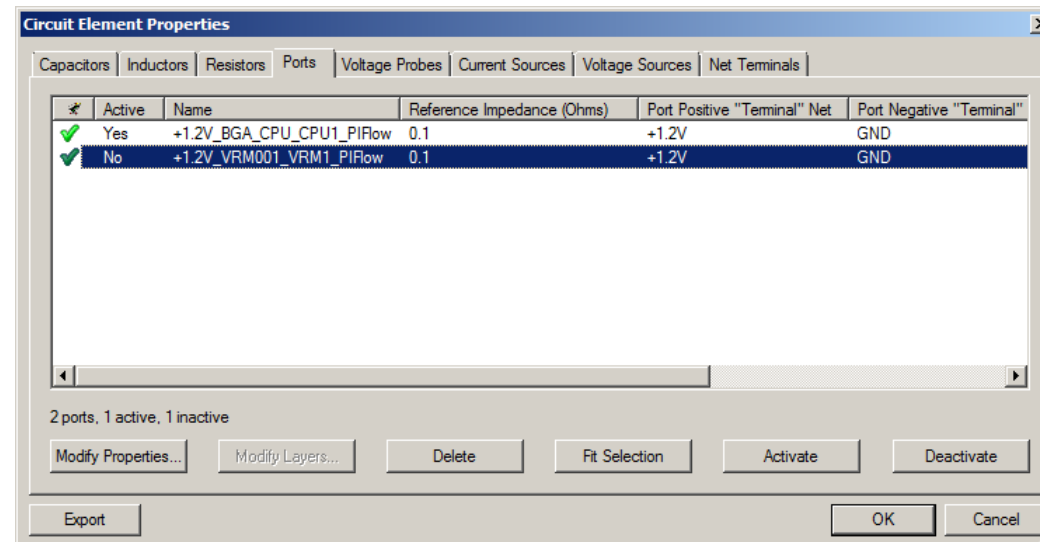
Deactivate All Capacitors

- On the Home ribbon click the Circuit Element Parameters button
- On the Capacitors tab select all the capacitors by clicking the first row in the list, scrolling to the bottom of the list, holding down Shift on the keyboard, and clicking the last row in the list
- Click the Deactivate button to deactivate all the capacitors



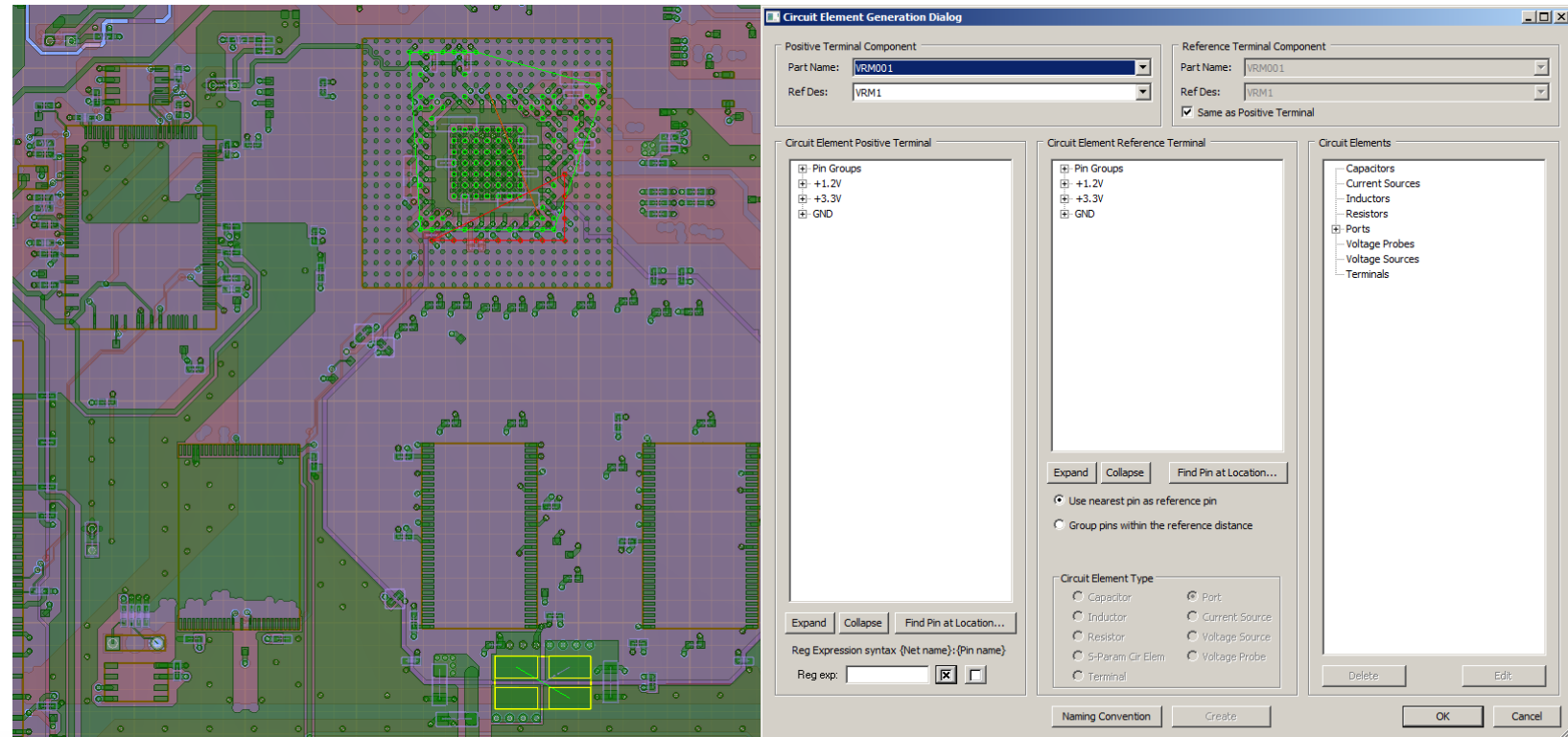
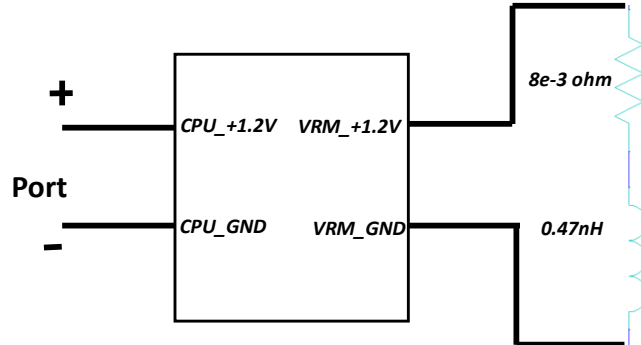
Deactivate VRM Port

- Activate the Ports tab
- Click the VRM port to select it
- Click the Deactivate button to deactivate the selected port
- Click OK to save the changes and close the dialog



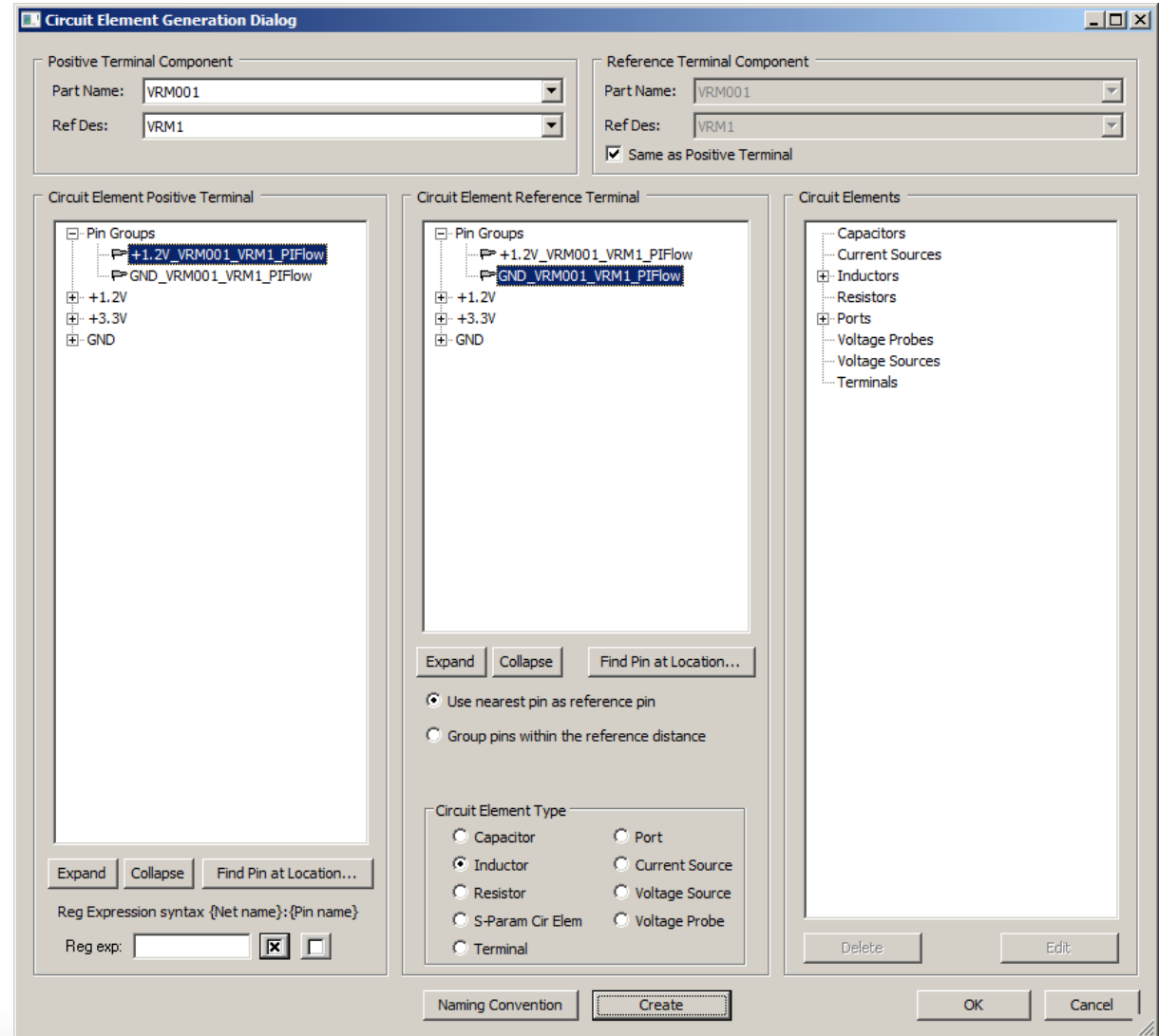
Create Simple VRM Output Model

- We can model the VRM to be a simple series RL circuit with parameters $R = 8\text{mohm}$ and $L = 0.47\text{nH}$
- Click the outline of the VRM device footprint to select it
- Go to **Tools** → **Generate Circuit Element on Components** button to raise the Circuit Element Generation Dialog
- The VRM1 component will be automatically selected



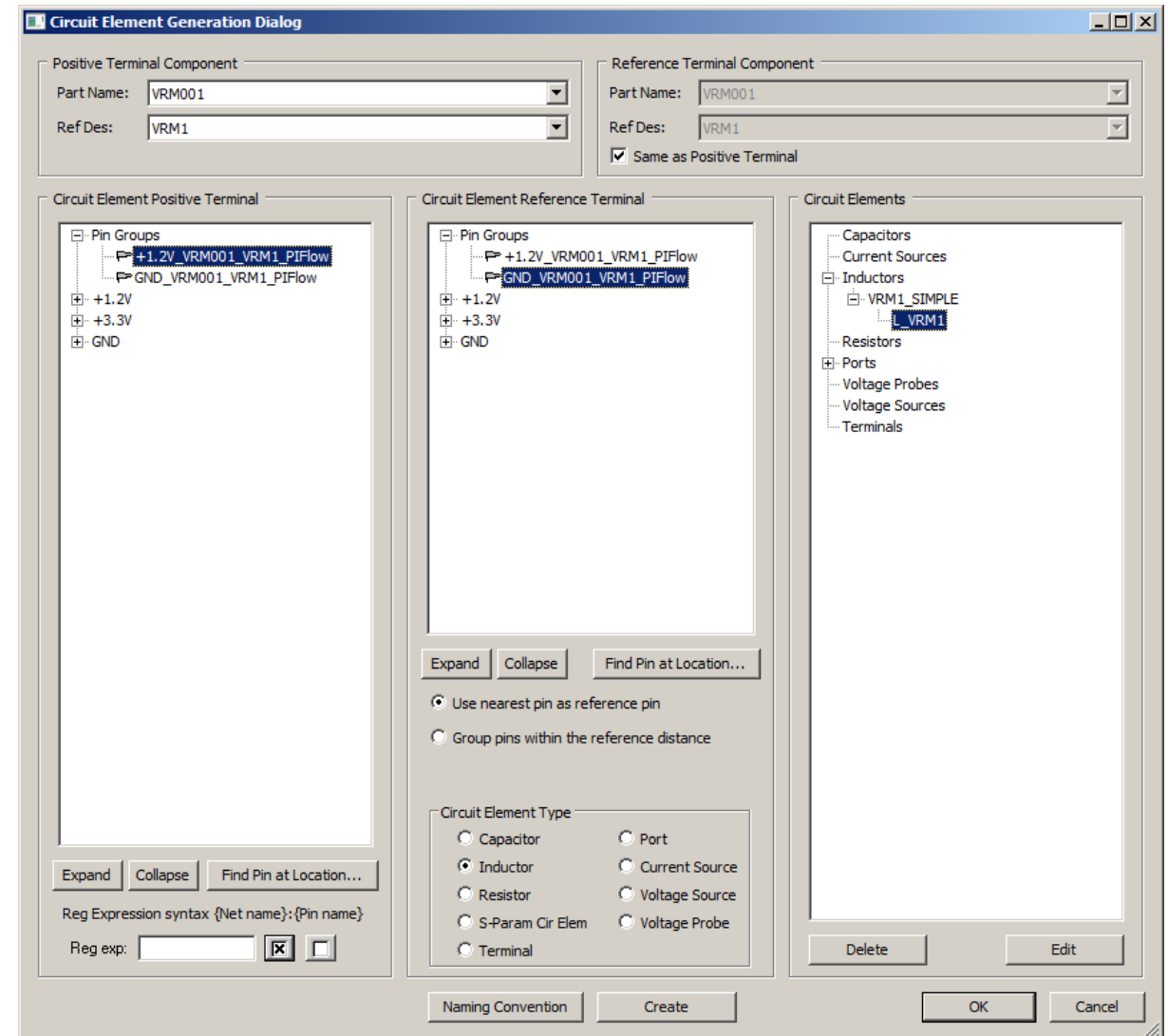
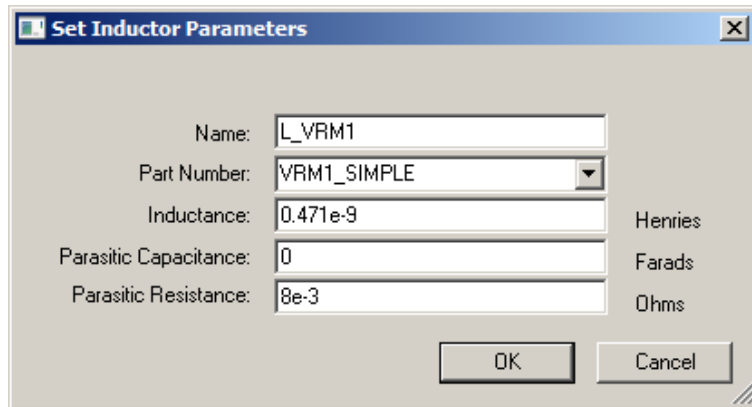
Create Simple VRM Output Model

- In the Circuit Element Positive Terminal list expand Pin Groups and select the **+1.2V_VRM001_VRM1_PIFlow** group
- In the Circuit Element Reference Terminal list expand Pin Groups and select the **GND_VRM001_VRM1_PIFlow** group
- In the Circuit Element Type list select **Inductor**
- Click **Create**



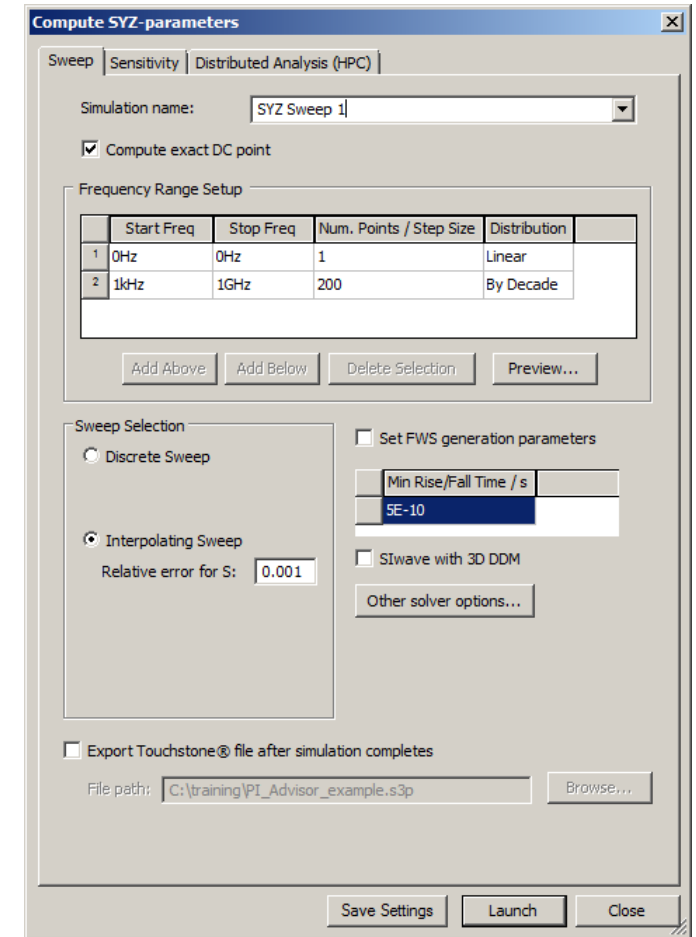
Create Simple VRM Output Model

- Enter **L_VRM1** in the Name text box
- Enter **VRM1_SIMPLE** in the Part Number text box
- Enter **0.471e-9** in the Inductance text box
- Enter 0 in the Parasitic Capacitance text box
- Enter **8e-3** in the Parasitic Resistance text box
- Click OK to create the Inductor



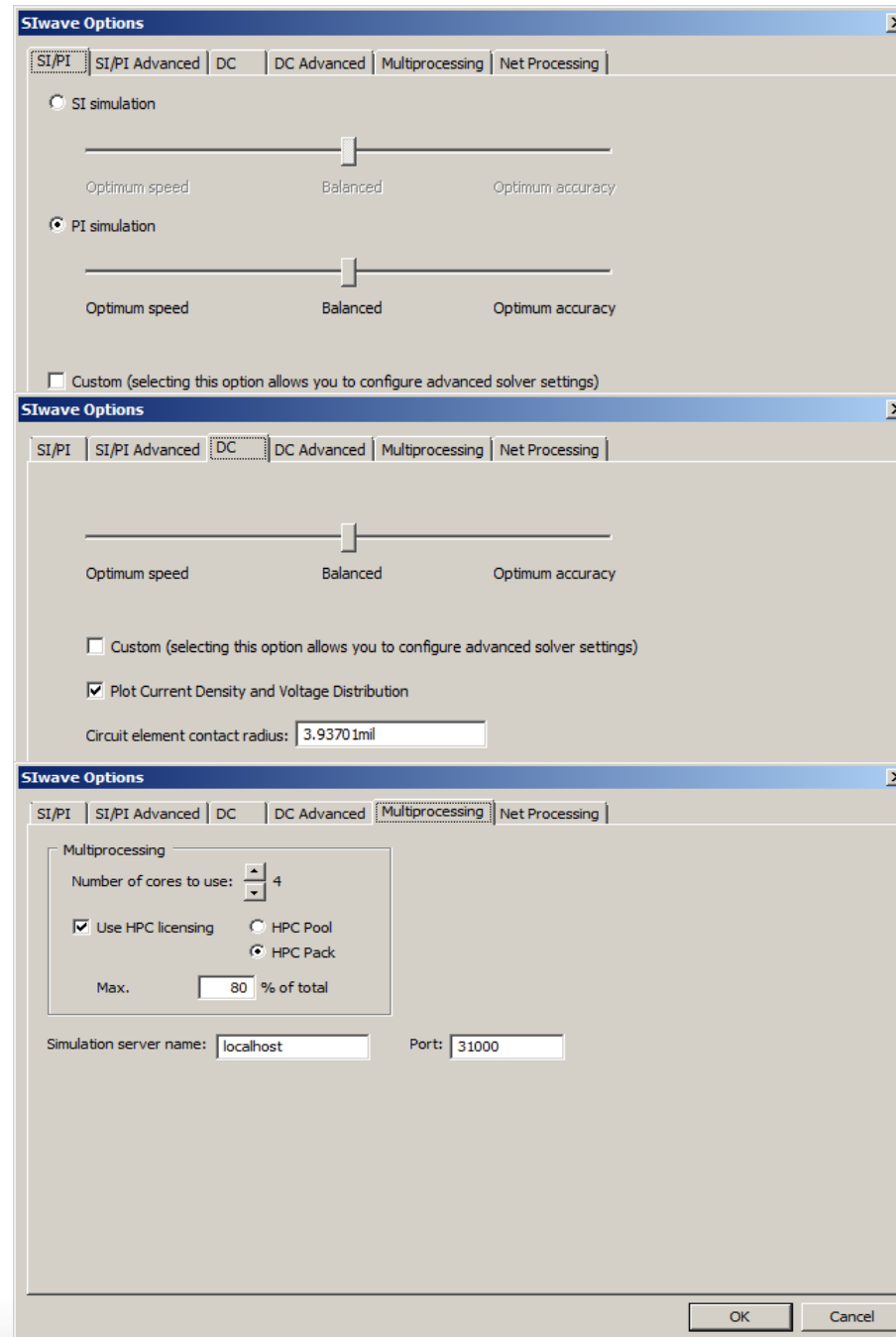
Set Up S-parameter Sweep

- Go to **Simulation** → **Compute SYZ Parameters** button
- Enter **SYZ Sweep 1** in the Simulation Name text box
- Turn on the **Compute Exact DC Point** check box
- Set up the following frequency ranges using the Add Above/Add Below/Delete Selection buttons:
 - 0 Hz to 0 Hz, 1 point, Linear
 - 1 kHz to 1 GHz, 200 points, By Decade
- Select the Interpolating sweep option button and enter **0.001** in the Relative Error for S text box
- Turn off the Export Touchstone File After Simulation Completes check box
- Click **Other Solver Options** button



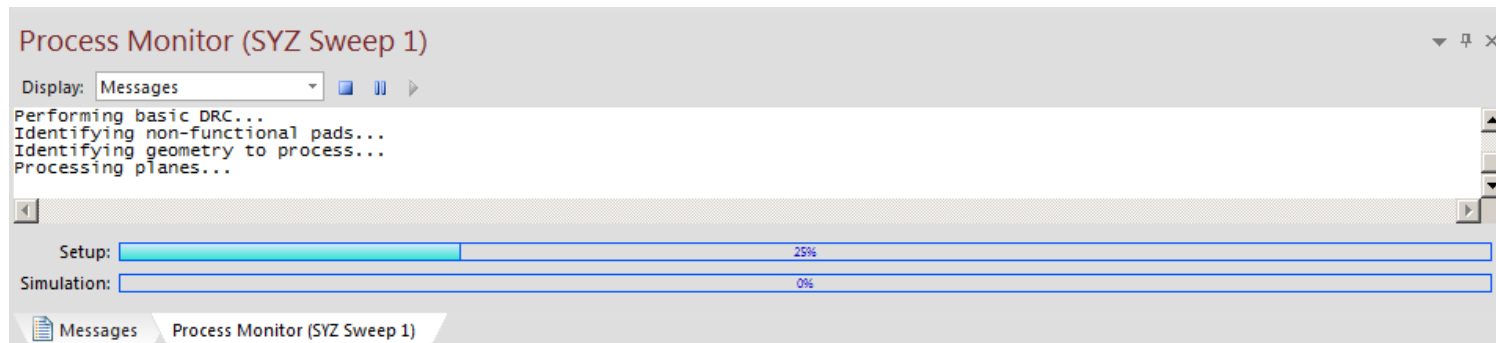
PI Options Setup

- On the **SI/PI tab** select the PI Simulation option button and set the slider to Balanced
- On the **DC tab** turn off the Custom check box and set the slider to Balanced
- On the **Multiprocessing tab** set the Number of Cores to the number of physical processor cores in your machine, turn on the **Use HPC Licensing** check box, and select the option button for the type of HPC licenses you have
- Click **OK** to save any changes and close the dialog



Launch S-parameter Sweep

- Click **Launch** to start the SYZ parameter analysis



Compute SYZ-parameters

Sweep Sensitivity Distributed Analysis (HPC)

Simulation name: SYZ Sweep 1

☒ Compute exact DC point

Frequency Range Setup

	Start Freq	Stop Freq	Num. Points / Step Size	Distribution
1	0Hz	0Hz	1	Linear
2	1kHz	1GHz	200	By Decade

Add Above Add Below Delete Selection Preview...

Sweep Selection

☐ Discrete Sweep

☒ Interpolating Sweep

Relative error for S: 0.001

☐ Set FWS generation parameters

Min Rise/Fall Time / s: 5E-10

☐ Siwave with 3D DDM

Other solver options...

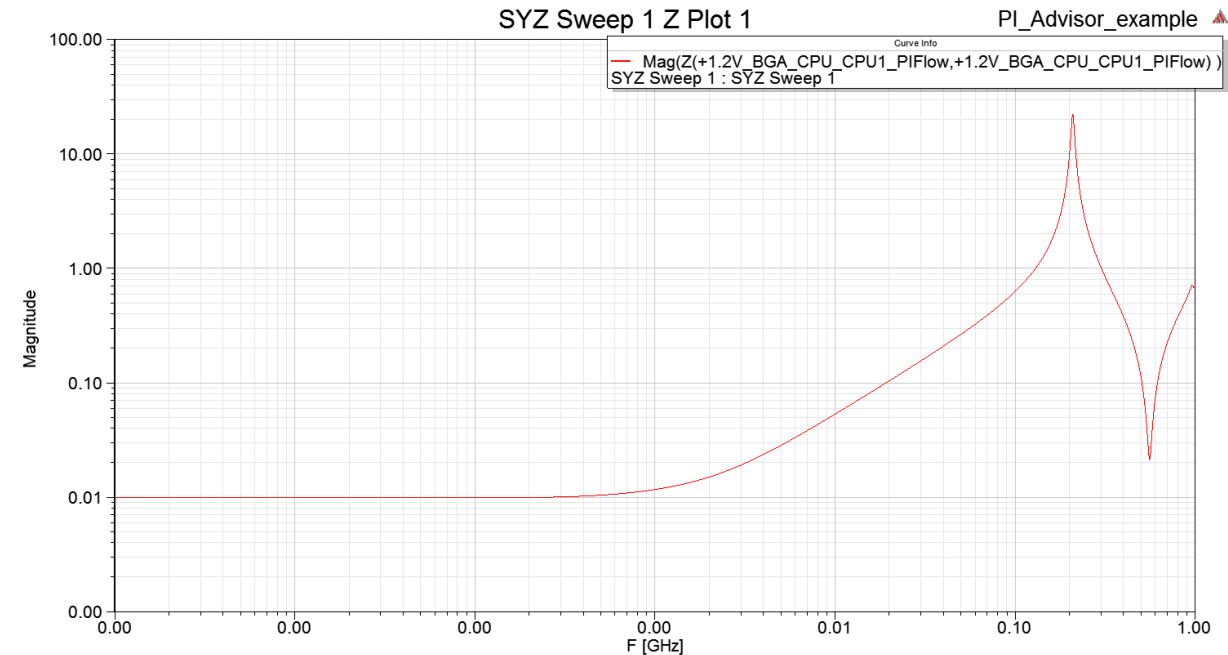
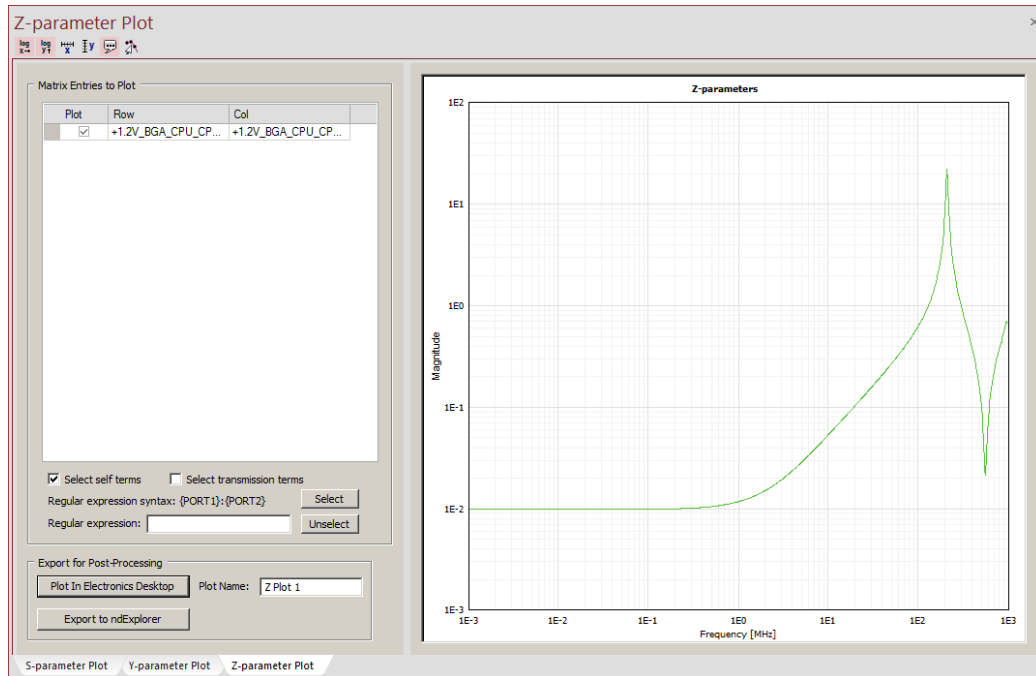
☐ Export Touchstone® file after simulation completes

File path: C:\training\PI_Advisor_example.s3p Browse...

Save Settings Launch Close

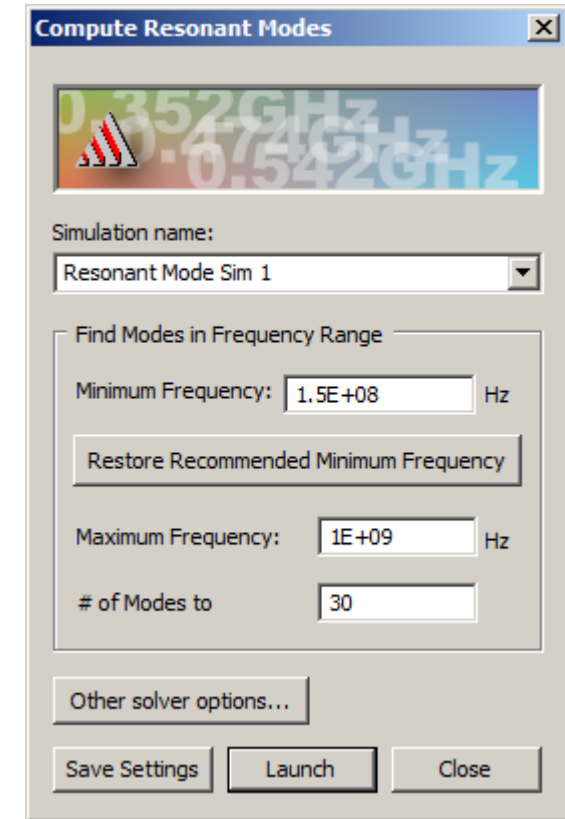
Plot PDN Impedance (Board + VRM)

- On the Results ribbon click **SYZ > SYZ Sweep 1 > Plot Magnitude** to raise the SYZ Parameter Plot dialog
- Activate the Z-Parameter Plot tab to display the impedance seen by the CPU1 device with all capacitors deactivated and the simple VRM model
- Click the Plot In Electronics Desktop button to launch ANSYS Electronics Desktop and plot the impedance in that interface as well



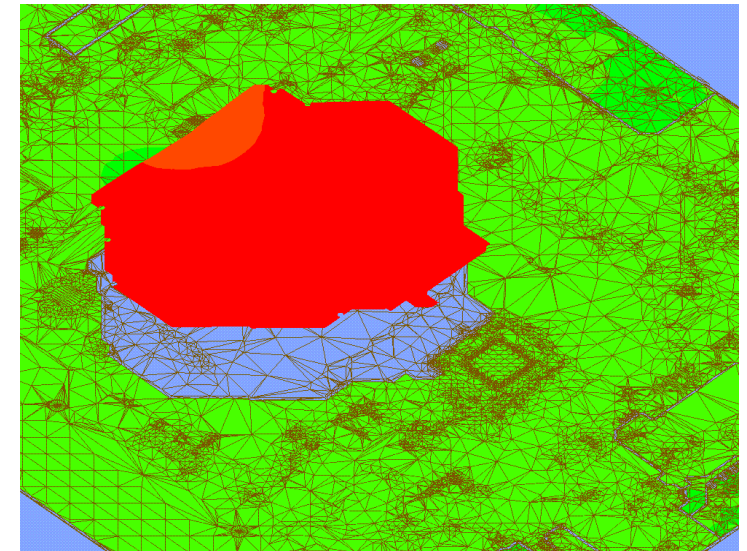
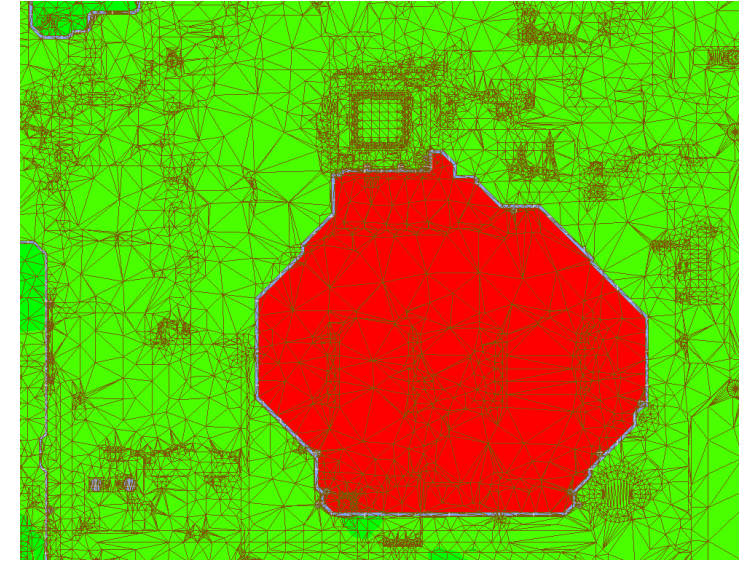
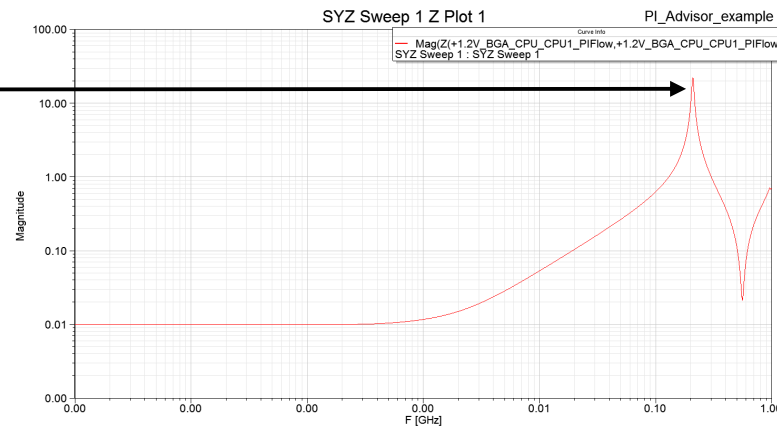
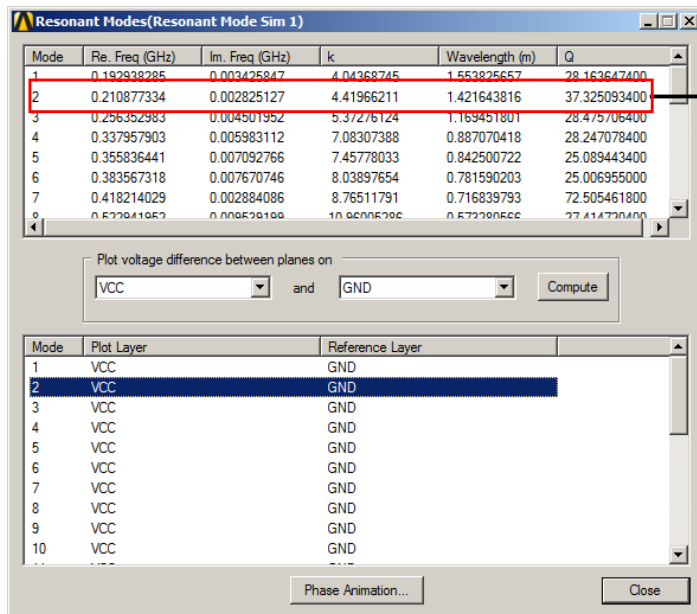
Set Up and Run Resonant Mode Simulation

- Go to **Simulation** → **Compute Resonant Modes** button
- Enter **Resonant Mode Sim 1** in the Simulation Name text box
- Enter **1.5e8 Hz** in the Minimum Frequency text box
- Enter **1e9 Hz** in the Maximum Frequency text box
- Enter **30** in the # of Modes to Compute text box
- Click **Launch** to start the Resonant Mode simulation



Examine Resonant Mode Simulation Results

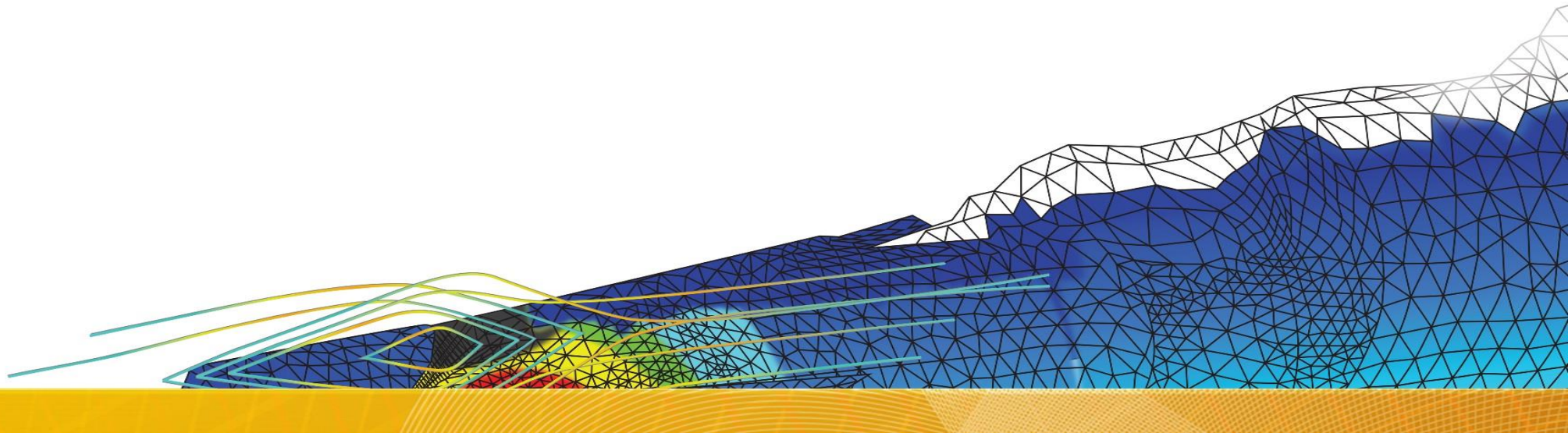
- **Results → Resonant Mode > Resonant Mode Sim 1 > View Results** to open the results dialog
 - Note that the second found mode at 211 MHz appears to correlate with the first large spike in the impedance plot from the earlier SYZ simulation
 - To view the shape of the modes select VCC and GND in the Plot Voltage Difference pull down menus and click the Compute button
- After viewing the plots click Close





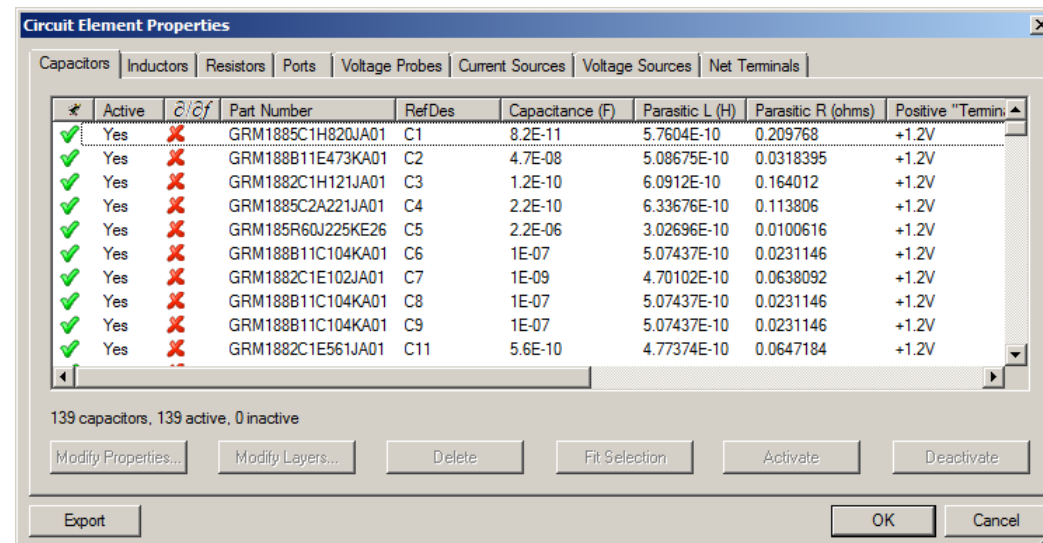
Impedance Analysis

Z11 extraction and Resonant mode analysis with active capacitors



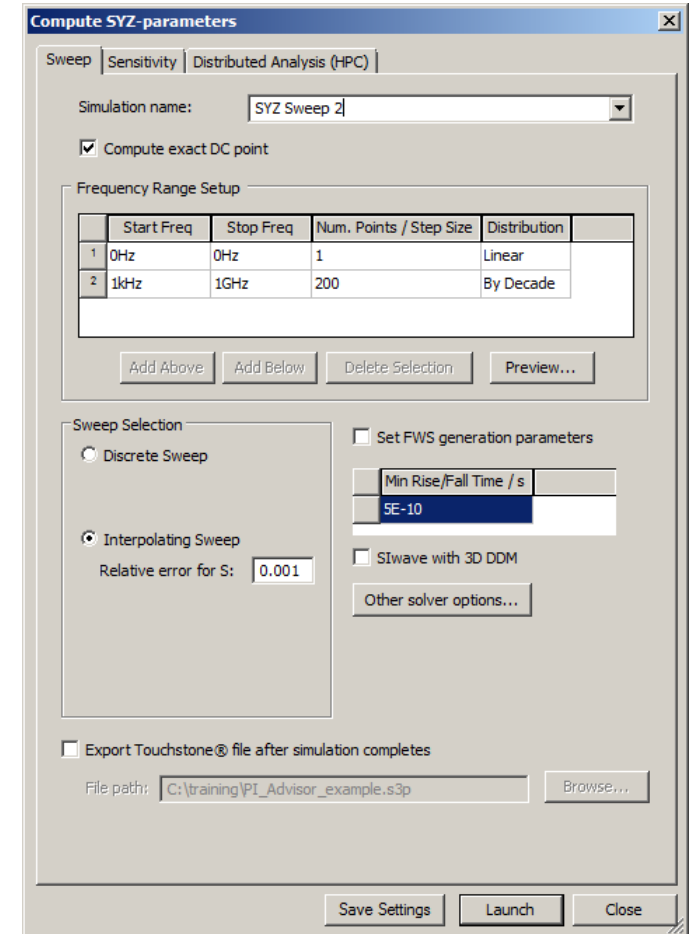
Activate All Capacitors

- On the Home ribbon click the **Circuit Element Parameters** button
 - On the Capacitors tab select all the capacitors by clicking the first row in the list, scrolling to the bottom of the list, holding down Shift on the keyboard, and clicking the last row in the list
 - Click the **Activate** button to reactivate all the capacitors



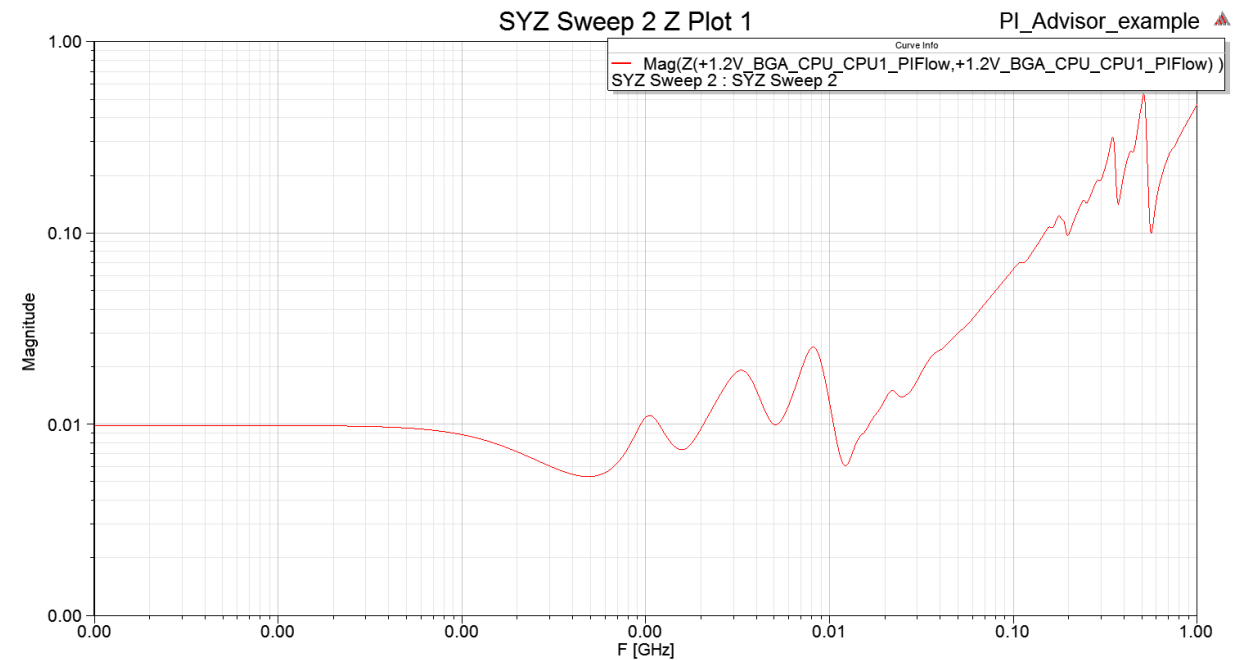
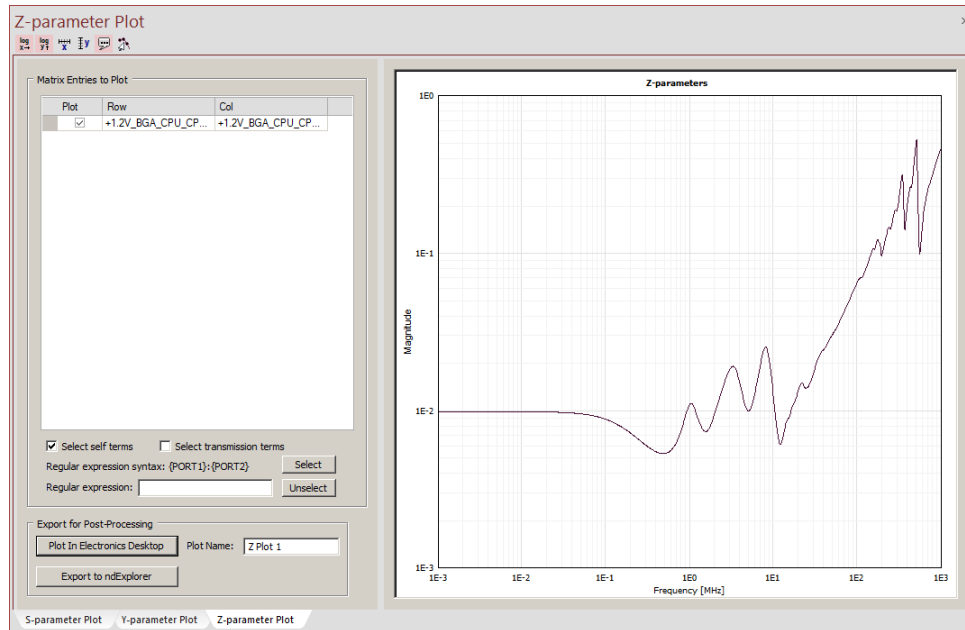
Set Up S-parameter Simulation

- On the Simulation ribbon click the **Compute SYZ Parameters** button
 - Enter **SYZ Sweep 2** in the Simulation Name text box
 - Turn on the **Compute Exact DC Point** check box
 - Set up the following frequency ranges using the Add Above/Add Below/Delete Selection buttons:
 - 0 Hz to 0 Hz, 1 point, Linear
 - 1 kHz to 1 GHz, 200 points, By Decade
 - Select the Interpolating sweep option button and enter 0.001 in the Relative Error for S text box
 - Turn off the Export Touchstone File After Simulation Completes check box
- Click **Launch** to start the S-parameter simulation



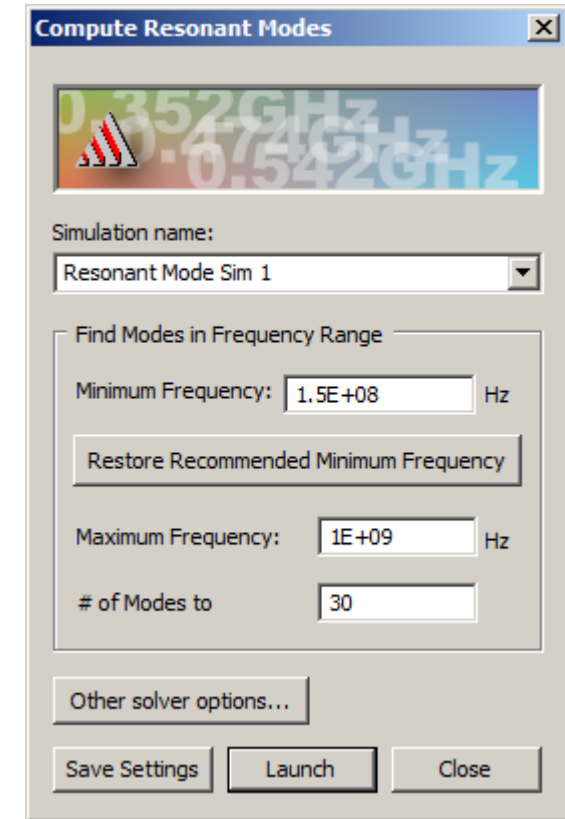
Plot PDN Impedance (Board + Capacitors + VRM)

- On the Results ribbon click **SYZ > SYZ Sweep 2 > Plot Magnitude** to raise the SYZ Parameter Plot dialog
- Activate the Z-Parameter Plot tab to display the impedance seen by the CPU1 device with all capacitors activated and the simple VRM model
- Click the Plot In Electronics Desktop button to launch ANSYS Electronics Desktop and plot the impedance in that interface as well



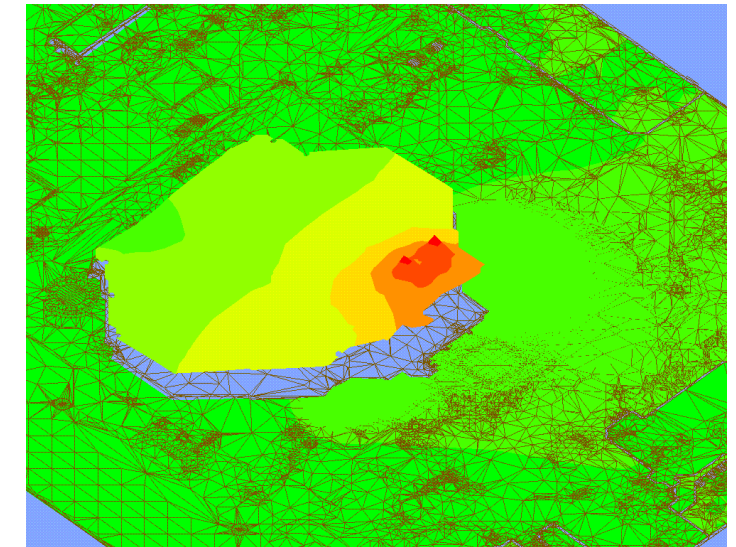
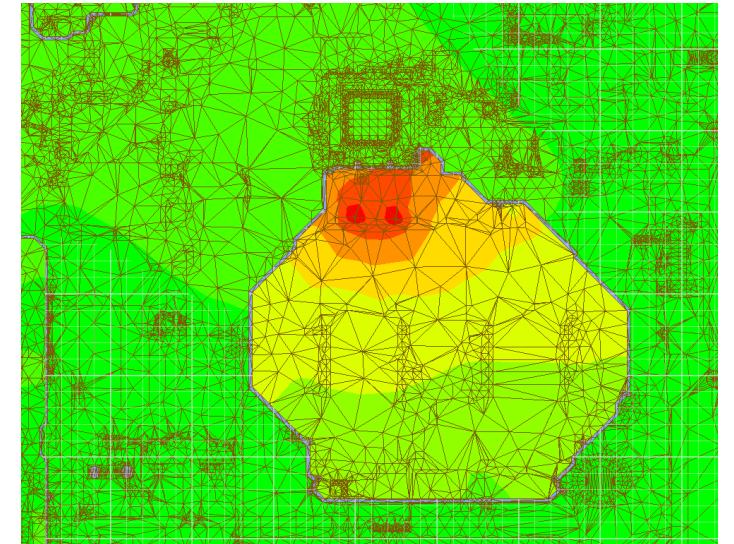
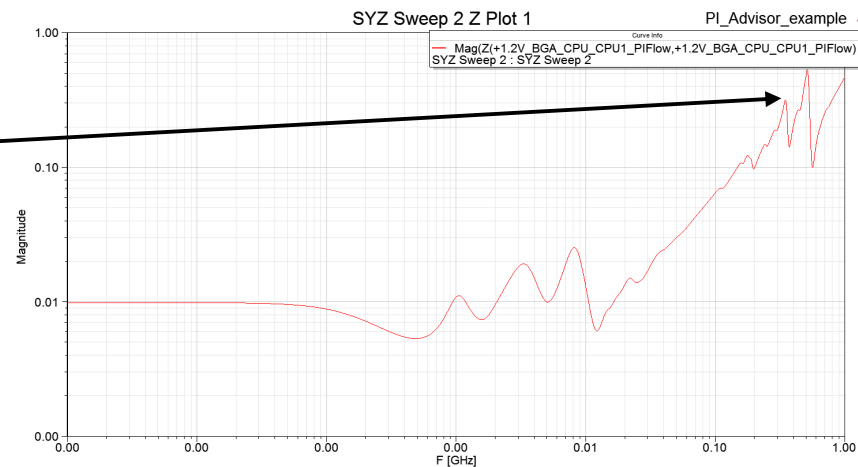
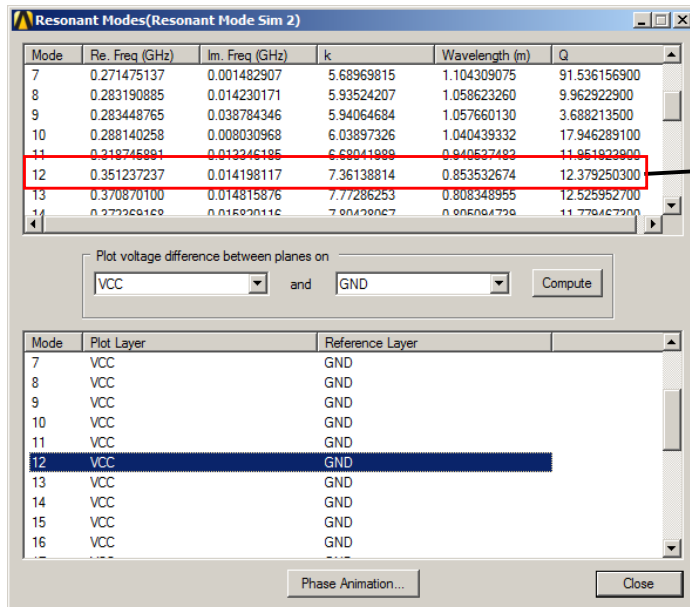
Set Up and Run Resonant Mode Simulation

- Go to **Simulation** → **Compute Resonant Modes** button
- Enter **Resonant Mode Sim 2** in the Simulation Name text box
- Enter **1.5e8 Hz** in the Minimum Frequency text box
- Enter **1e9 Hz** in the Maximum Frequency text box
- Enter **30** in the # of Modes to Compute text box
- Click **Launch** to start the Resonant Mode simulation



Examine Resonant Mode Simulation Results

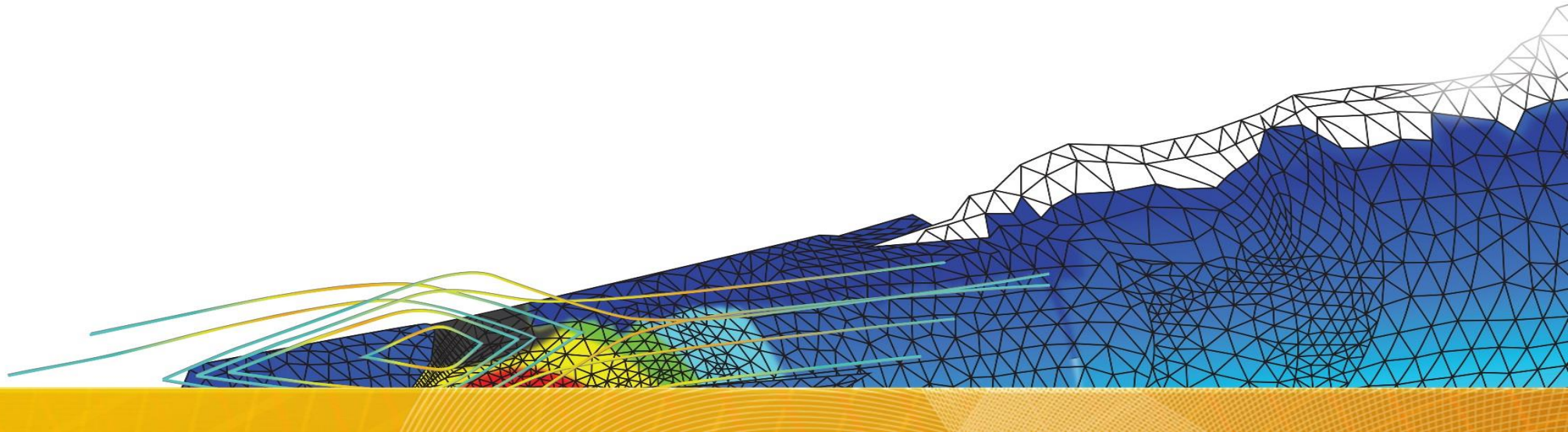
- **Results → Resonant Mode > Resonant Mode Sim 1 > View Results** to open the results dialog
 - Note that the 12th found mode at 351 MHz appears to correlate with a spike in the impedance plot from the earlier SYZ simulation
 - To view the shape of the modes select VCC and GND in the Plot Voltage Difference pull down menus and click the Compute button
- After viewing the plots click Close



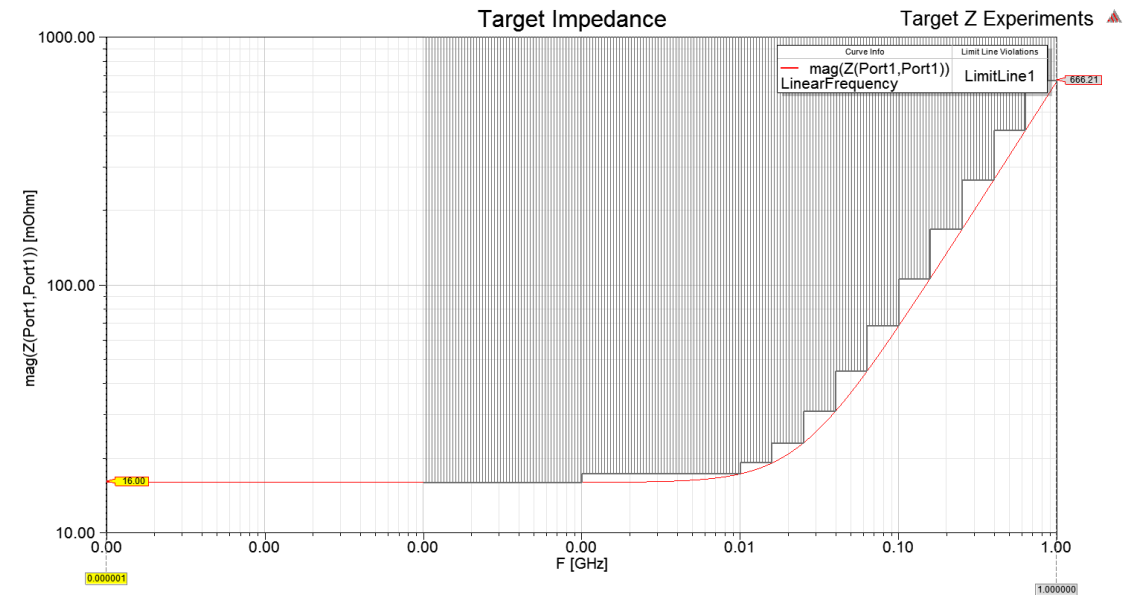
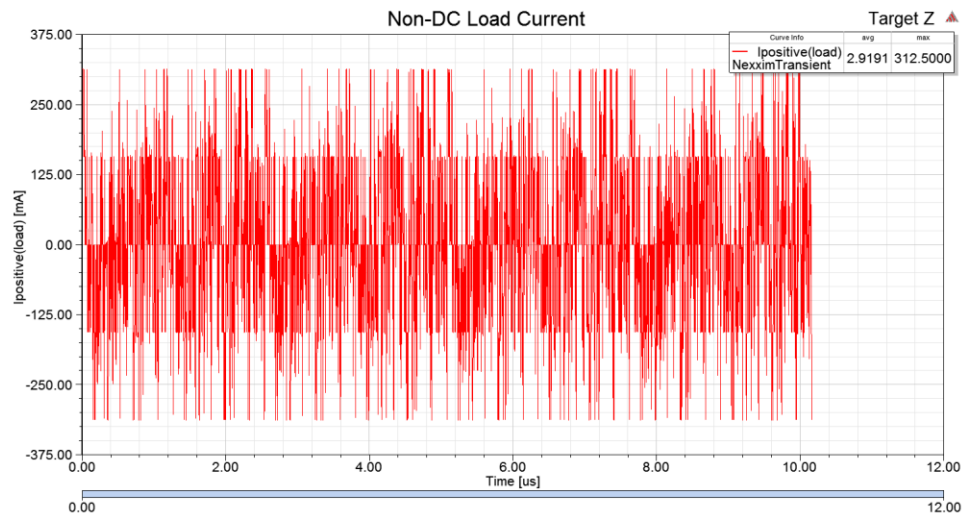


Impedance Target Definition

(OPTIONAL)



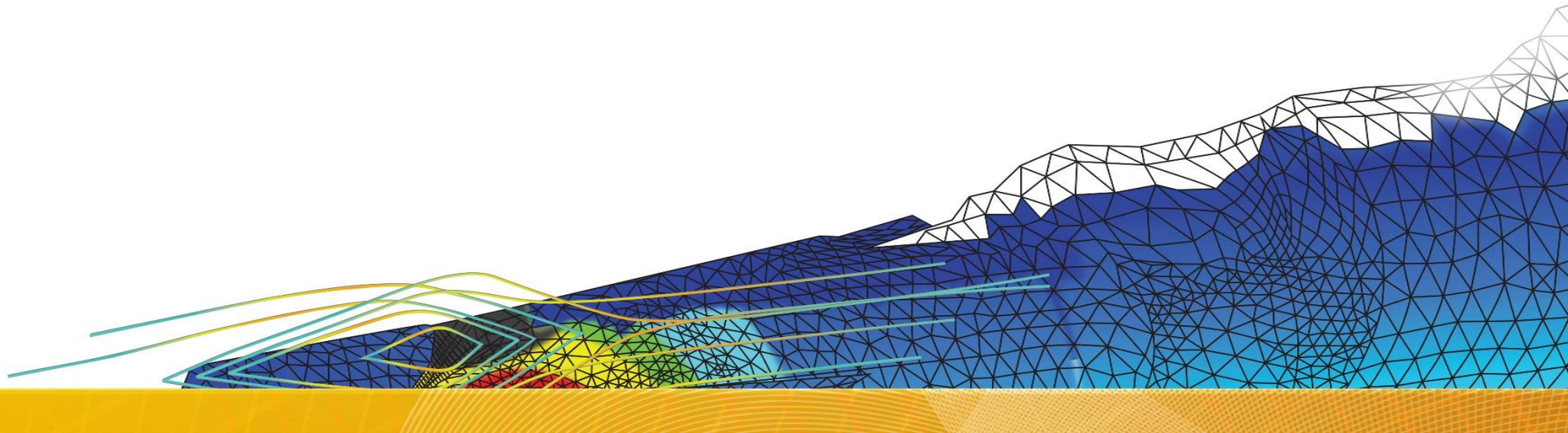
- Please refer to Workshop [Slwave_LnL_WSP03_Optional.pptx](#) located in the same directory as this workshop to follow a simple exercise for defining target impedance





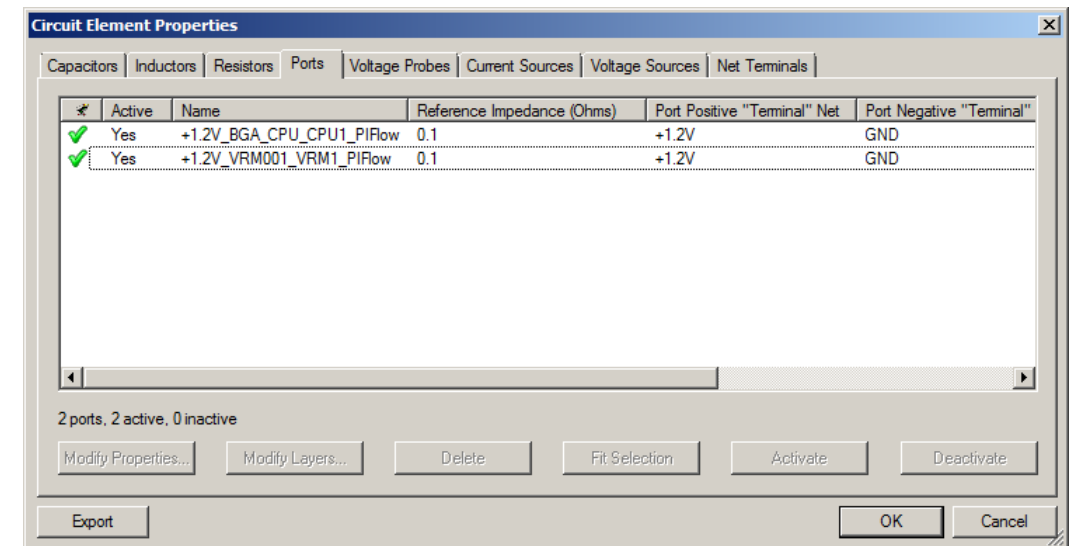
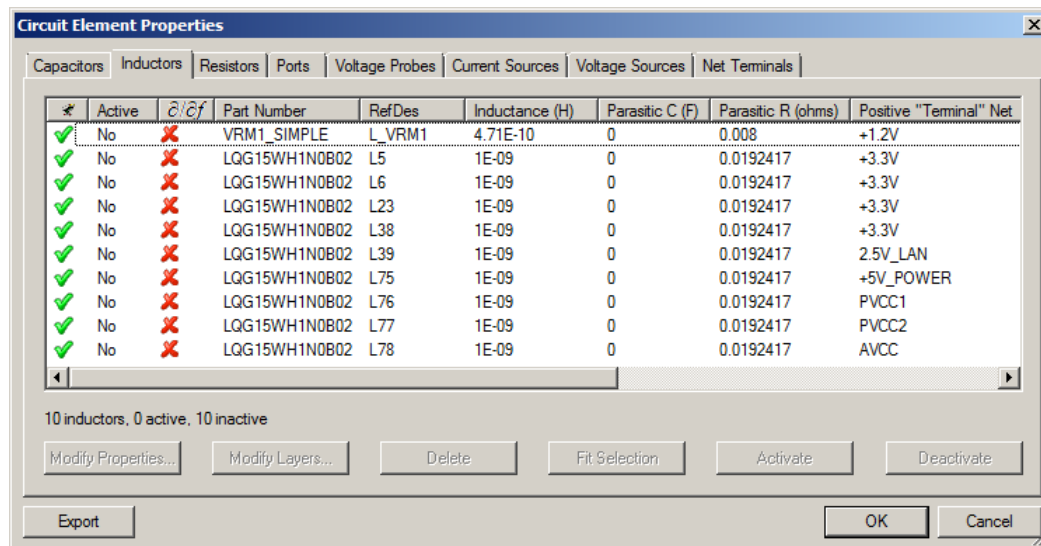
PI Advisor Simulation

Capacitor Optimization

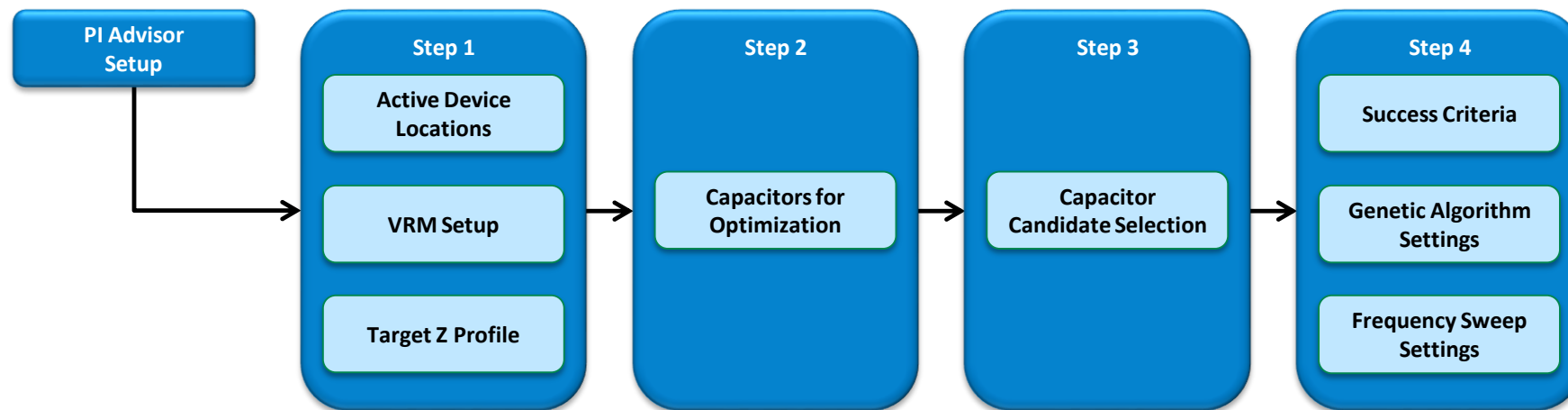


Deactivate Simple VRM Model

- In SIwave on the Home ribbon click the Circuit Element Parameters button
 - Activate the **Inductors** tab
 - Click the **VRM1_SIMPLE** inductor instance L_VRM1 to select it
 - Click the **Deactivate** button to deactivate the simple VRM model
 - Activate the **Ports** tab
 - Click the **VRM1** port to select it
 - Click the **Activate** button to reactivate the port at the VRM output

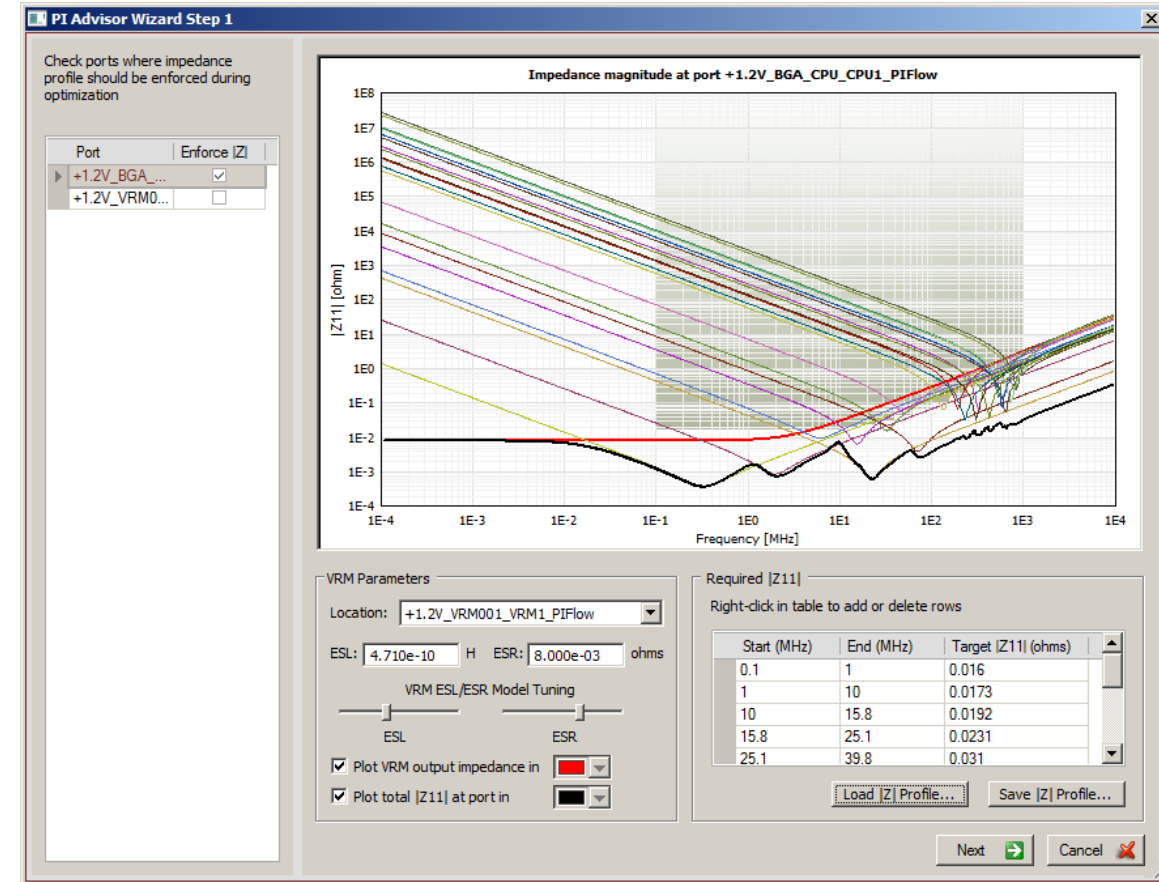


PI Advisor Workflow Diagram



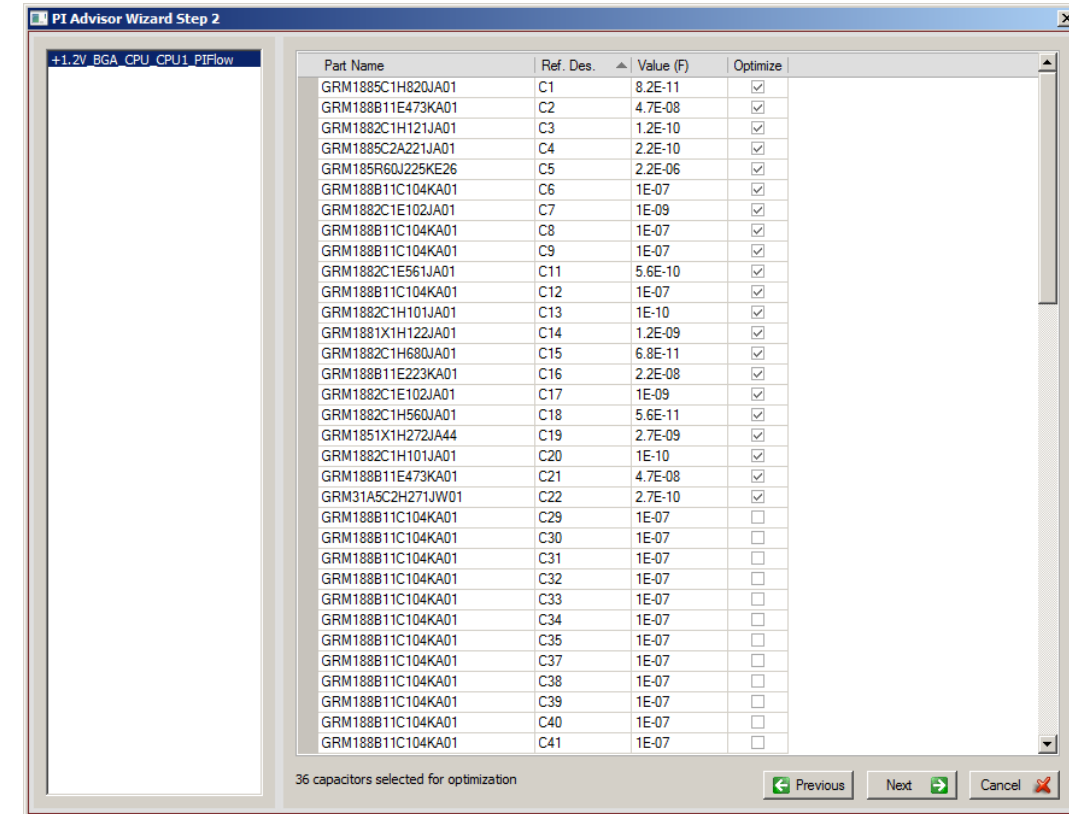
Define Target Impedance and VRM Parameters

- Go to **Simulation** → **PI Advisor** to raise the PI Advisor Step 1 dialog
 - In the list of ports on the left click the Enforce $|Z|$ check box for the **+1.2V_BGA_CPU_CPU1_PIFlow** port
 - Click the **+1.2V_BGA_CPU_CPU1_PIFlow** port to select it
 - In the VRM Parameters area set the following options:
 - Location: **+1.2V_VRM001_VRM1_PIFlow**
 - ESL: **0.471e-9 H**
 - ESR: **8e-3 ohm**
- In the Required $|Z_{11}|$ area you can right click and select **Add Row** to add a target impedance between a minimum and maximum frequency, but in this case we have provided a loadable target due to the large number of steps
 - Click the **Load $|Z|$ Profile** button, browse to the file **PI_advanced.zprof** and select it, and click Open to load the target impedance profile
 - After reviewing the settings click the Next button to advance to Step 2



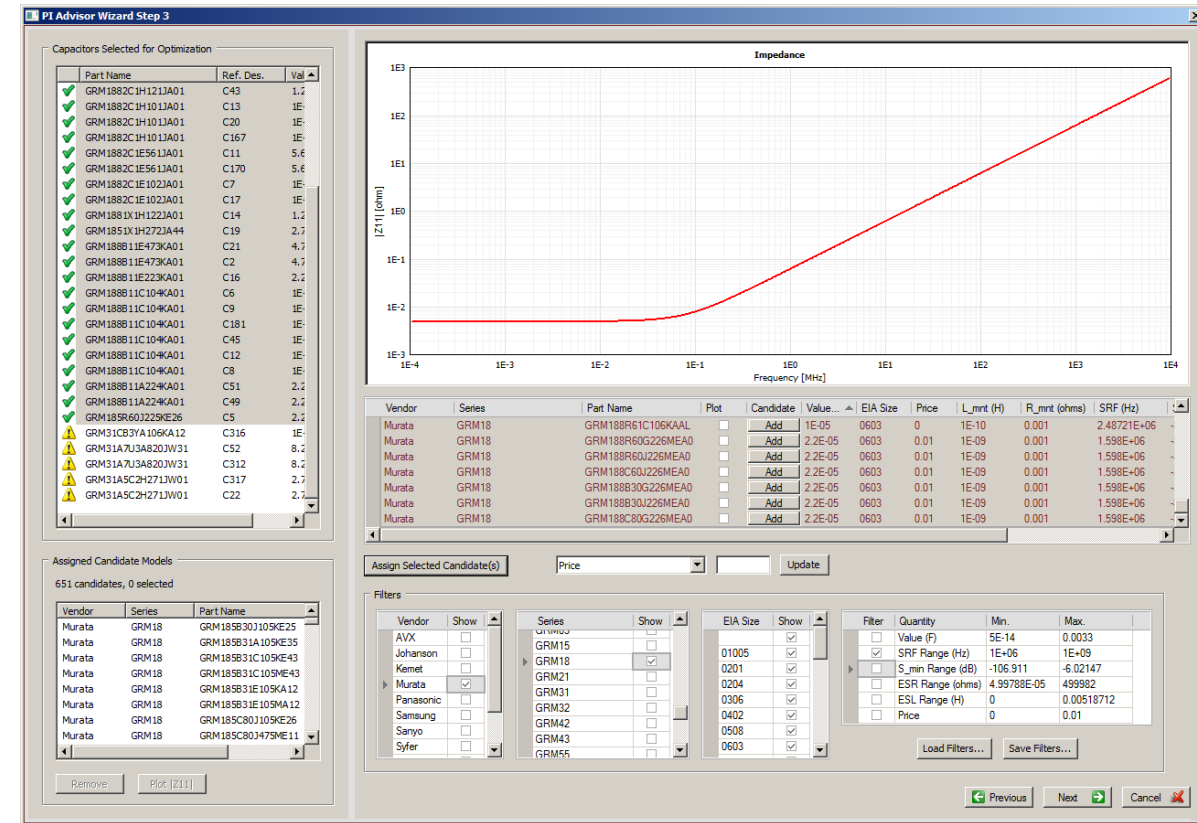
Select Capacitors To Optimize

- In this step we will select the capacitor locations we want to optimize; the list will display all the capacitors that are visible to the ports selected for enforcing the impedance magnitude, but not all these capacitors are directly connected
 - To sort the list by reference designator, click the Ref Des column header
- Select the following capacitor reference designators:
 - C1-9
 - C11-22
 - C43
 - C45-49
 - C51-52
 - C167
 - C170
 - C180-181
 - C312
 - C316-317
- Confirm that there are **36 capacitors** selected for optimization before clicking the Next button to advance to the next step

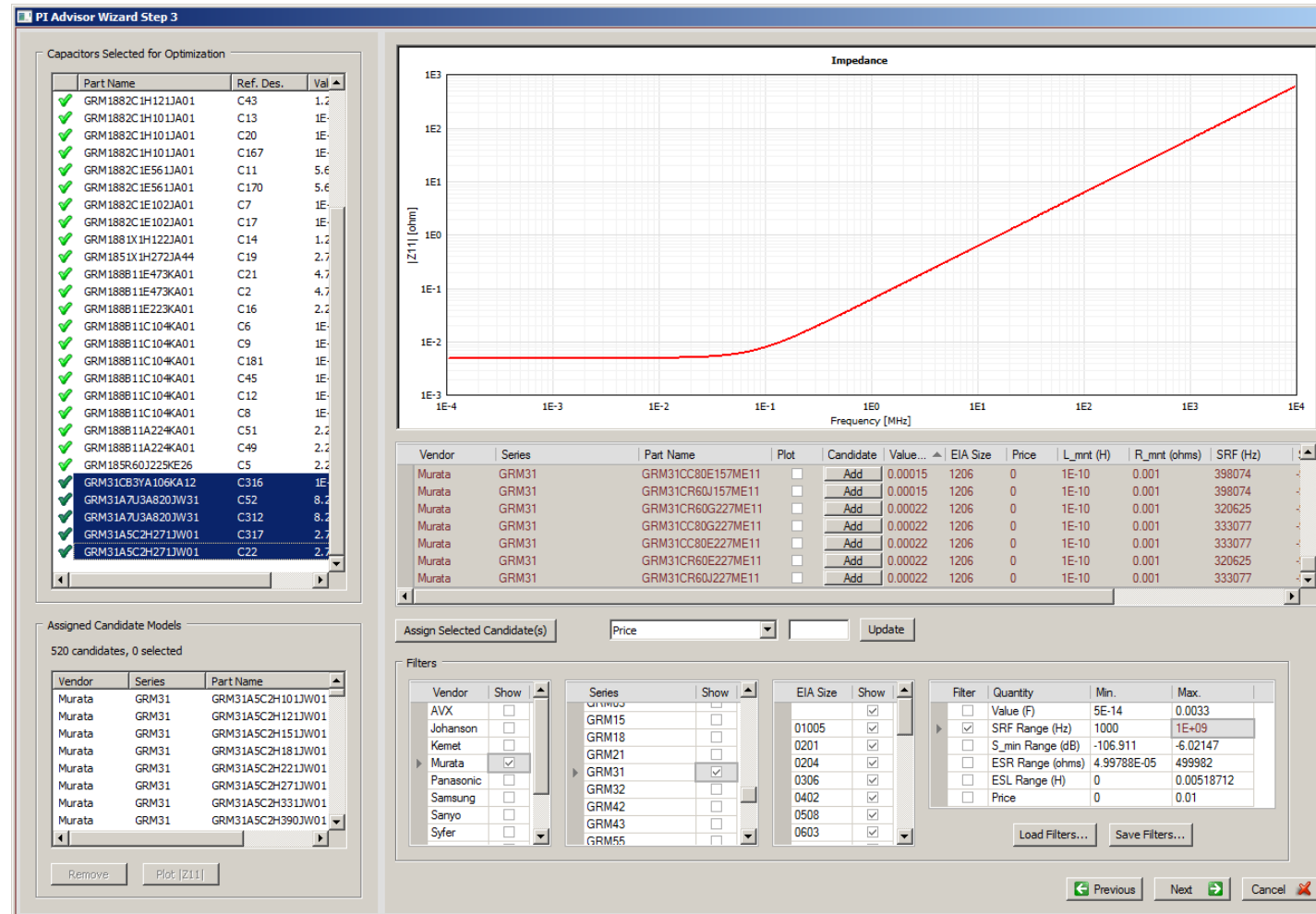


Select Candidate Capacitors

- Select candidate capacitor models for each reference designator to be optimized
 - In the **Capacitors Selected For Optimization** area click the **Part Name** column header to sort the list by part name
 - Select all the parts with part names beginning with **GRM18**
- In the **Filters** area:
 - Click the Show header in the **Vendor** list to turn off all Vendors
 - Click the Show check box for **Murata** to show only parts from this vendor
 - Click the Show header in the **Series** list to turn off all Series
 - Click the Show check box for **GRM18** to show only parts from this series
 - Click the Filter check box for the **SRF Range** filter to turn it on and enter **1e9**
- Select all the capacitor models in design
 - Click the **Assign Selected Candidates** button
 - Repeat this process to assign all capacitor models matching the same set of filters except with **Series GRM31** for the capacitors with part names beginning with **GRM31**
- Click Next to advance to the next step

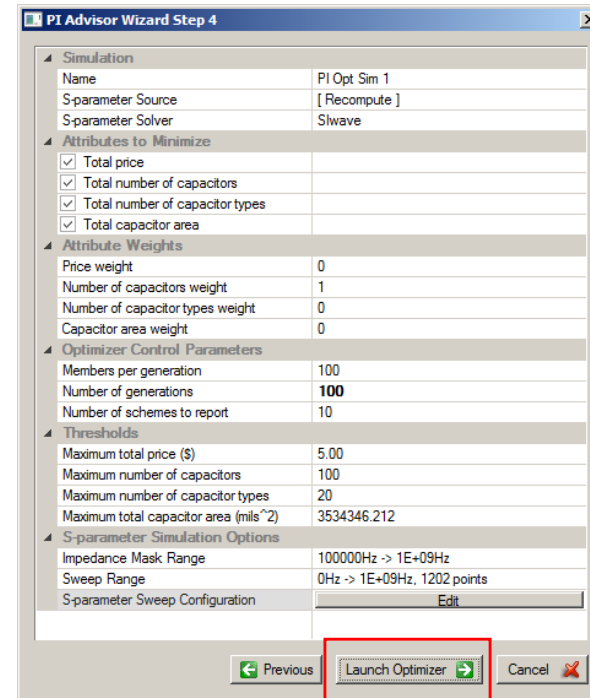
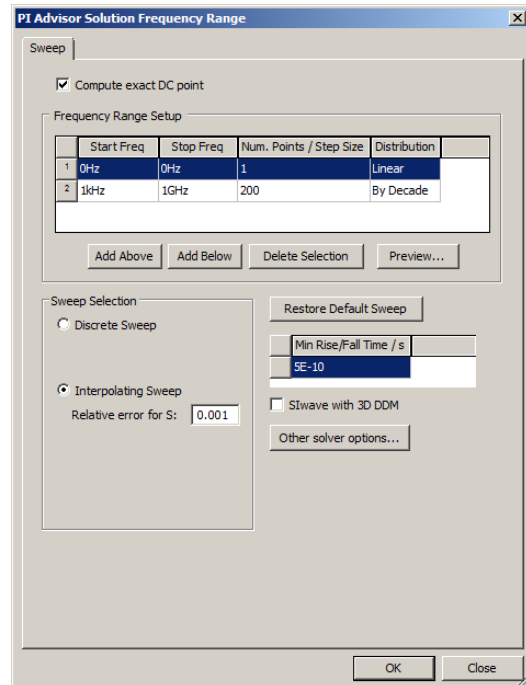
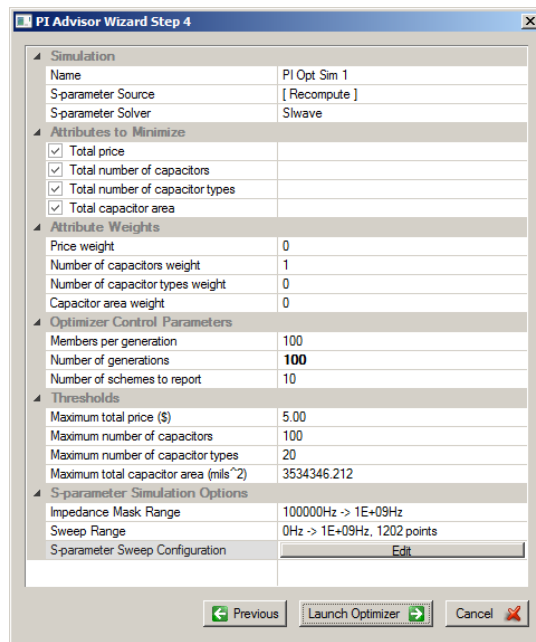


Select Candidate Capacitors for 1206-size Locations



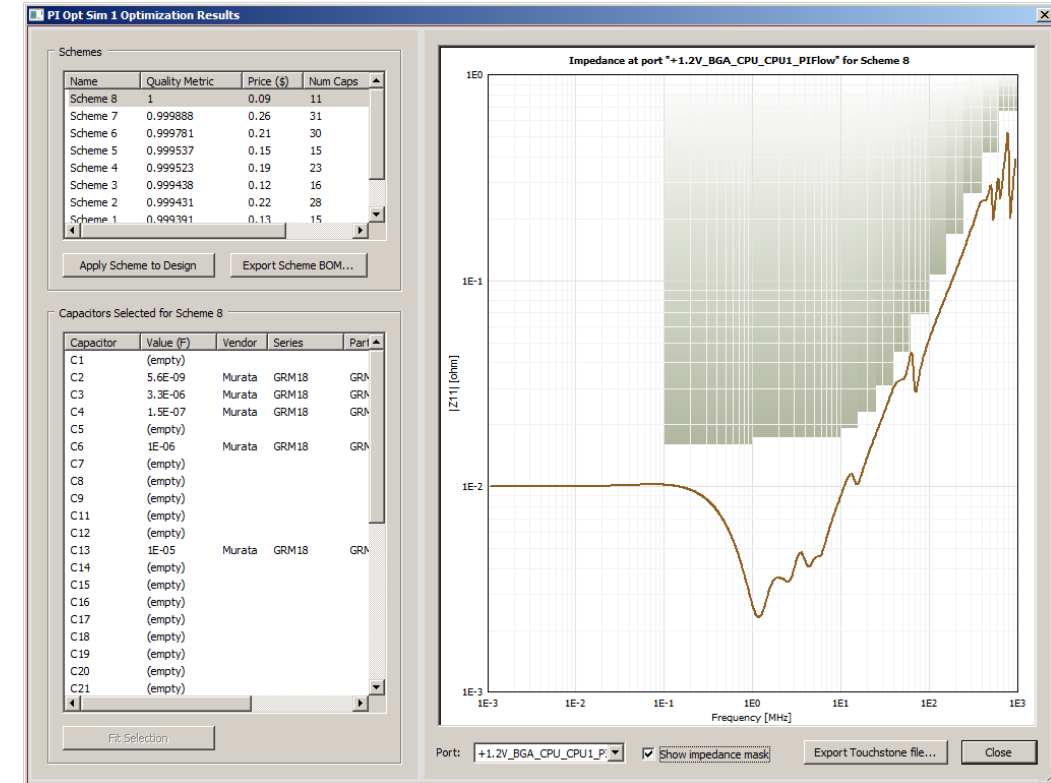
Set Up PI Advisor Simulation

- Enter **PI Opt Sim 1** in the Name text box
- Enter **100** in the Number of Generations text box
- Click the Edit button in the S-parameter Sweep Configuration row
 - Configure as shown and select OK
- Click Launch Optimizer to launch the simulation



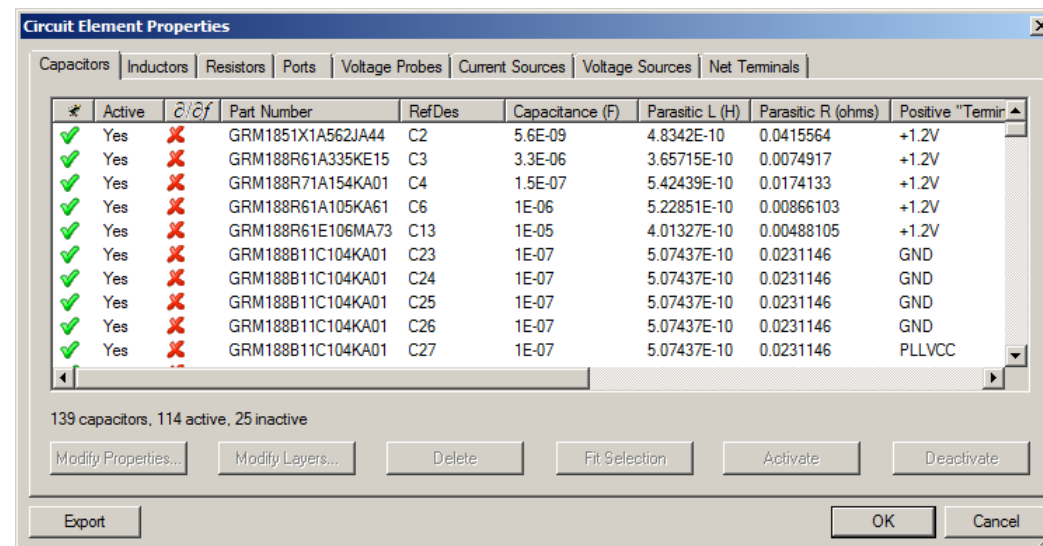
PI Advisor Result

- Go to **File** → **Save As** and save the project as **PI_advanced_optimized.siw**
- On the Results ribbon click **PI Advisor > PI Opt Sim 1 > View Schemes** to examine the PI Advisor results
 - Click **Scheme 8** to select it
 - Turn on the **Show Impedance Mask** check box
 - Note that this scheme has just **11 capacitors versus 36** in the original design, indicating that the PCB was overdesigned for the PDN requirements
 - Click the **Apply Scheme To Design** button to assign the capacitors for this scheme to the design
 - Capacitors marked (empty) will be deactivated
 - Capacitors marked with a part name will have that candidate model applied
- Click **Close** to close the dialog



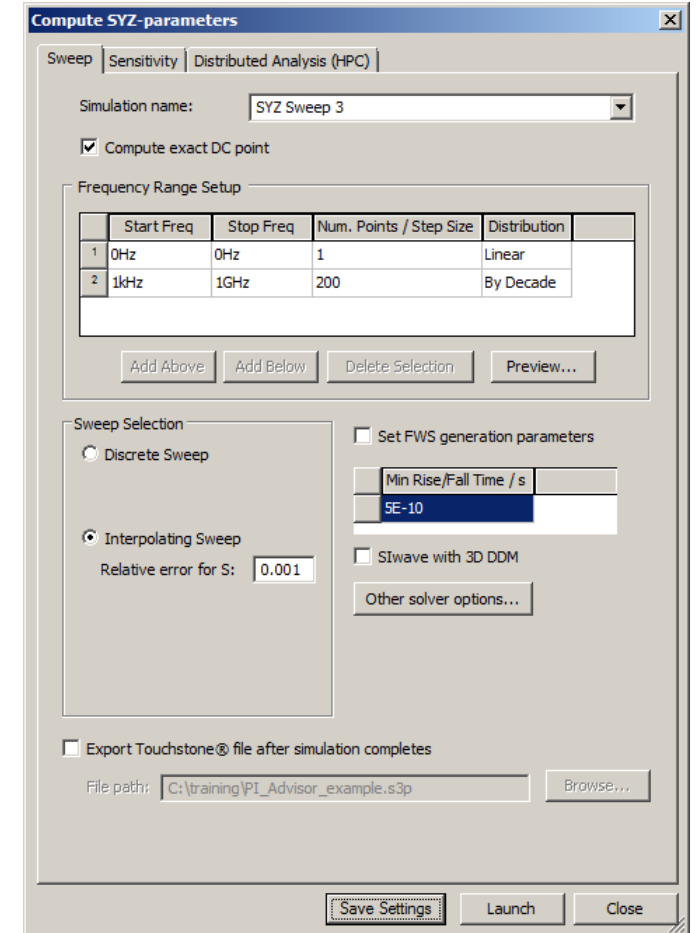
Confirm Scheme Applied To Design

- On the Home ribbon click the Circuit Element Parameters button
- In the capacitors list confirm that there are now 25 inactive capacitors; these are the capacitors that were marked (empty) in the PI Advisor scheme applied to the design
- Click OK to close the dialog



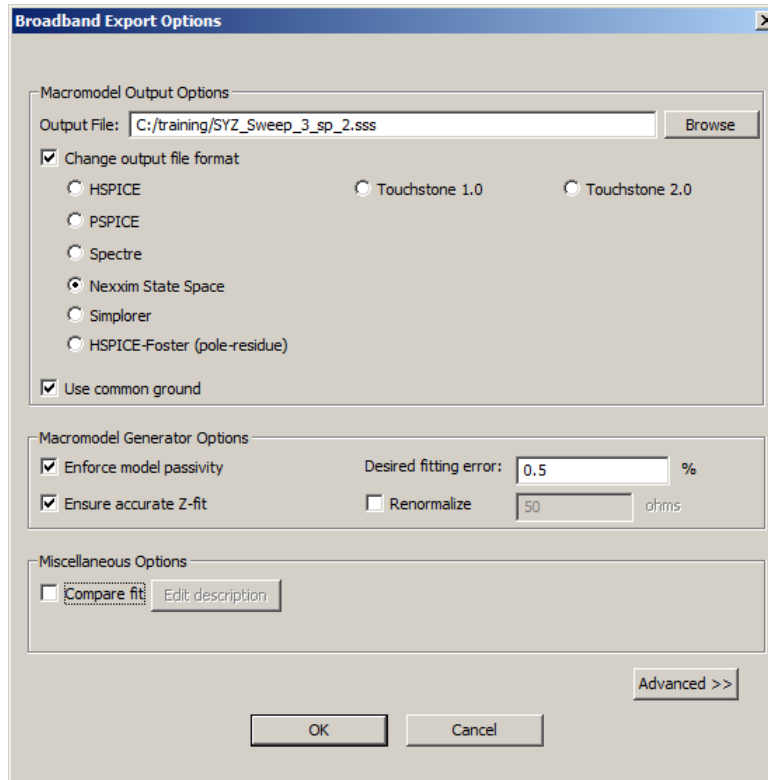
Set Up S-parameter Simulation

- On the Simulation ribbon click the **Compute SYZ Parameters** button
 - Enter **SYZ Sweep 3** in the Simulation Name text box
 - Turn on the **Compute Exact DC Point** check box
 - Set up the following frequency ranges using the Add Above/Add Below/Delete Selection buttons:
 - 0 Hz to 0 Hz, 1 point, Linear
 - 1 kHz to 1 GHz, 200 points, By Decade
 - Select the Interpolating sweep option button and enter 0.001 in the Relative Error for S text box
 - Turn off the Export Touchstone File After Simulation Completes check box
- Click **Launch** to start the S-parameter simulation



Export State-Space Model for Circuit Simulation

- On the **Results ribbon select SYZ > SYZ Sweep 3 > Compute FWS Subcircuit**
 - Turn on the Change Output File Format check box and select the **Nexxim State Space** option button
 - Turn on the **Enforce Model Passivity** check box
 - Click Browse to specify a file name and location; save the model in the same directory as your Siwave projects
- Click **OK** to generate and export the model

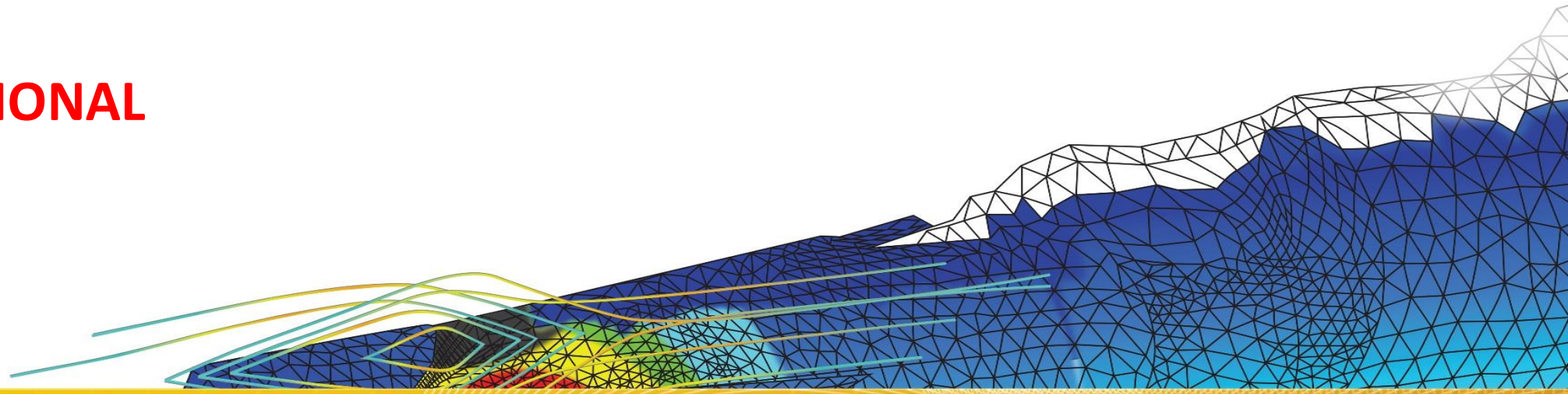




Validation and Post-processing

Transient VRM testbench

OPTIONAL



Opening ANSYS Electronics Desktop

Starting ANSYS Electronics Desktop

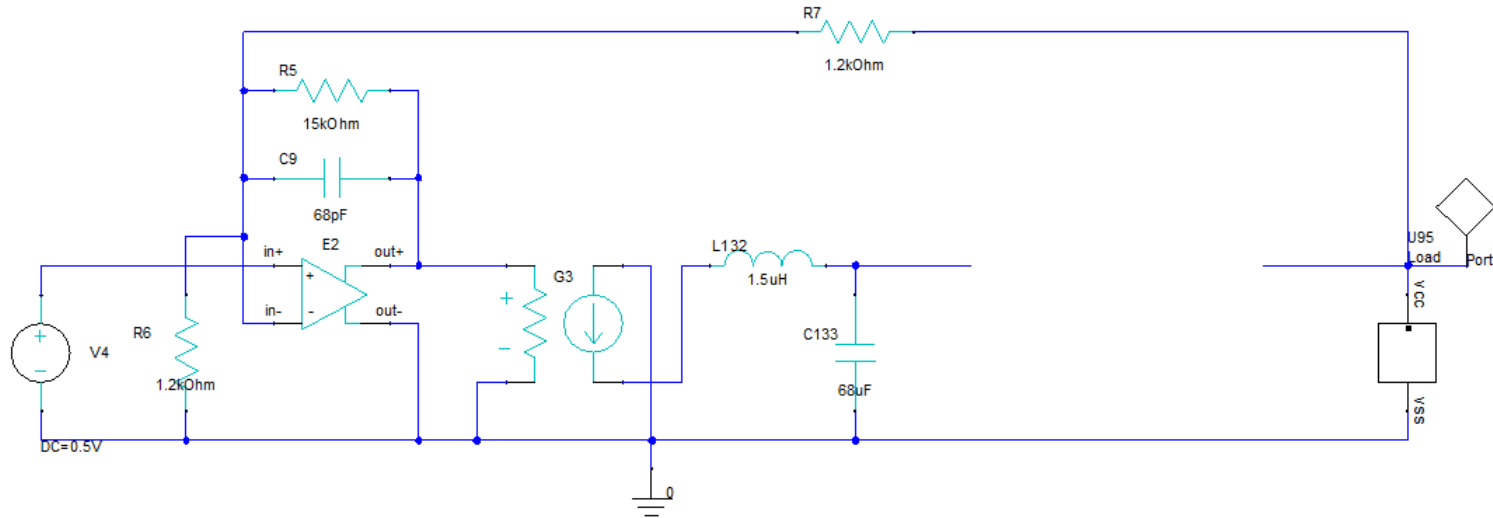
- To launch SIwave, click the Microsoft **Start Button** > **ALL Programs** > **ANSYS Electromagnetics** > **ANSYS Electromagnetics Suite 18.0**
- Select the **ANSYS Electronics Desktop 2017.0** executable.

Open an Electronics Desktop Project

- Select the **File** > **Open** menu item
 - Browse to the file: **PI_advanced_circuit.aedt**
 - Click the **Open** button

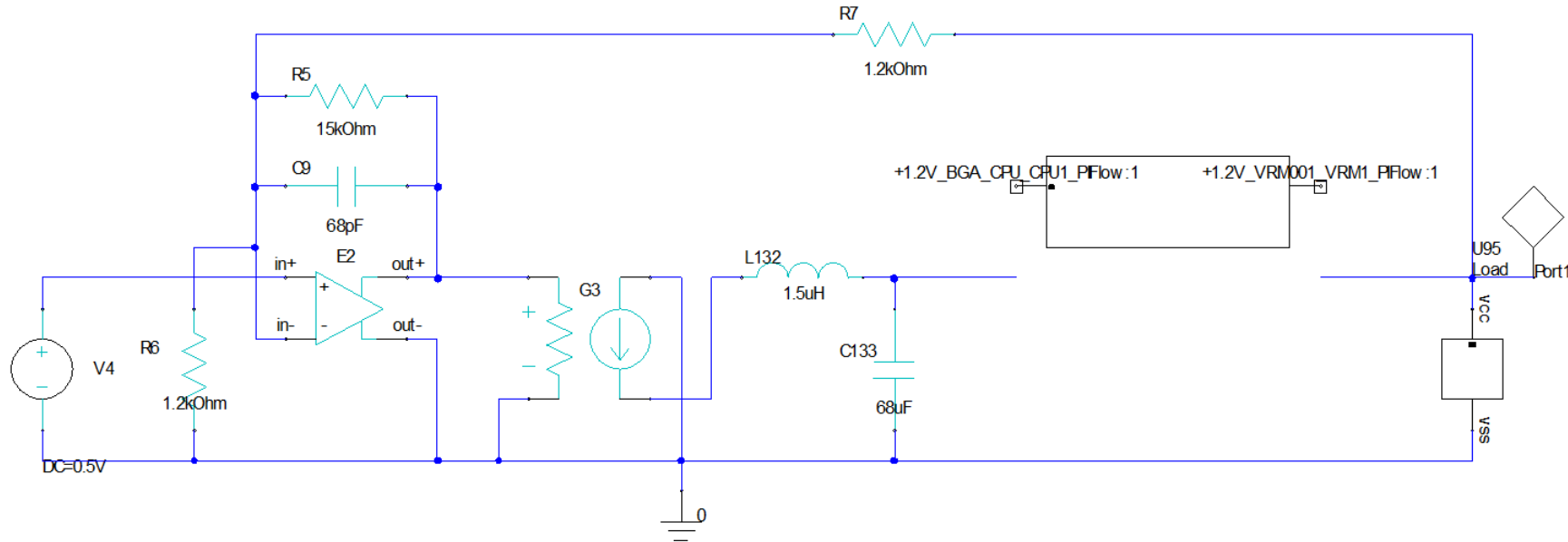
PDN Impedance Measurement Circuit

- Double click on the [Optimized PDN Z design](#) to open the schematic
- We will add the State Space model just generated to this circuit to compute the full PDN impedance



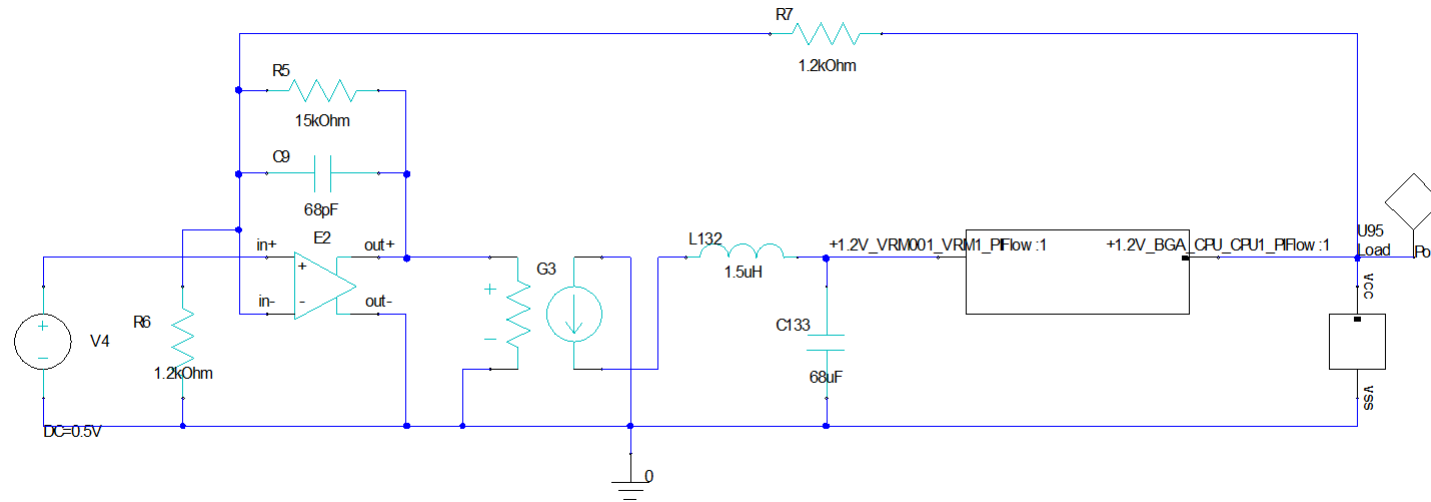
PDN Impedance Measurement Setup

- In the **Component Libraries** window click the **Import Models** button to show just importable model types
 - Click **SSS** to activate the state space model importer
 - Browse to and select the **SYZ_Sweep_3_sp_2.sss** file and click Open to import the model
 - Click in the schematic to place the component in a way that it is not connected to any wires because it needs to be flipped before connecting

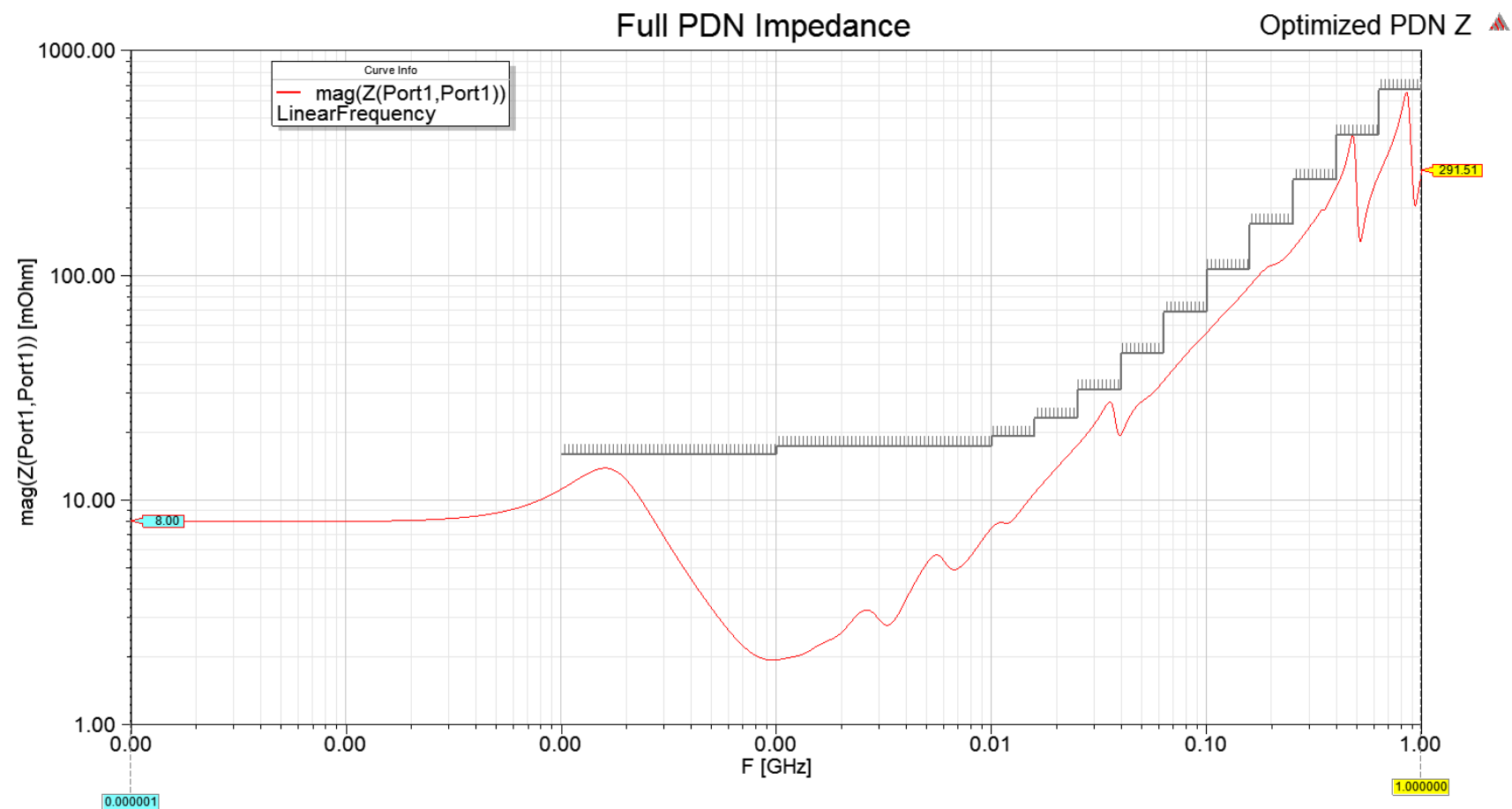


PDN Impedance Measurement

- Right-click on the state-space model component and select **Flip Horizontal** to flip it
 - Click and drag on the component to connect it to the existing wires between the VRM model and the load
- Expand **Optimized PDN Z > Analysis**, right click on the **LinearFrequency** solution setup, and click Analyze to run the impedance simulation
- Expand **Optimized PDN Z > Results** and double click on the report named **Full PDN Impedance** to open the report and examine the results

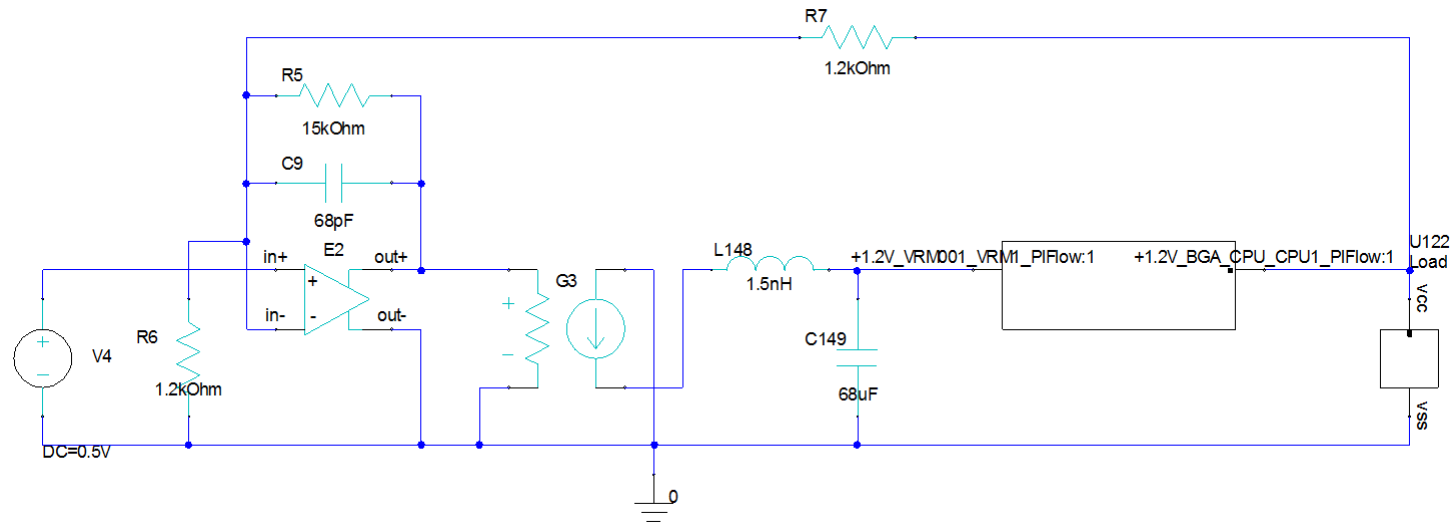


PDN Impedance (Board + Optimized Capacitors + VRM)



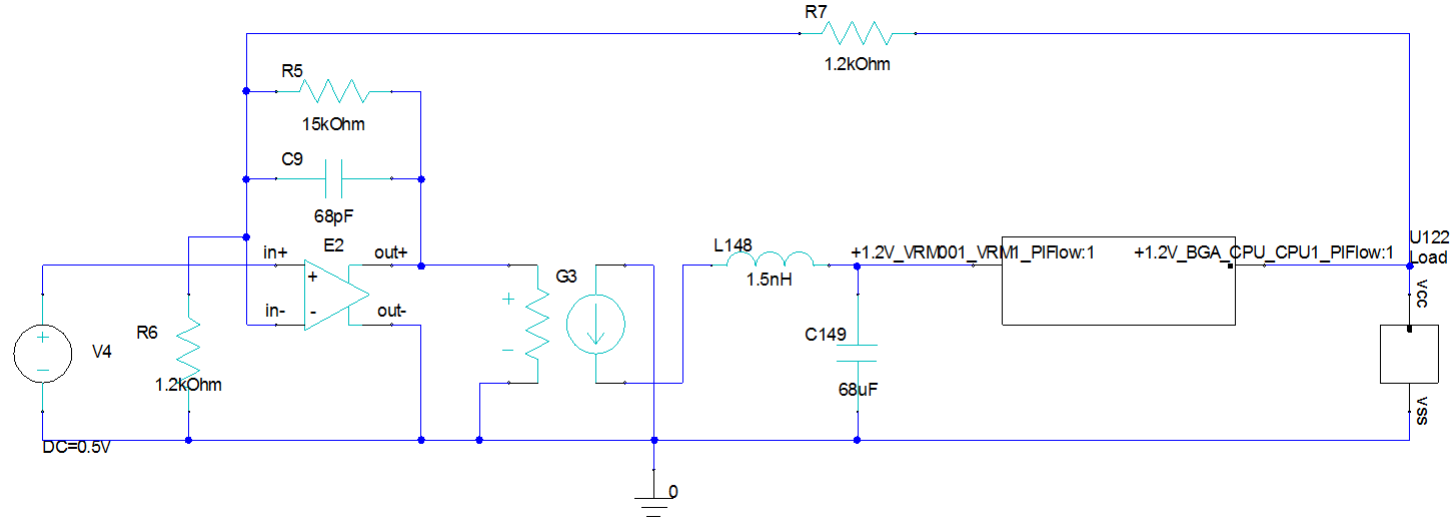
Setup PDN Transient Circuit

- In the Project Manager double click on **Optimized PDN Transient** to open the schematic for the time domain simulation of the PDN
 - In the Component Libraries window click the **Proj** button to display just the components in the current project
 - Click and drag out an instance of the **SYZ_Sweep3_sp_2** model into the schematic
 - As for the impedance circuit flip the model instance and connect it to the other models



Run PDN Transient Circuit Simulation

- Expand **Optimized PDN Transient > Analysis**, right click on the **Nexxim Transient** solution setup, and select **Analyze** to run the simulation
- Expand **Optimized PDN Transient > Results** and double click on the report named **Load Voltage** to open the report and examine the results



Load Voltage Swing Within 50 mV Target!

