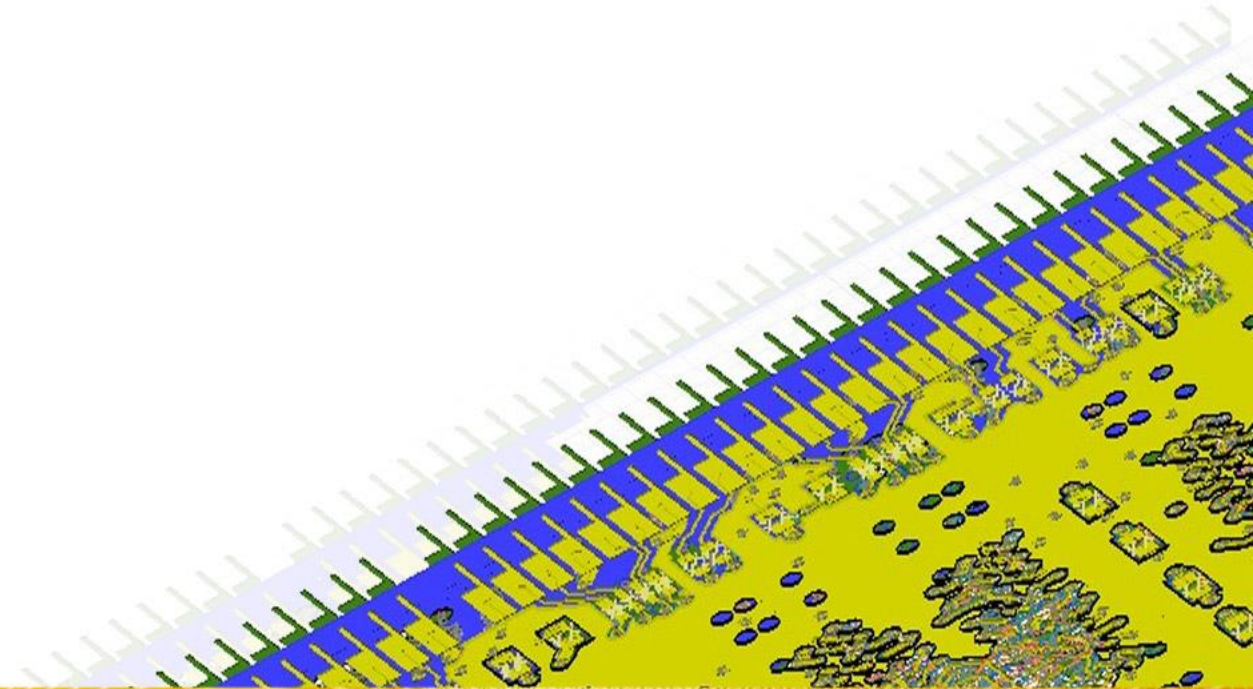


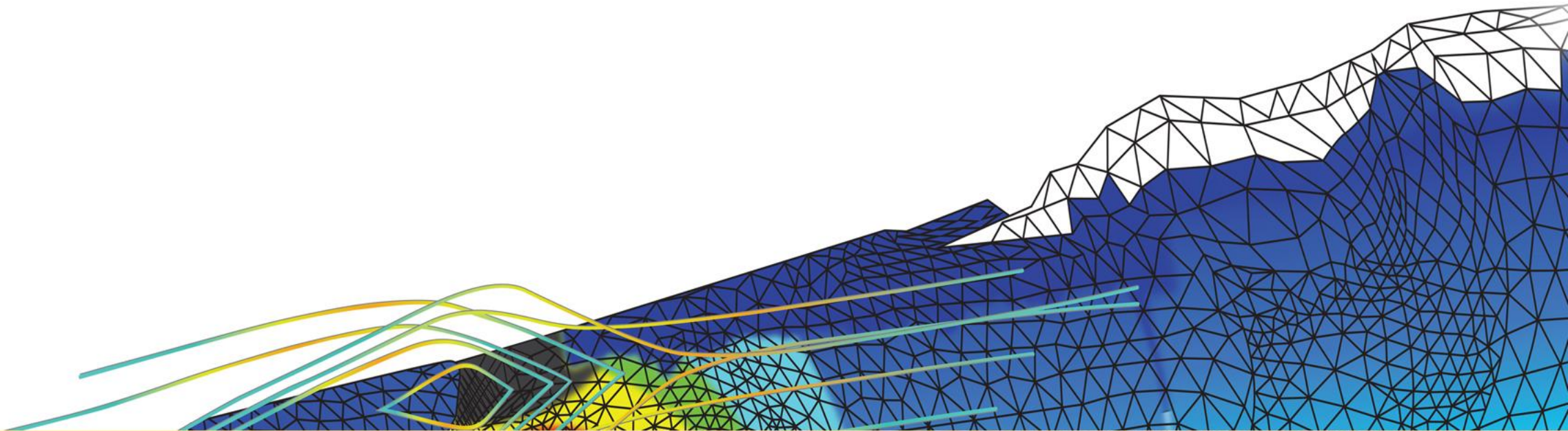


## Power Integrity Analysis using SIwave



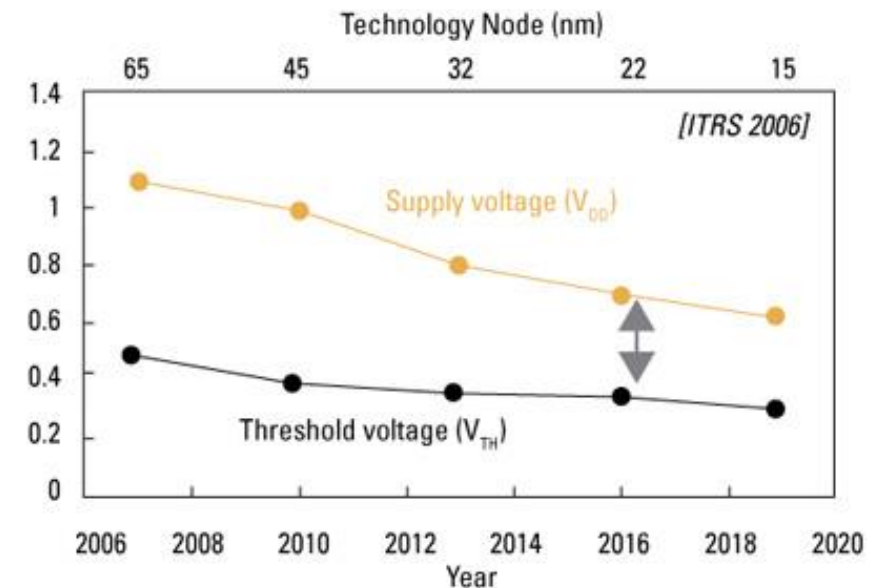


## DCIR Analysis



# Why is it important to run DC IR simulations?

- Supplying clean and sufficient power to today's high speed semiconductors
- More functionality into every integrated circuit is desired
- Being able to operate many different IC functions into an ever shrinking area
- Simulation helps:
  - Avoid DC current crowding in planes, traces and vias which can lead to PCB failures and bad circuit performance
  - Debug existing PCB designs, making minor layout changes that result in major performance and reliability improvements
  - Reduce design spins
  - Decrease warranty costs associated with thermal-cycling issues





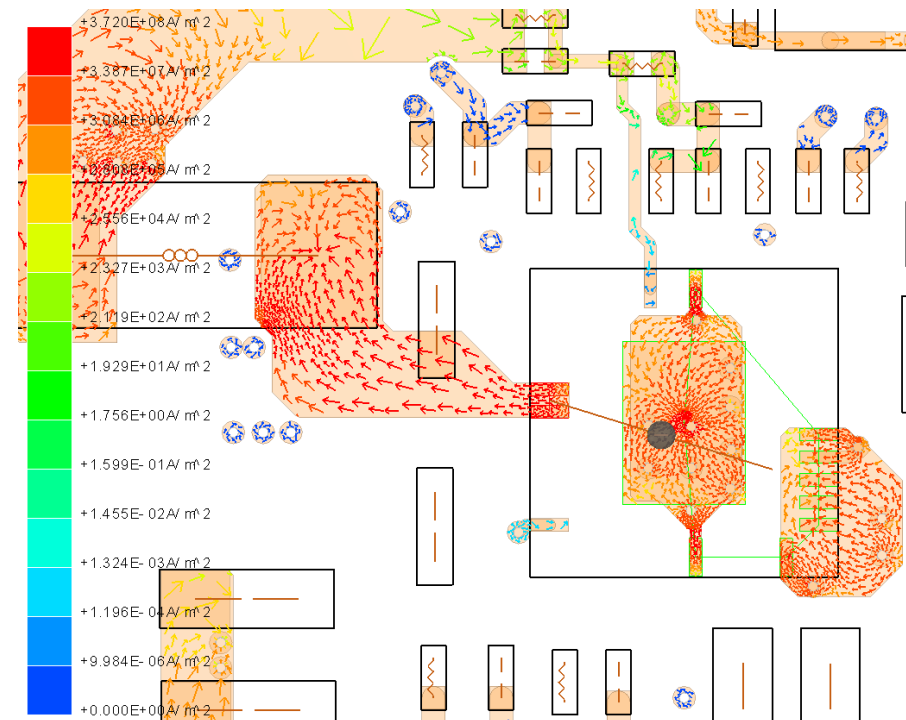
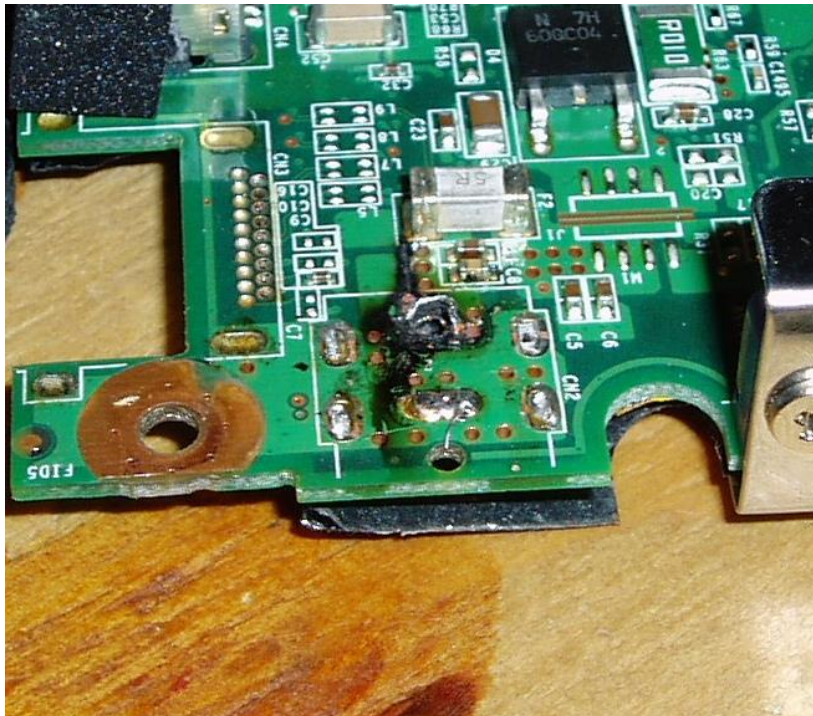
# The Importance of DC Simulations

- Failures

- Lack of good DC design may not lead to high DC resistance but it can cause **thermal hot spots** due to excessive temperatures and eventual product failure.

- Solution

- Robust and accurate DC and PDN design results in a more even spread of current density and reduces risk of failure.



# Joule Heating

- **What is Joule Heating?**

- Joule heating / resistive heating is the process by which the passage of electric current (  $I$  ) through a conductor of electrical resistance (  $R$  ) releases heat (  $\dot{Q}$  )

$$\dot{Q} = I^2 R$$

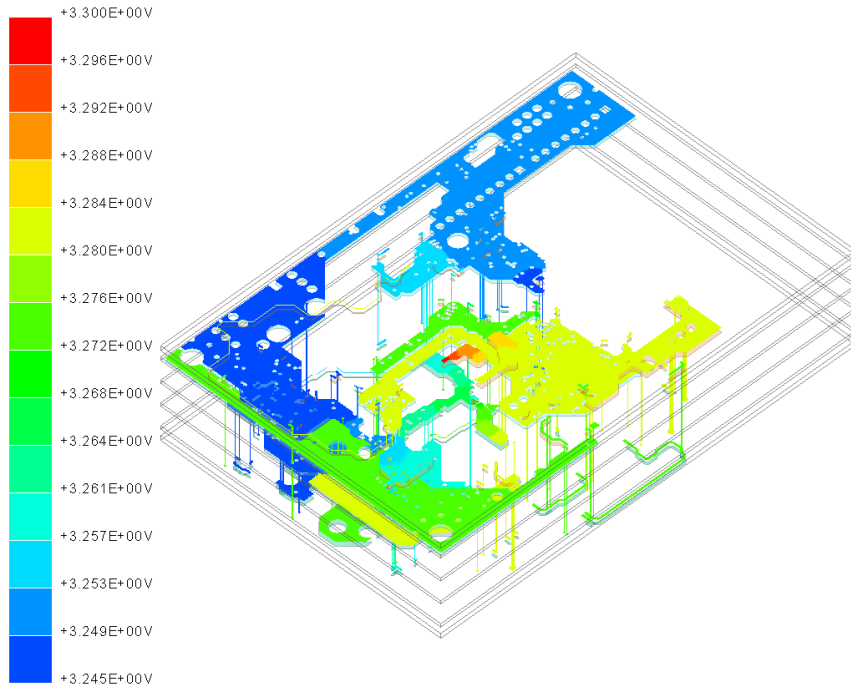
- **Why do we need to perform thermal analysis on printed circuit boards?**

- High current PCB's are densely populated with components
  - Reduction of trace and via dimensions
  - Current densities increase
- Joule heating effects on copper traces → Temperatures increase → Reliability issues → PCB delamination and failure

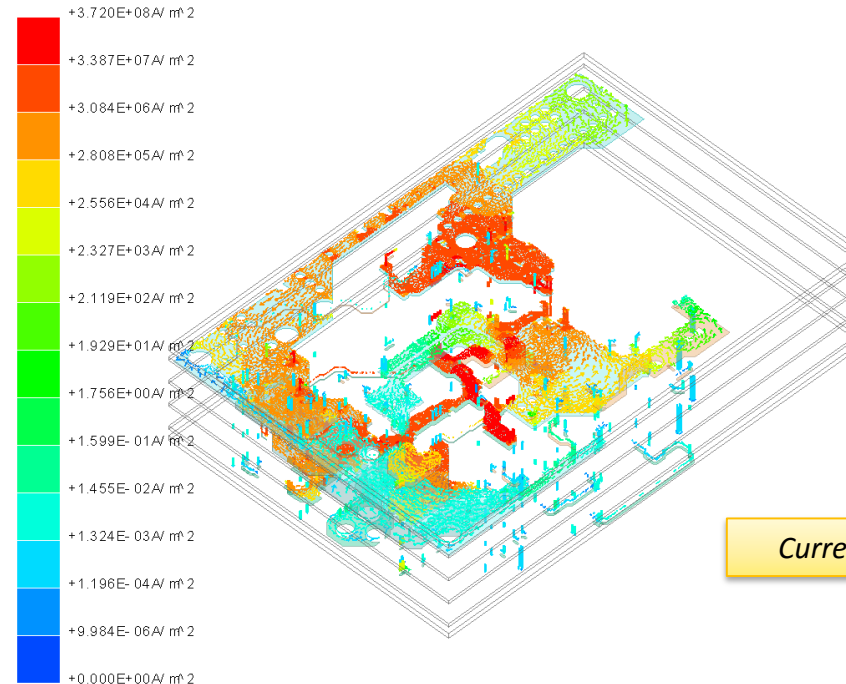
# Siwave-DC Solutions

- Import, setup, and simulate DC power delivery Network
- Combine Chip, Package and Board to perform System Level analysis

- DC IR drop (Voltage) for all nets including Power, Ground, and Signals.
- DC current distribution (Amperes/Area<sup>2</sup>) including return paths.
- DC current magnitude (Amperes) into and out of vias.
- Power density (W/Area<sup>2</sup>) and total power loss (Watts) per layer.
- Automated report generation with user defined pass/fail criteria.
- Bi-directional coupling to Icepak for thermal loss simulations



Voltage Drop across a power rail

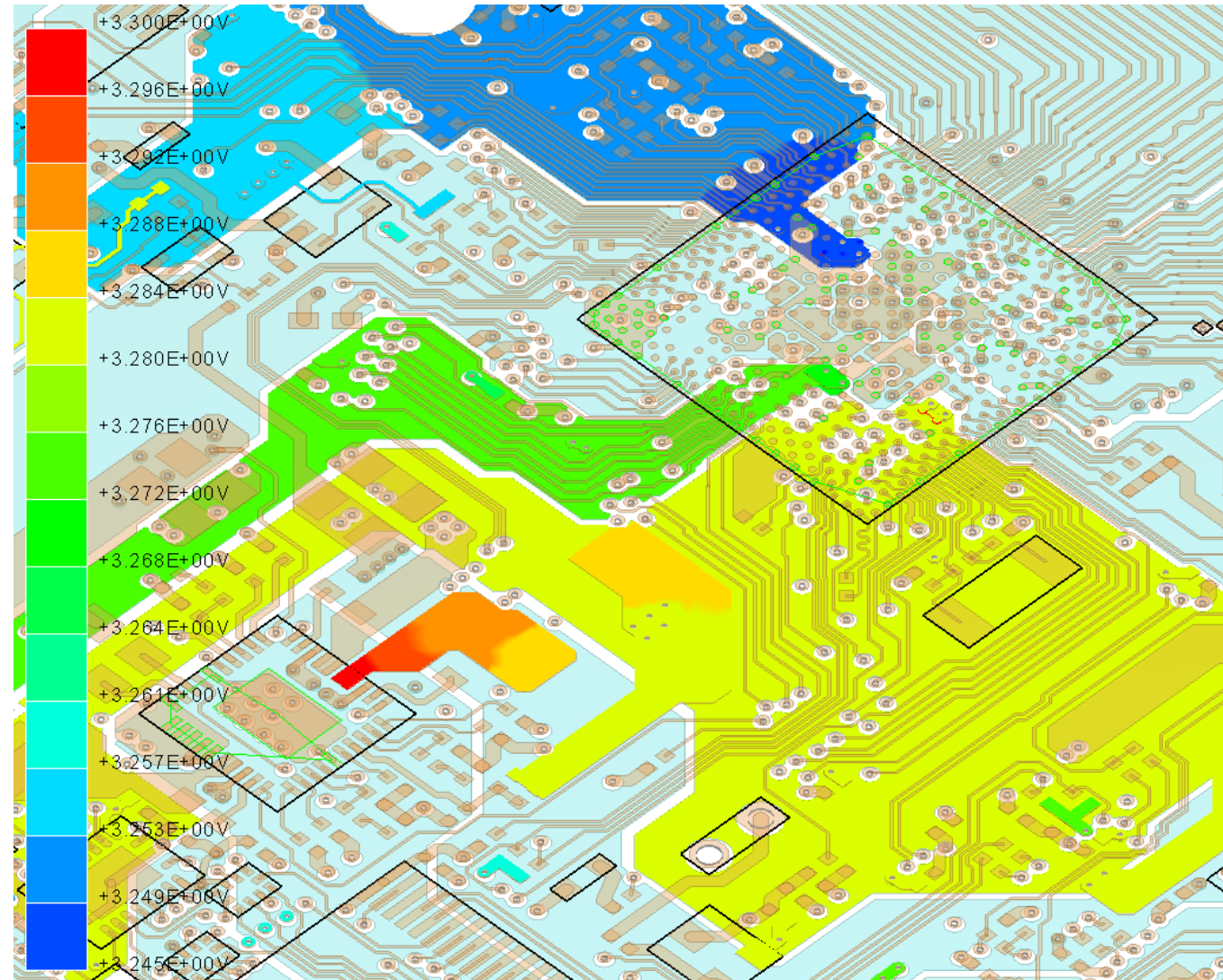


Current Distribution across a power rail



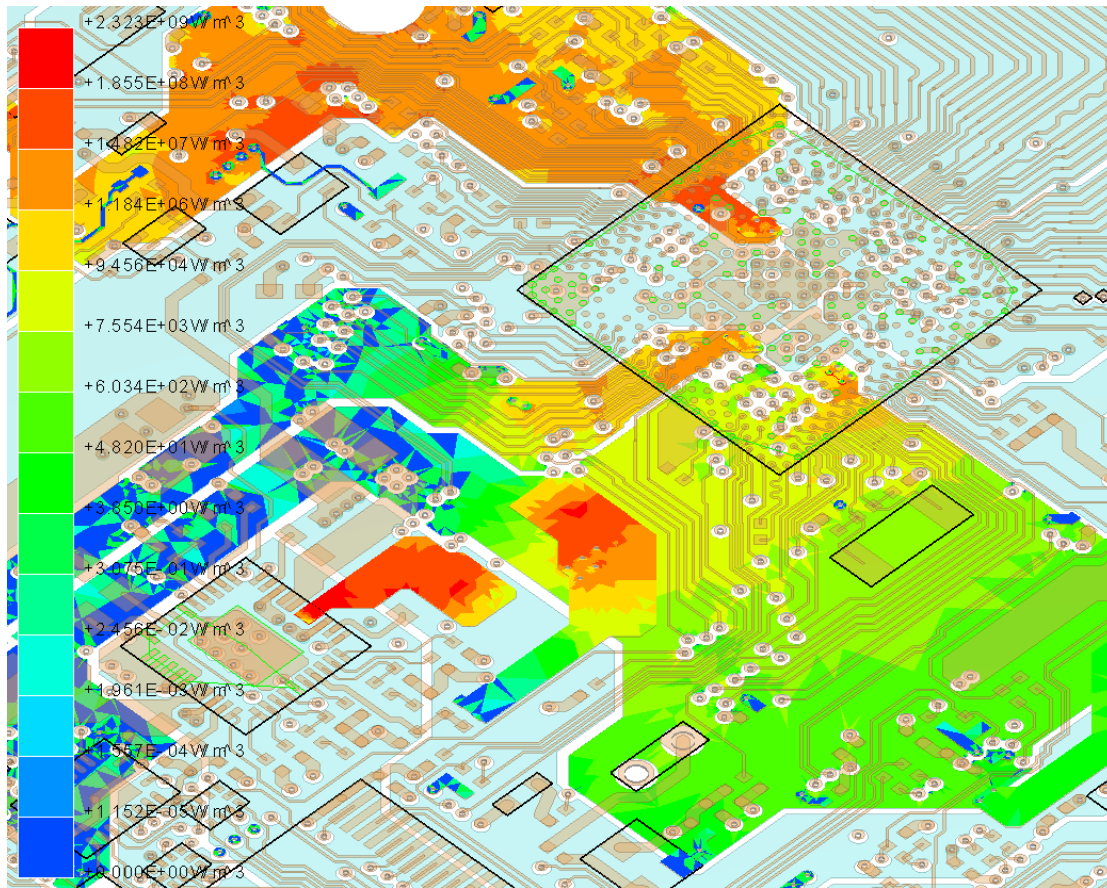
# IR Drop with SIwave-DC

*Voltage Drop from Power Supply to Active Devices*

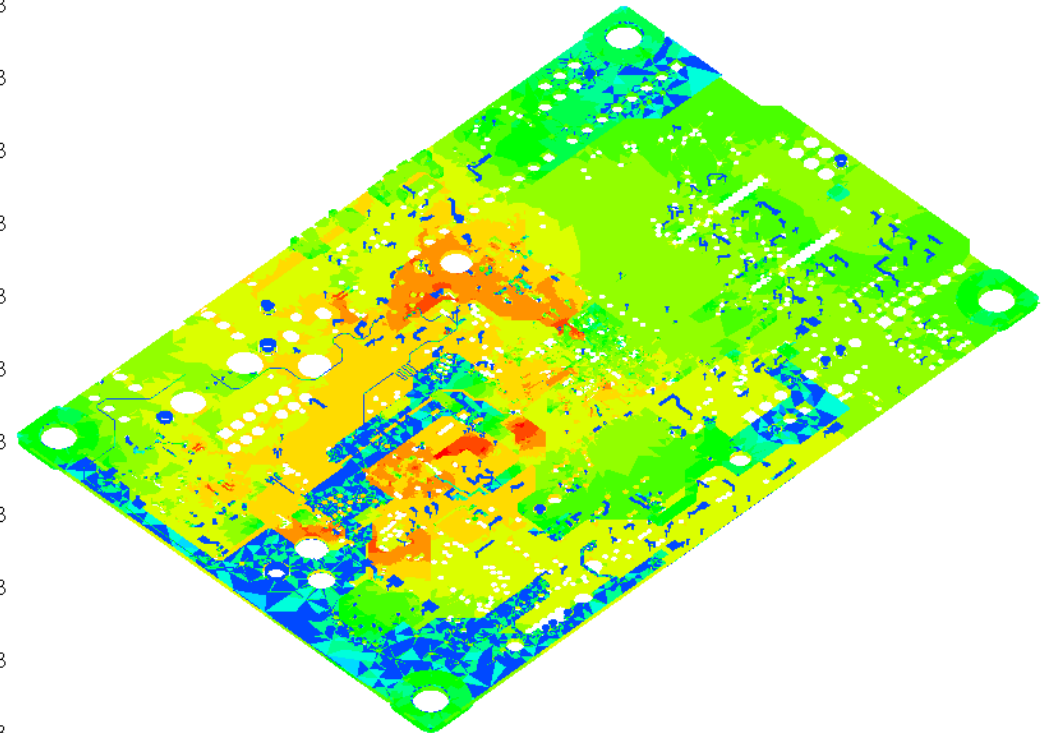
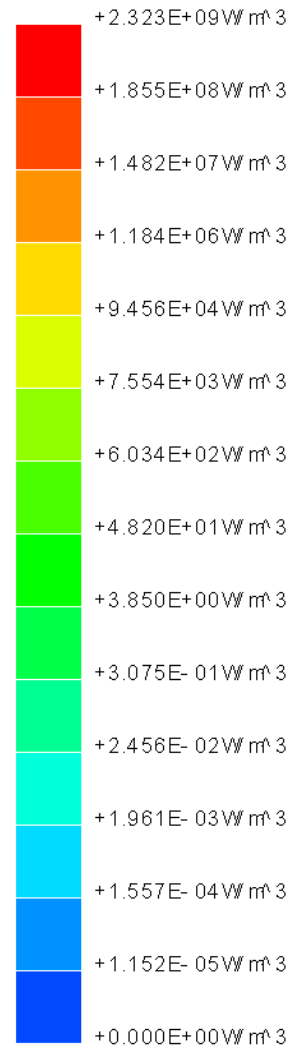


# IR Drop with Slwave-DC

Quickly Identify High Power regions



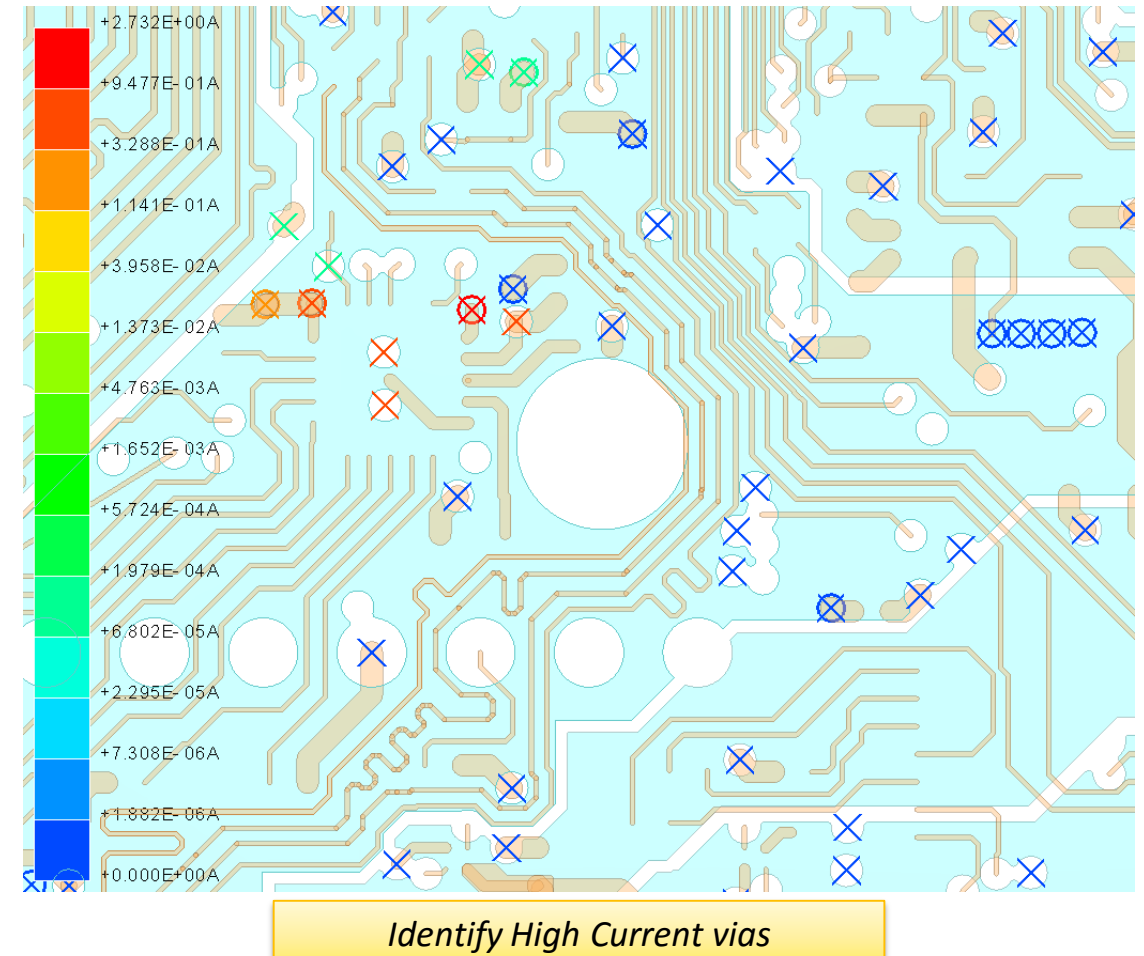
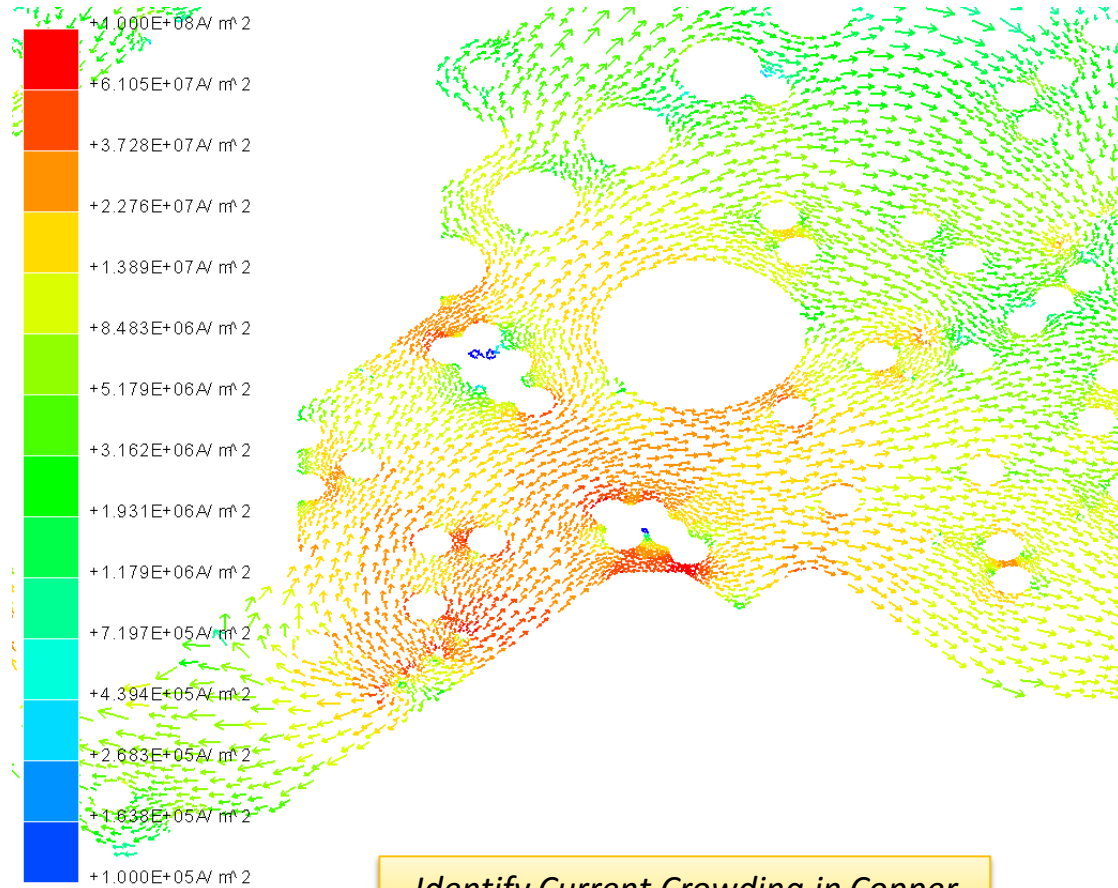
Power Loss across a specific Net



Power Loss across all geometry



# IR Drop with SIwave-DC



# SIwave-DC Tabular Element Data

DC Simulation Element Data(DC IR Sim 1)

Bondwires Current Sources Metallization Vias Voltage Probes Voltage Sources

| Via                | Net     | x (mm)     | y (mm)     | Current / A         | Limit / A          | Pass / Fail | Resistance / Ohms  | IR Drop / V         | Power / W          |
|--------------------|---------|------------|------------|---------------------|--------------------|-------------|--------------------|---------------------|--------------------|
| Via 14 (PWR-BO...  | V3P3_S5 | 5.7480e+01 | 4.0157e+01 | 1.710957311026e+00  | 1.641732232276e+00 | Fail        | 8.054497150167e-04 | 1.378090078572e-03  | 2.357853295185e-03 |
| Via 15 (TOP-PWR)   | V3P3_S5 | 5.6718e+01 | 4.0183e+01 | 2.731681960131e+00  | 1.641732232276e+00 | Fail        | 1.404435419627e-04 | 3.836470899965e-04  | 1.048001834800e-03 |
| Via 15 (PWR-BO...  | V3P3_S5 | 5.6718e+01 | 4.0183e+01 | 1.936616449037e+00  | 1.641732232276e+00 | Fail        | 8.054497150169e-04 | 1.559847166974e-03  | 3.020825681546e-03 |
| Via 84 (TOP-PWR)   | V3P3_S0 | 3.9751e+01 | 3.1928e+01 | -1.669258665420e+00 | 1.641732232276e+00 | Fail        | 1.404435419627e-04 | -2.344365994236e-04 | 3.913353250794e-04 |
| Via 14 (TOP-PWR)   | V3P3_S5 | 5.7480e+01 | 4.0157e+01 | 1.797983192812e+00  | 1.641732232276e+00 | Fail        | 1.404435419632e-04 | 2.525151279889e-04  | 4.540179560548e-04 |
| Via 0 (TOP-BOTT... | V3P3_S5 | 2.6289e+01 | 5.3061e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 9.146835809879e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 1 (TOP-LYR_1)  | V3P3_S5 | 7.4625e+01 | 5.8268e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 3.613120182118e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 1 (LYR_1-BO... | V3P3_S5 | 7.4625e+01 | 5.8268e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 5.821804944608e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 2 (TOP-PWR)    | V3P3_S5 | 7.7318e+01 | 3.3757e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 1.404435419627e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 2 (PWR-BOT...  | V3P3_S5 | 7.7318e+01 | 3.3757e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 8.054497150169e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 3 (TOP-LYR_1)  | V3P3_S5 | 8.4557e+01 | 6.0884e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 3.613120182118e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 3 (LYR_1-BO... | V3P3_S5 | 8.4557e+01 | 6.0884e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 5.821804944608e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 4 (TOP-LYR_1)  | V3P3_S5 | 7.2796e+01 | 5.8572e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 3.613120182118e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 4 (LYR_1-BO... | V3P3_S5 | 7.2796e+01 | 5.8572e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 5.821804944608e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 5 (TOP-LYR_1)  | V3P3_S5 | 7.8740e+01 | 5.9868e+01 | 1.843652525238e-11  | 1.641732232276e+00 | Pass        | 3.853994860925e-04 | 7.105427357601e-15  | 1.309993909074e-25 |
| Via 5 (LYR_1-BO... | V3P3_S5 | 7.8740e+01 | 5.9868e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 5.821804944608e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 6 (TOP-LYR_1)  | V3P3_S5 | 8.5166e+01 | 3.8278e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 3.613120182118e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 6 (LYR_1-BO... | V3P3_S5 | 8.5166e+01 | 3.8278e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 5.821804944608e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 7 (TOP-PWR)    | V3P3_S5 | 8.3210e+01 | 3.8684e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 1.404435419627e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 7 (PWR-LYR_1)  | V3P3_S5 | 8.3210e+01 | 3.8684e+01 | -7.786768865485e-10 | 1.641732232276e+00 | Pass        | 2.515078396791e-04 | -1.958433415439e-13 | 1.524986834447e-22 |
| Via 7 (LYR_1-BO... | V3P3_S5 | 8.3210e+01 | 3.8684e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 5.821804944608e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 8 (TOP-PWR)    | V3P3_S5 | 8.3414e+01 | 3.8001e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 1.404435419627e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 8 (PWR-LYR_1)  | V3P3_S5 | 8.3414e+01 | 3.8001e+01 | -7.645831872444e-10 | 1.641732232276e+00 | Pass        | 2.514973270052e-04 | -1.922906278651e-13 | 1.470221811303e-22 |
| Via 8 (LYR_1-BO... | V3P3_S5 | 8.3414e+01 | 3.8001e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 5.821804944608e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 9 (TOP-LYR_1)  | V3P3_S5 | 8.0797e+01 | 5.8674e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 3.613120182118e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 9 (LYR_1-BO... | V3P3_S5 | 8.0797e+01 | 5.8674e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 5.821804944608e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 10 (TOP-PWR)   | V3P3_S5 | 4.8438e+01 | 4.5136e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 1.404435419627e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 10 (PWR-BO...  | V3P3_S5 | 4.8438e+01 | 4.5136e+01 | 0.000000000000e+00  | 1.641732232276e+00 | Pass        | 8.054497150169e-04 | 0.000000000000e+00  | 0.000000000000e+00 |
| Via 11 (TOP-PWR)   | V3P3_S5 | 4.3197e+01 | 3.9719e+01 | -1.588847948745e-01 | 1.641732232276e+00 | Pass        | 1.404435419683e-04 | -2.231434335709e-05 | 3.545409867050e-06 |
| Via 11 (PWR-BO...  | V3P3_S5 | 4.3197e+01 | 3.9719e+01 | -1.050609985199e-02 | 1.641732232276e+00 | Pass        | 8.054497149746e-04 | -8.462135131282e-06 | 8.890403665028e-08 |
| Via 12 (TOP-PWR)   | V3P3_S5 | 4.3197e+01 | 4.0430e+01 | -2.011152708993e-01 | 1.641732232276e+00 | Pass        | 1.404435419627e-04 | -2.824534098789e-05 | 5.680569404423e-06 |
| Via 12 (PWR-BO...  | V3P3_S5 | 4.3197e+01 | 4.0430e+01 | 1.050609995620e-02  | 1.641732232276e+00 | Pass        | 8.054497150592e-04 | 8.462135216103e-06  | 8.890403842326e-08 |
| Via 13 (TOP-PWR)   | V3P3_S5 | 5.7455e+01 | 4.0869e+01 | 1.365175058363e+00  | 1.641732232276e+00 | Pass        | 1.404435419627e-04 | 1.917300205956e-04  | 2.617450420565e-04 |
| Via 13 (PWR-BO...  | V3P3_S5 | 5.7455e+01 | 4.0869e+01 | 1.372868968130e+00  | 1.641732232276e+00 | Pass        | 8.054497150172e-04 | 1.105776919136e-03  | 1.518086817956e-03 |
| Via 16 (TOP-PWR)   | V3P3_S5 | 5.8318e+01 | 4.0894e+01 | 1.070507826481e+00  | 1.641732232276e+00 | Pass        | 1.404435419627e-04 | 1.503459108498e-04  | 1.609464742441e-04 |

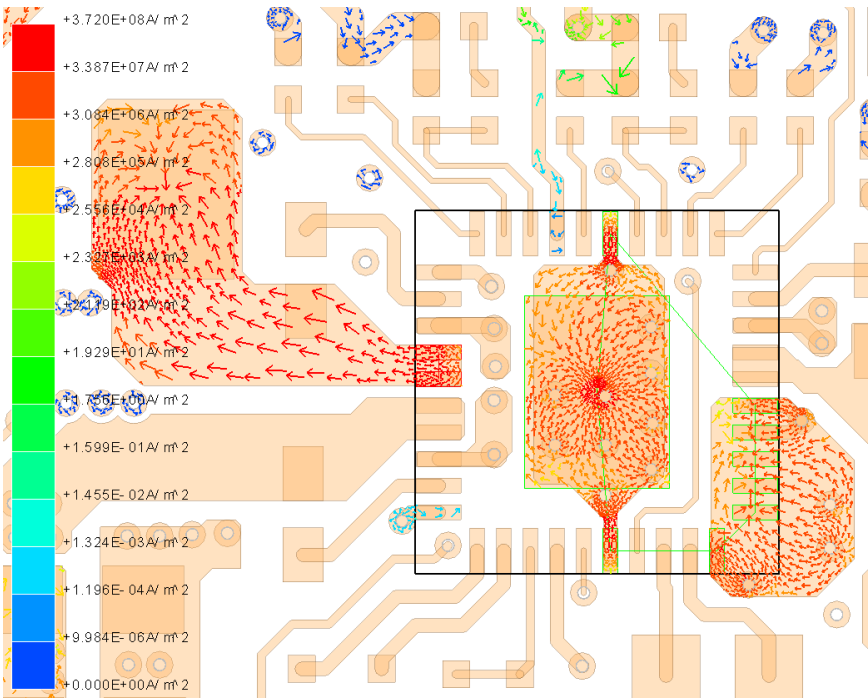
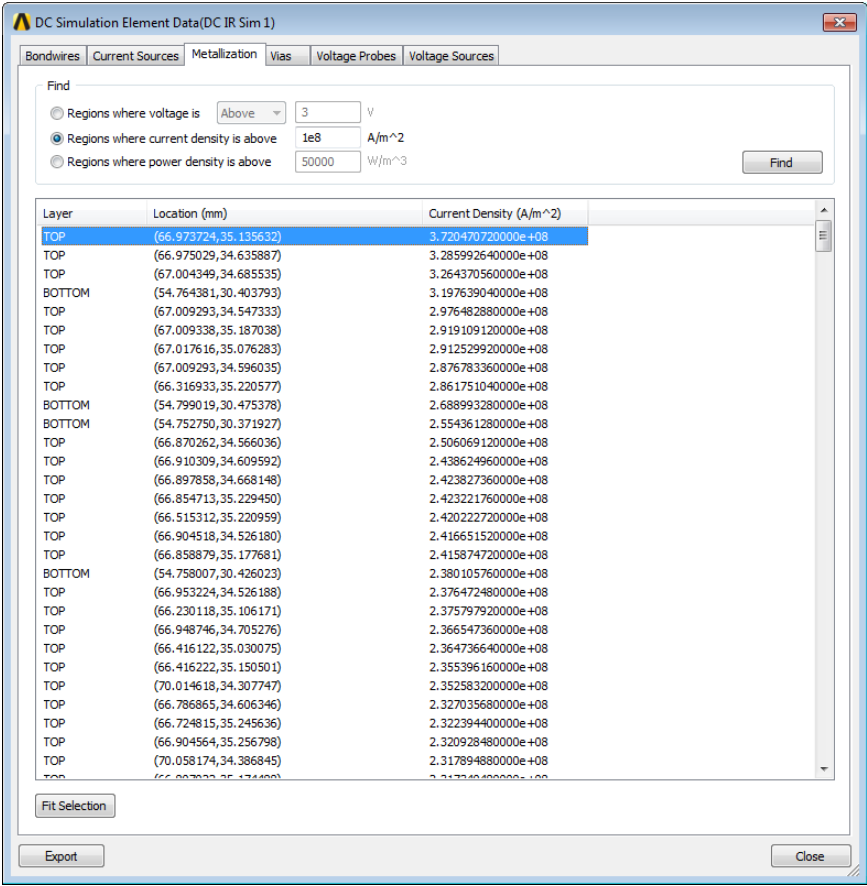
Fit Selection

Export

Via Current Density Check

Close

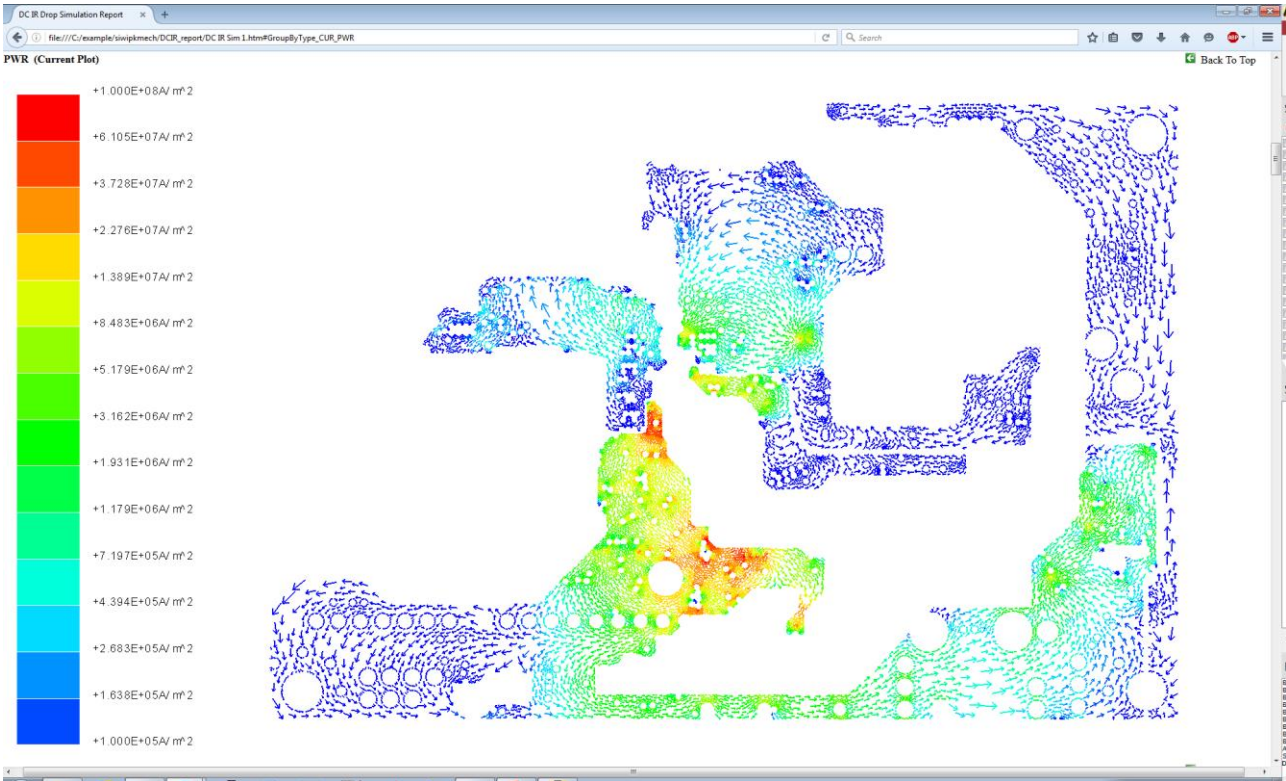
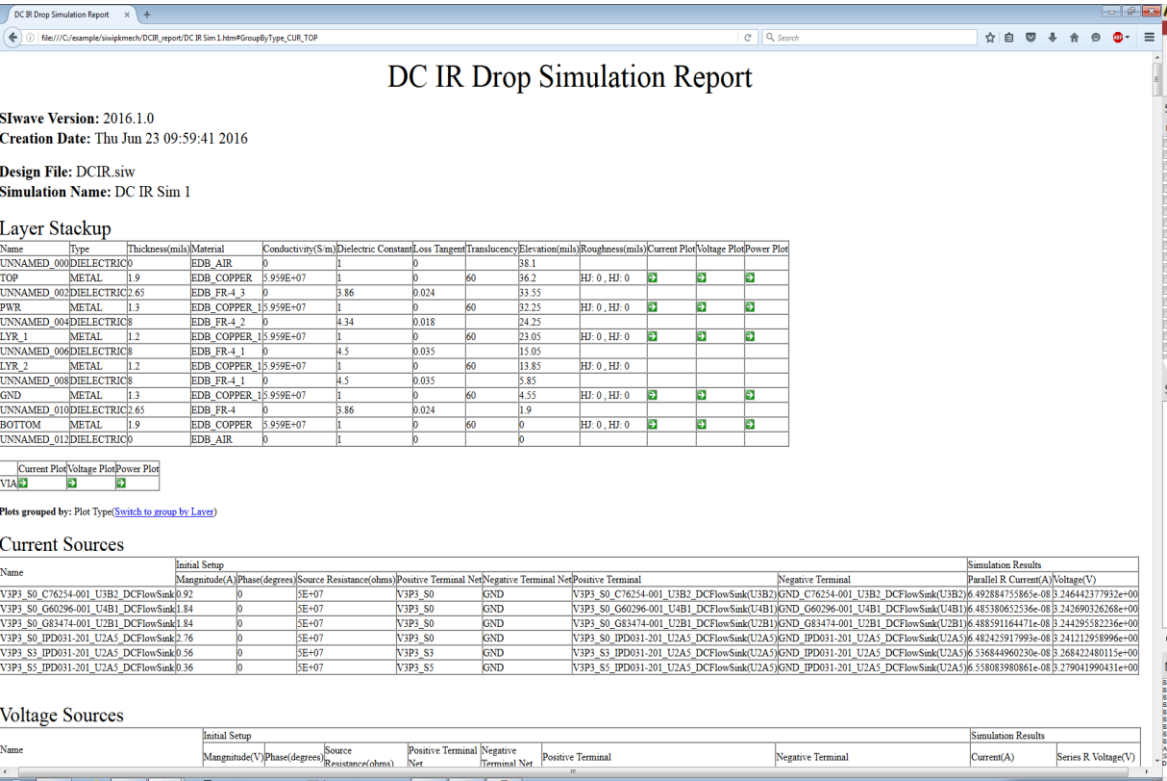
# SIwave-DC Tabular Element Data



Metallization Current Density Check



# SIwave-DC Automated Report

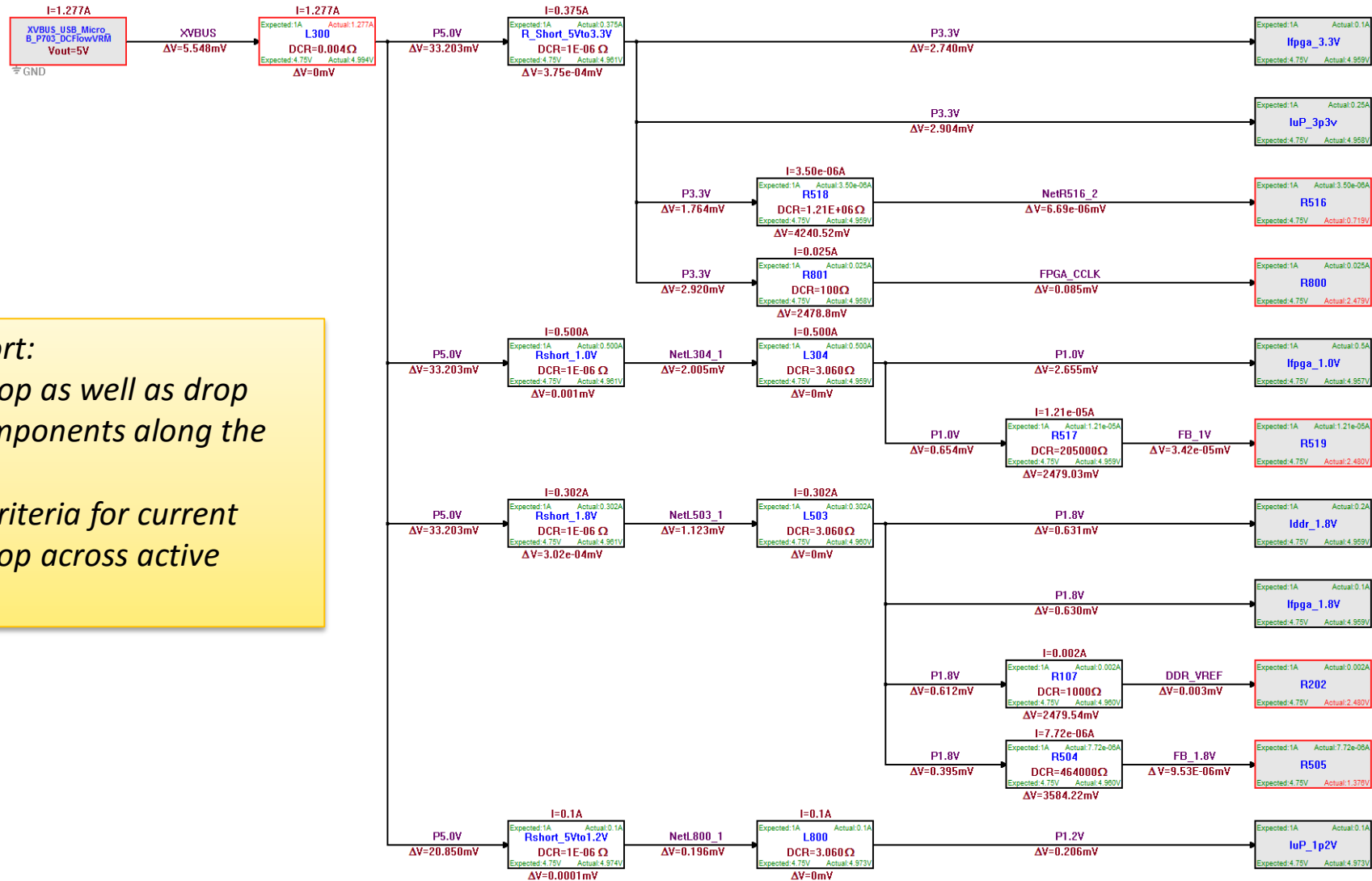


- Fully Automated Report:
- Set Voltage/Current Limits
  - HTML or PDF Format
  - Layer by Layer Results

# SIwave-DC Signal Flow Graph

## Fully Automated Report:

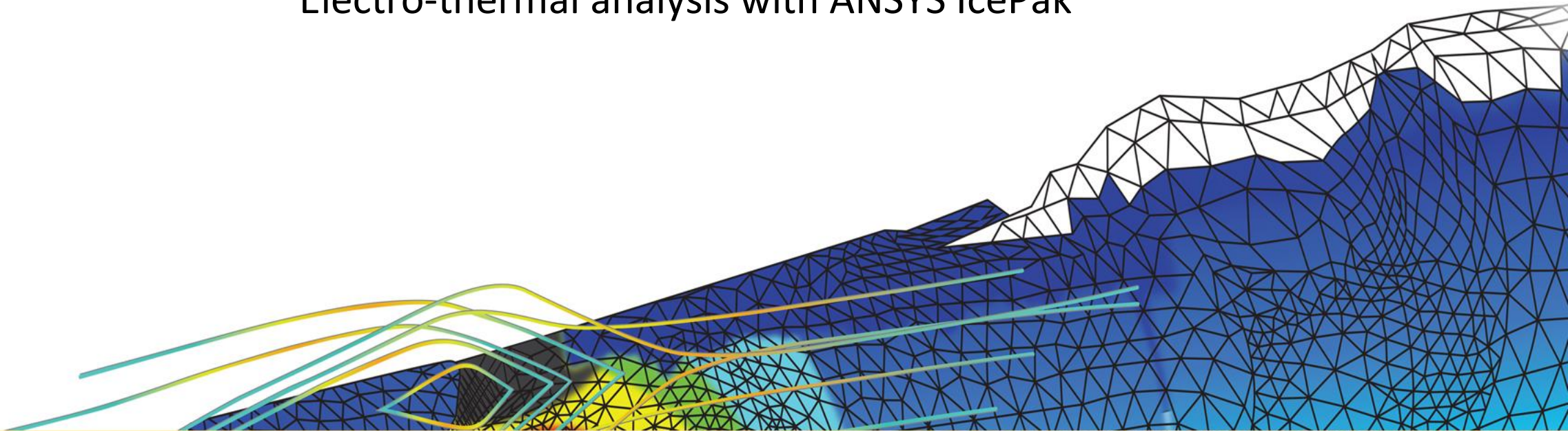
- Identify path IR drop as well as drop across lumped components along the power rail(s)
- Specify Pass/Fail criteria for current drawn/Voltage Drop across active devices





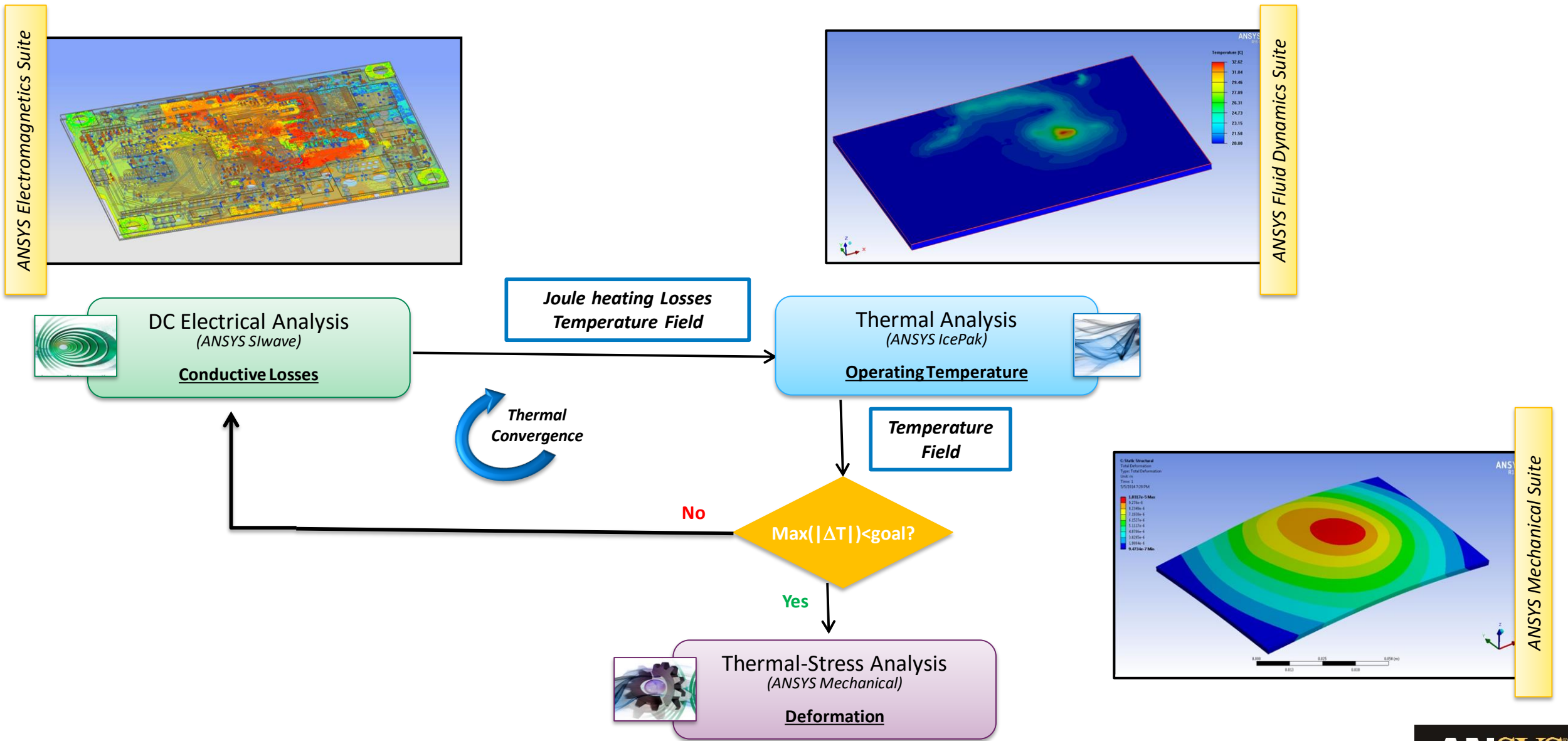
# Multiphysics Simulations

Electro-thermal analysis with ANSYS IcePak

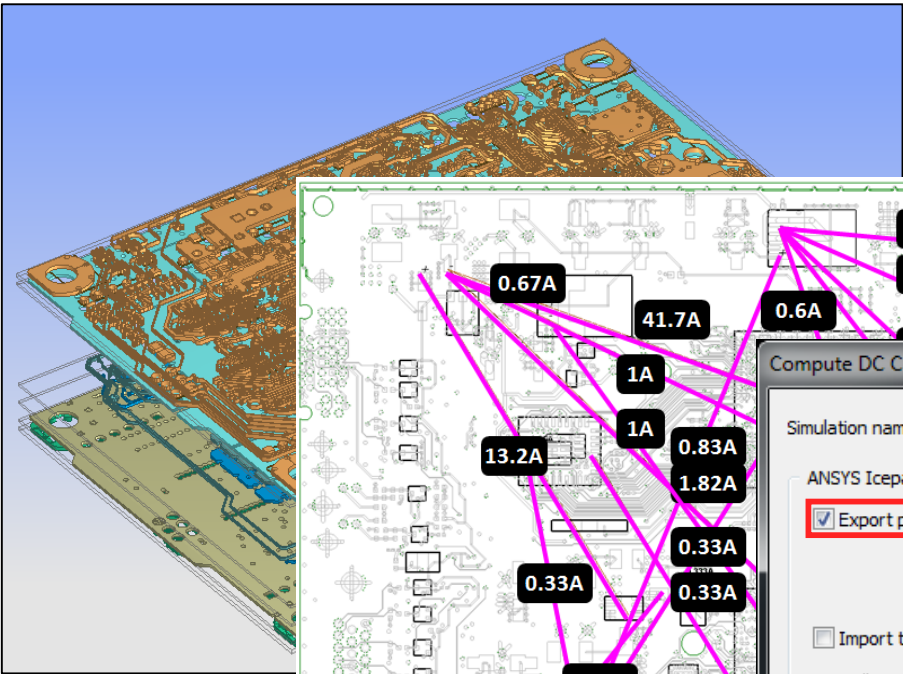




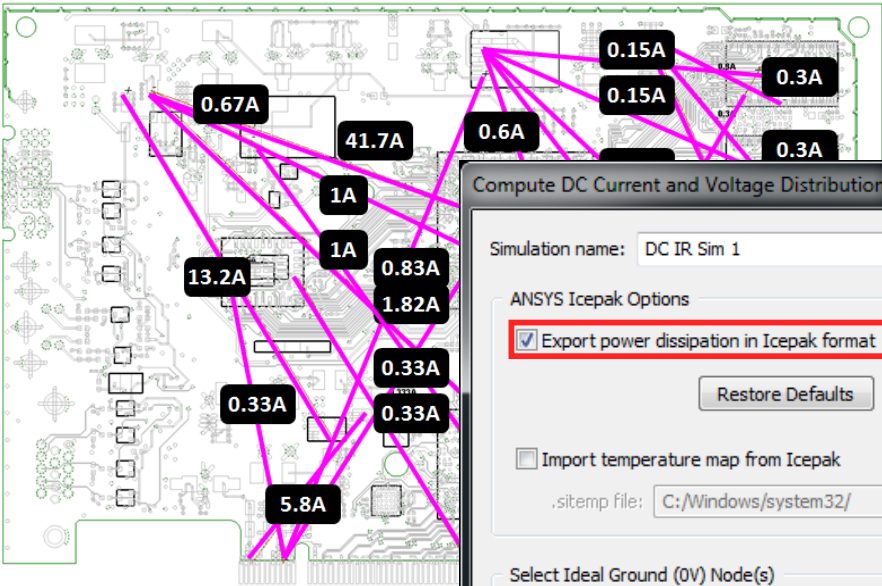
# Multi-Physics Solutions for PCBs



# Initial Setup in Slwave



Import Layout



Define Excitation

Compute DC Current and Voltage Distribution

Simulation name: DC IR Sim 1

ANSYS Icepak Options

- ☒ Export power dissipation in Icepak format
- ☐ Import temperature map from Icepak

Restore Defaults

Min. Thermal Cell Size: 3.27633 mm

Max. Thermal Cell Size: 9.82898 mm

Min. Power Loss Per Cell: 7.97376 milliwatts

.sitemp file: C:/Windows/system32/ Browse...

Select Ideal Ground (0V) Node(s)

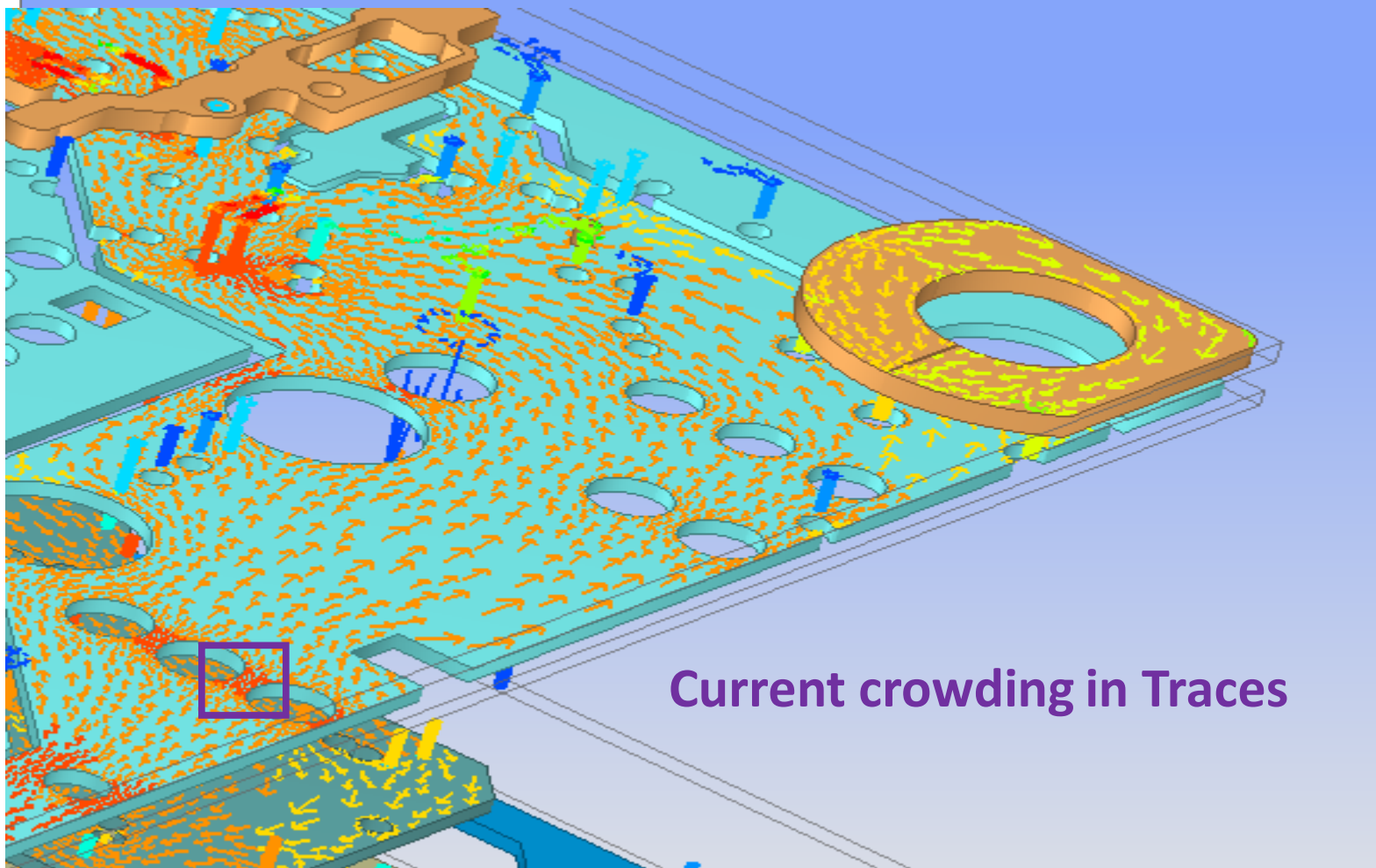
| Source Name               | Positive Node Net | Negative Node Net | Node to Ground |
|---------------------------|-------------------|-------------------|----------------|
| U2A5_AD24_V3P3_S0         | V3P3_S0           | GND               | Neither        |
| V3P3_S0_C76254-001_U3B... | V3P3_S0           | GND               | Neither        |
| V3P3_S0_G60296-001_U4B... | V3P3_S0           | GND               | Neither        |
| V3P3_S0_G83474-001_U2B... | V3P3_S0           | GND               | Neither        |
| V3P3_S0_G94441-001_U2M... | V3P3_S0           | GND               | Negative       |

Other solver options...

Save Settings Launch Close

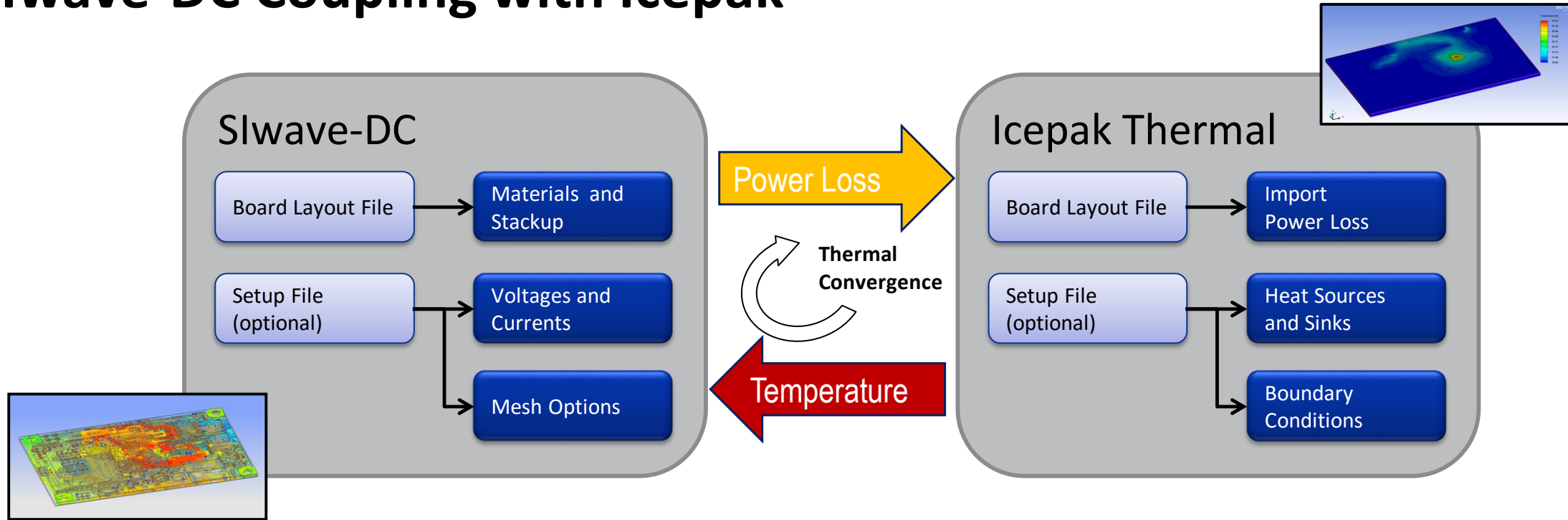
Solve

# SIwave results: Current Crowding in Traces



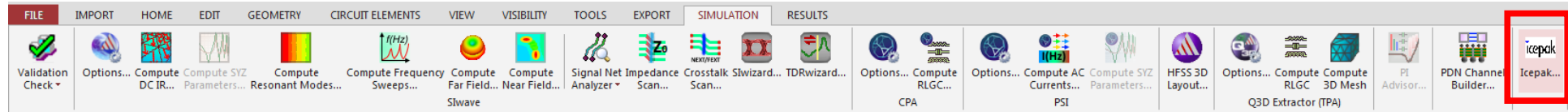


# SIwave-DC Coupling with Icepak

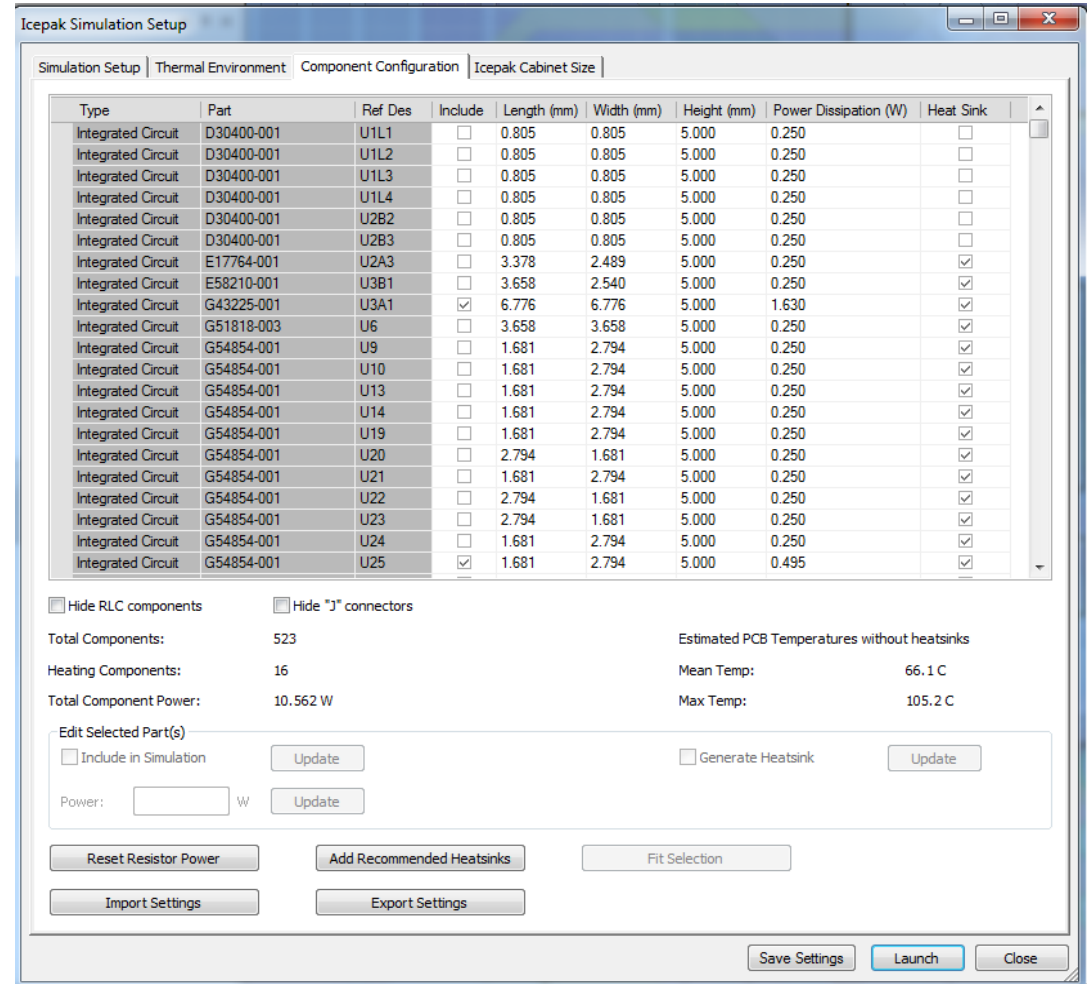


- **Spatial Power Loss** information from the DC-IR analysis (SIwave) is transferred to Icepak as a spatial Joule Heating map
- **Spatial Temperature** information from the Thermal analysis (Icepak) is transferred to SIwave and interpreted as spatial thermal modifiers for electrical conductivity

# Overview: Slwave with built-in Icepak



- In R17.1 Slwave users can now quickly and easily set up an Icepak simulation including:
  - Conduction only or Convection
  - Airflow inside enclosure
  - Component power dissipation
  - Enclosure size
- Simulation runs completely inside Slwave; no Icepak GUI interaction is required
- Allows electrical engineers to quickly estimate board temperatures



# Power Map from Siwave

Compute DC Current and Voltage Distribution

Simulation name: DC IR Sim 1

ANSYS Icepak Options

☒ Import temperature map from Icepak

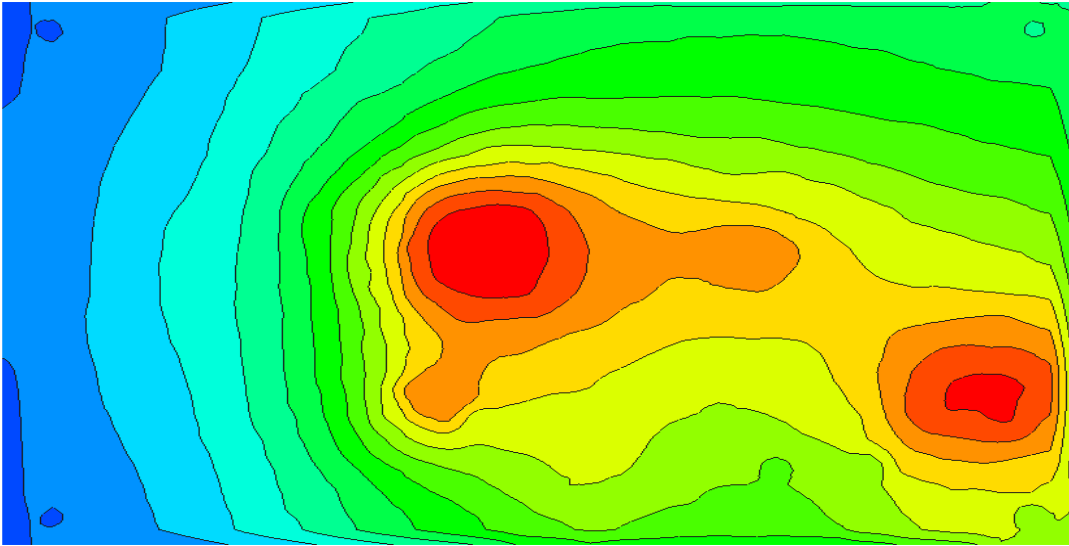
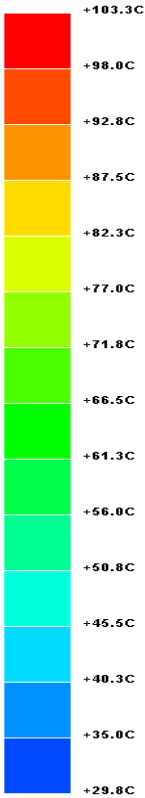
☐ Simulation Results:

☐ External .sitemp file: C:/Windows/system32/ Browse...

Select Ideal Ground (0V) Node(s)

| Source Name               | Positive Node Net | Negative Node Net | Node to Ground |
|---------------------------|-------------------|-------------------|----------------|
| U2A5_AB24_V3P3_S0         | V3P3_S0           | GND               | Neither        |
| U2A5_AD24_V3P3_S0         | V3P3_S0           | GND               | Neither        |
| V3P3_S0_C76254-001_U3B... | V3P3_S0           | GND               | Neither        |
| V3P3_S0_G60296-001_U4B... | V3P3_S0           | GND               | Neither        |
| V3P3_S0_G83474-001_U2B... | V3P3_S0           | GND               | Neither        |
| V3P3_S0_G94441-001_U2M... | V3P3_S0           | GND               | Negative       |

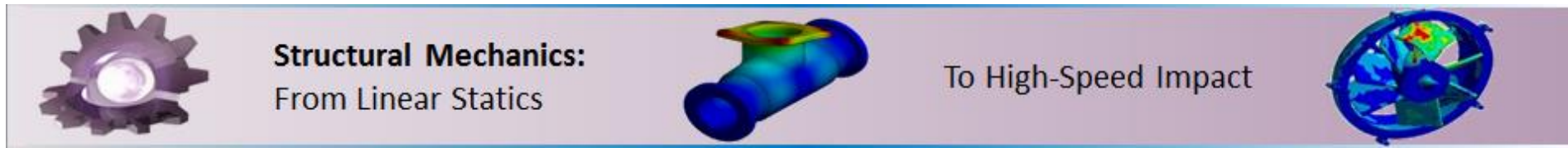
Other solver options... Save Settings Launch Close



Temperature from Icepak



# What is ANSYS Mechanical?



- **Structural (static and transient)**

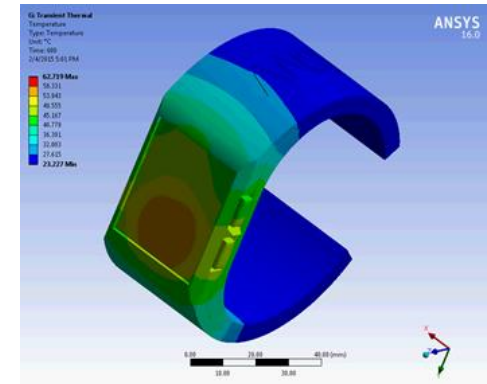
- *Linear and nonlinear structural analyses*

- **Dynamics**

- *Modal, harmonic, response spectrum, random vibration, flexible and rigid dynamics*

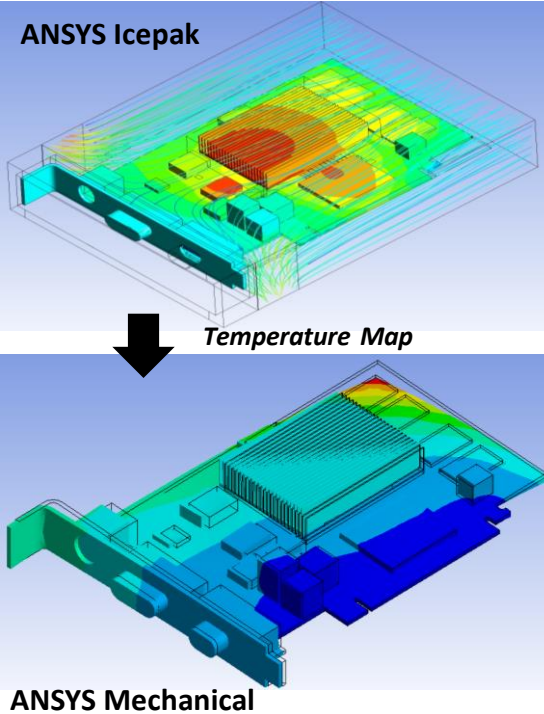
- **Heat Transfer (steady state and transient)**

- *Solve for temperature field and heat flux inclusive of Temperature dependent materials*

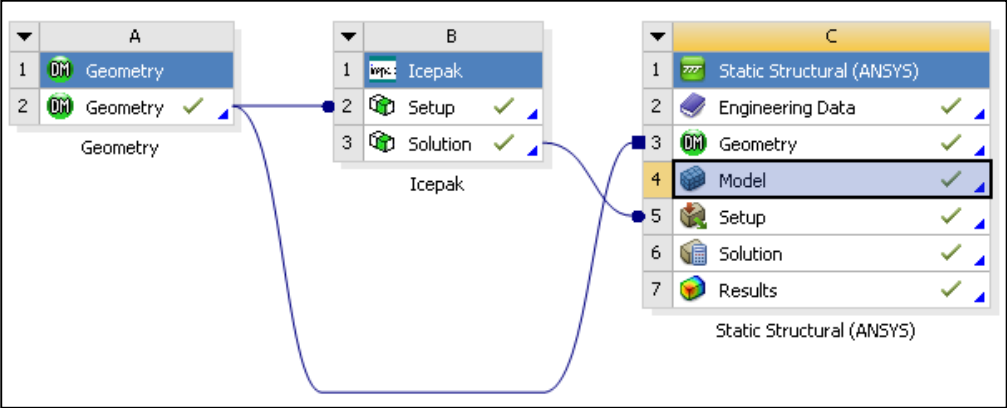


# ANSYS Icepak coupling with ANSYS Mechanical

- The distribution of copper in PCB trace layouts can affect the thermo-mechanical response
- Criteria common for PCB's are thermally induced stresses and displacements

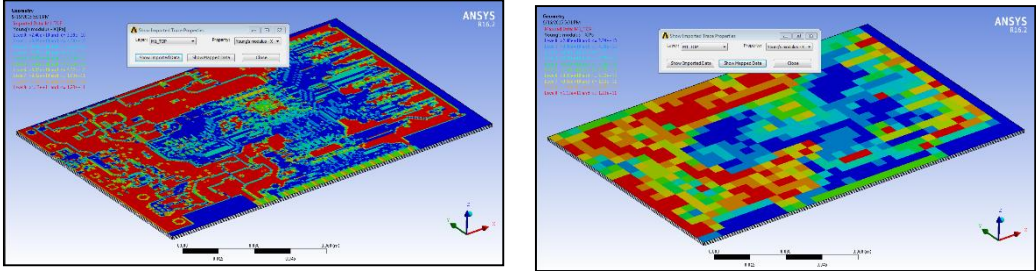


Thermal-stress simulation for a computer graphics card performed in ANSYS Workbench

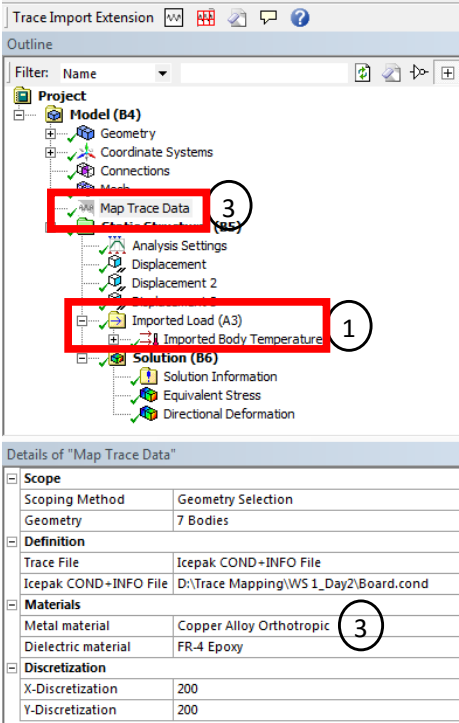


ANSYS Workbench Setup

- Necessary structural boundary conditions can be added here



View the plots per layer



# ANSYS Mechanical: Deformation Results

- Displacement profile

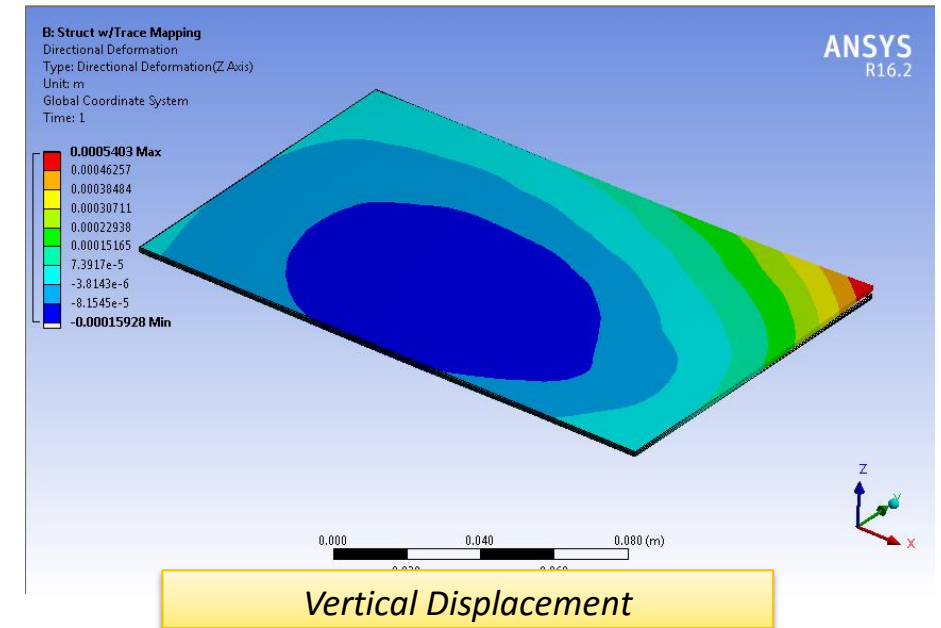
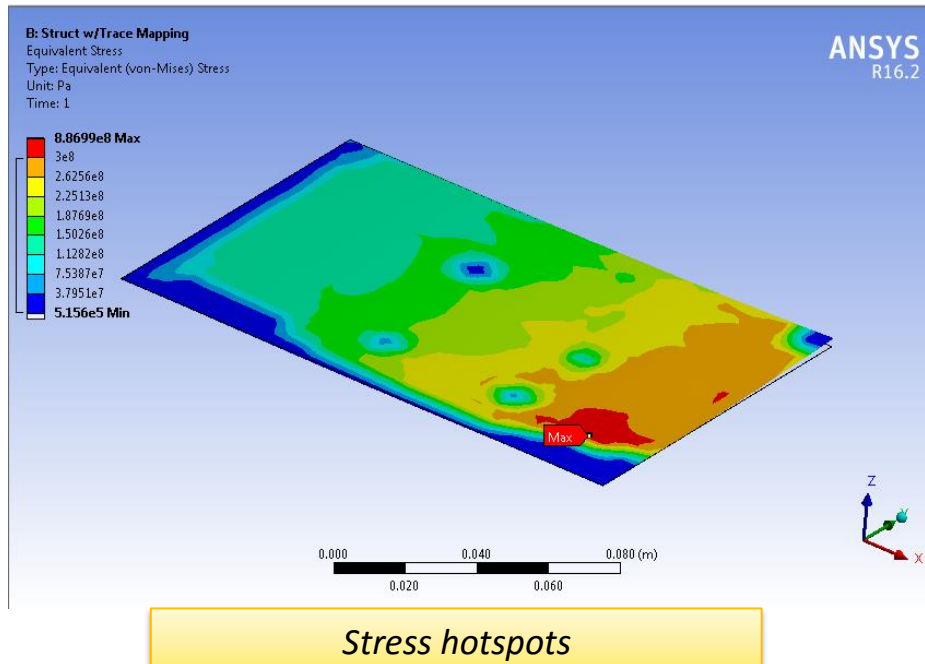
- Bow downward at center and upward deflection of corner

- Stress profile

- With trace mapping, it is possible to view distribution of stress in each layer

- The layer and location of peak stress can be identified

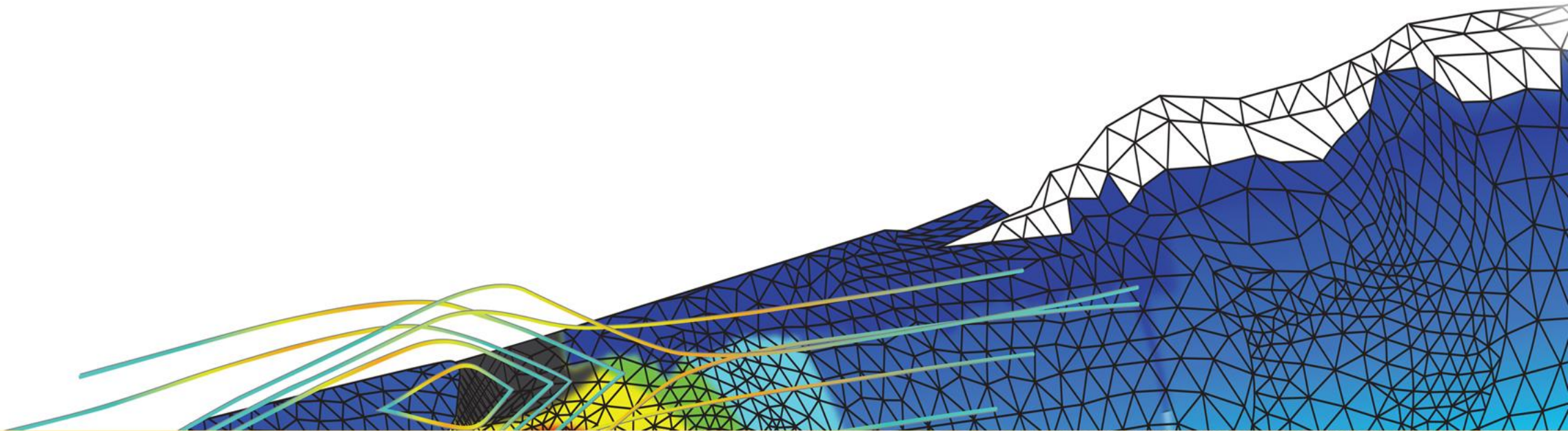
- These differences in stress distributions can lead to differences in random vibration response







# Power Integrity Simulation

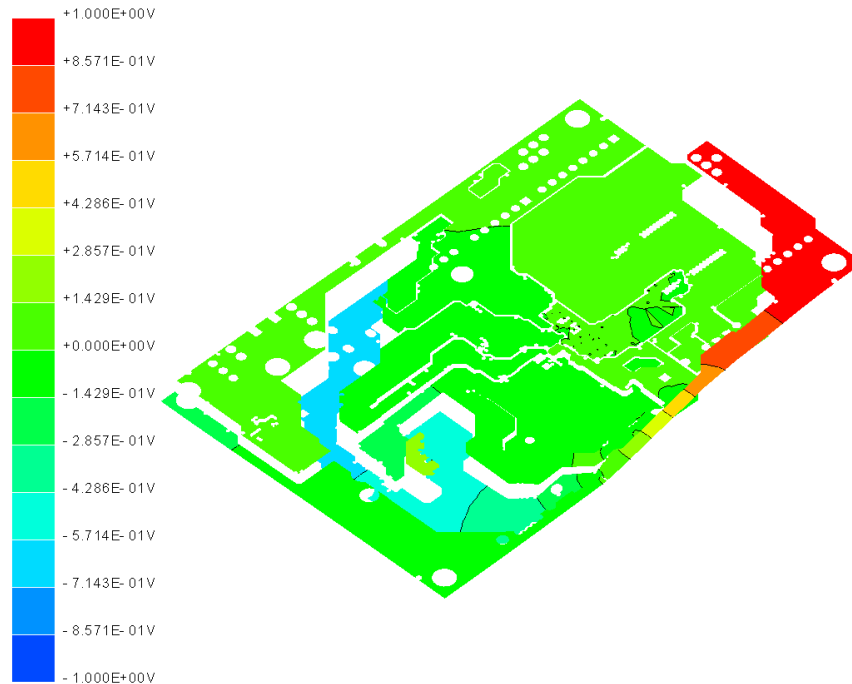


# SIwave-PI Overview

SIwave-PI includes everything from SIwave-DC plus simulation types for high-frequency power integrity analysis:

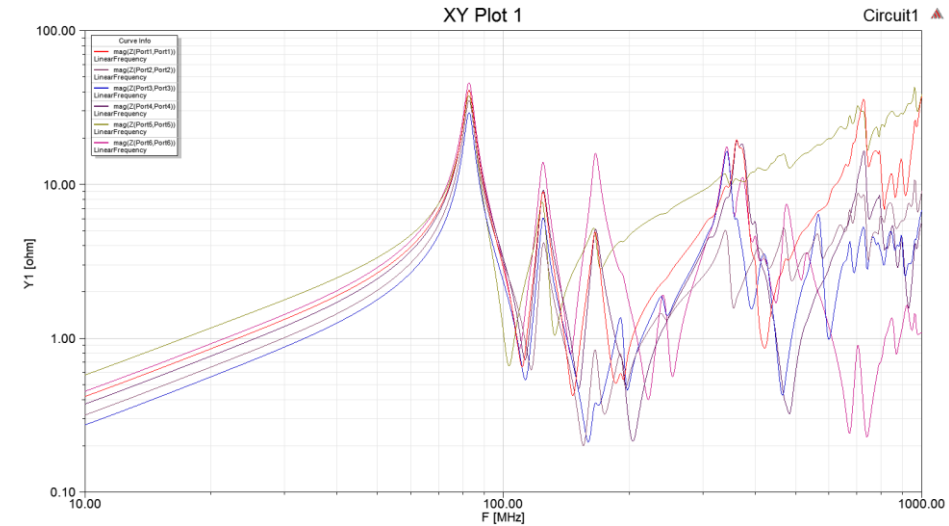
- SYZ-Parameter Extraction
- Plane Resonance Analysis
- AC Frequency Sweep Solver
- PI Advisor Decoupling Capacitor Optimization

## Resonant Modes



## Capacitor Optimization

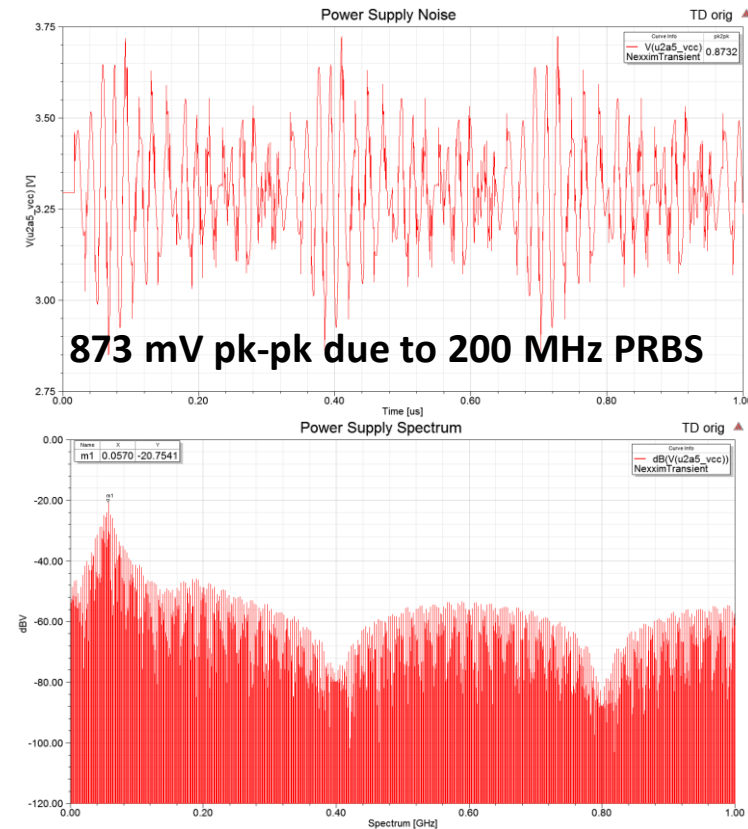
## Z-Parameters



## AC Surface Voltages

## Power Delivery Network

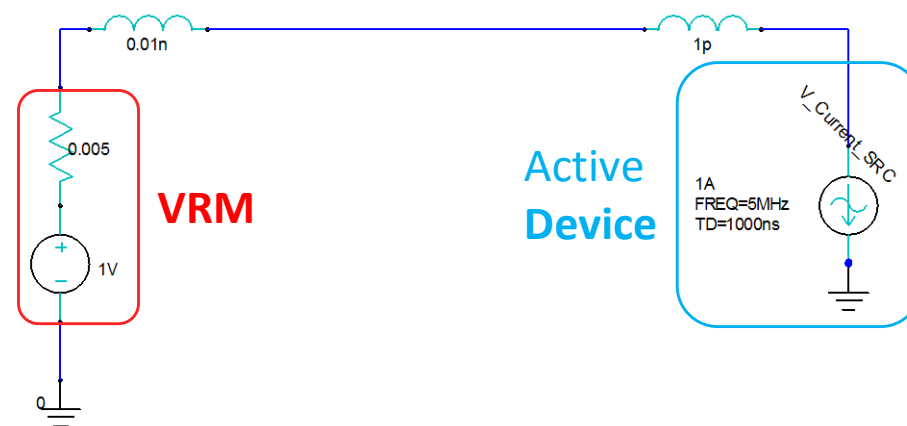
- Designs of today operate in conjunction with a number of clocks, oscillators, power supplies, and signaling standards. Supplying sufficient power means designing a Power Delivery Network capable of handling any perturbations or irregularities that these complex systems demand.
- The example below shows voltage for both the time and frequency domain simulation results of a memory interface. A good design will minimize the voltage ripple to ensure that all active devices have a stable and reliable voltage reference. Excessive perturbations in power could cause adverse affects to input and output margins or even couple to other power rails.





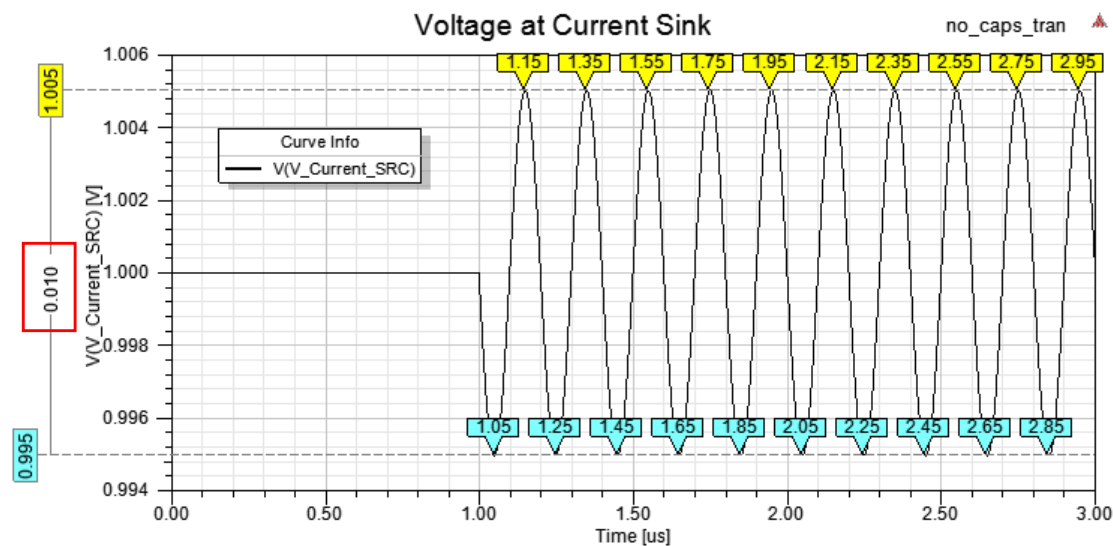
## VRM Transient Simulation Setup

- Voltage Regulator Module (VRM) is modeled with a series source resistance of  $5\text{m}\Omega$  for this example.
- Active Device is modeled as a Current Sink
  - 1A Amplitude:  $I_{pk-pk} = 2\text{A}$
  - Frequency = 5 MHz
  - Time Delay =  $1\mu\text{s}$



## Example

- $V_{ripple} = I(5\text{MHz}) * Z(5\text{MHz})$
- $V_{ripple} = 5\text{mV} = 10\text{mV}_{pk-pk}$

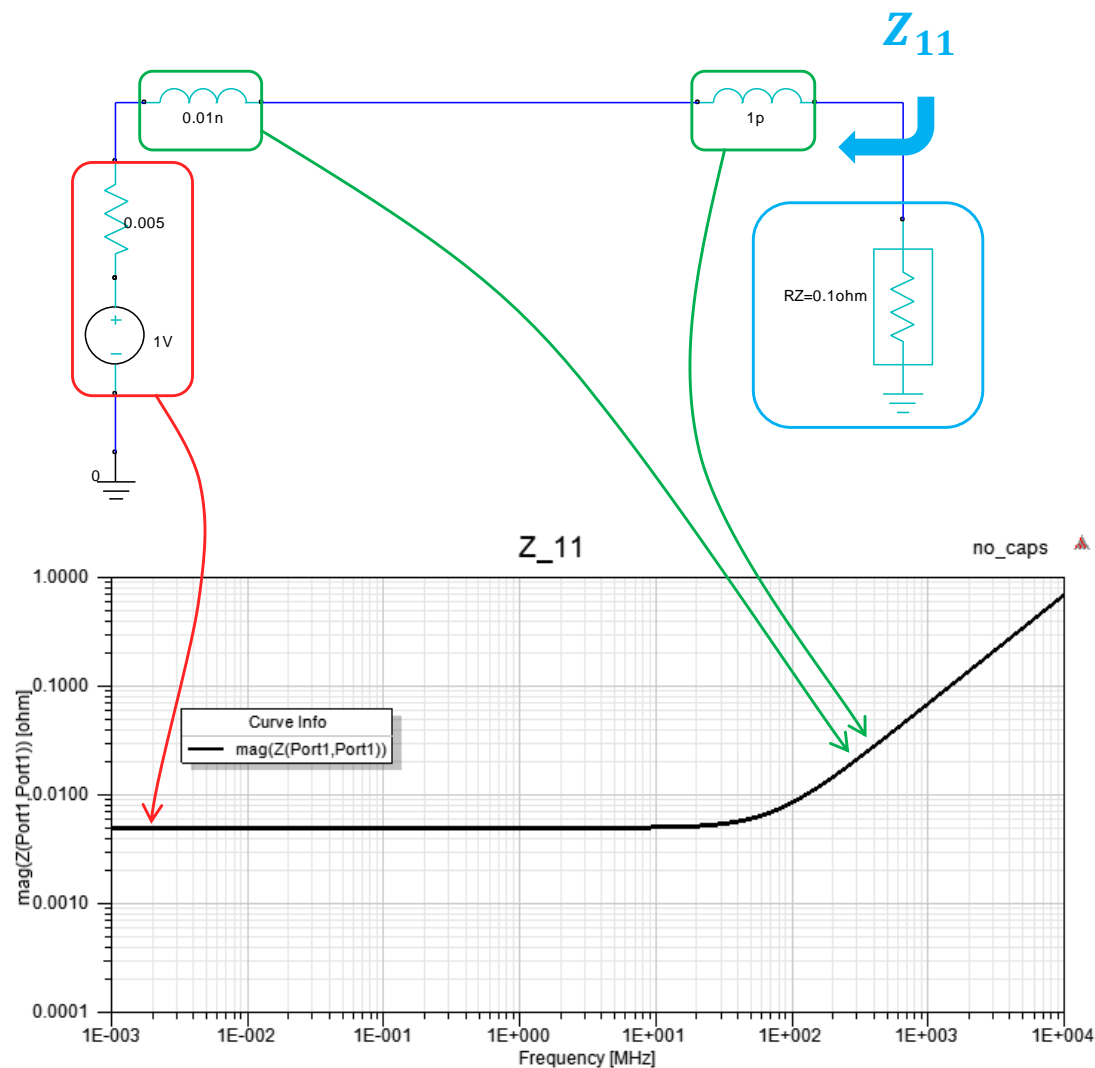


## VRM Frequency Domain Response

- At DC,  $|Z_{11}| = 5m\Omega$  which is the VRM series resistance.
- At  $f \rightarrow \infty$ ,  $|Z_{11}| \rightarrow \infty$  due to the path loop inductance. In this case, a total of 11pH.

## Example

- $V_{ripple} = I(5\text{ MHz}) * Z(5\text{ MHz})$
- $V_{ripple} = 1A * 5m\Omega$
- $V_{ripple} = 5mV = 10mV_{pk-pk}$

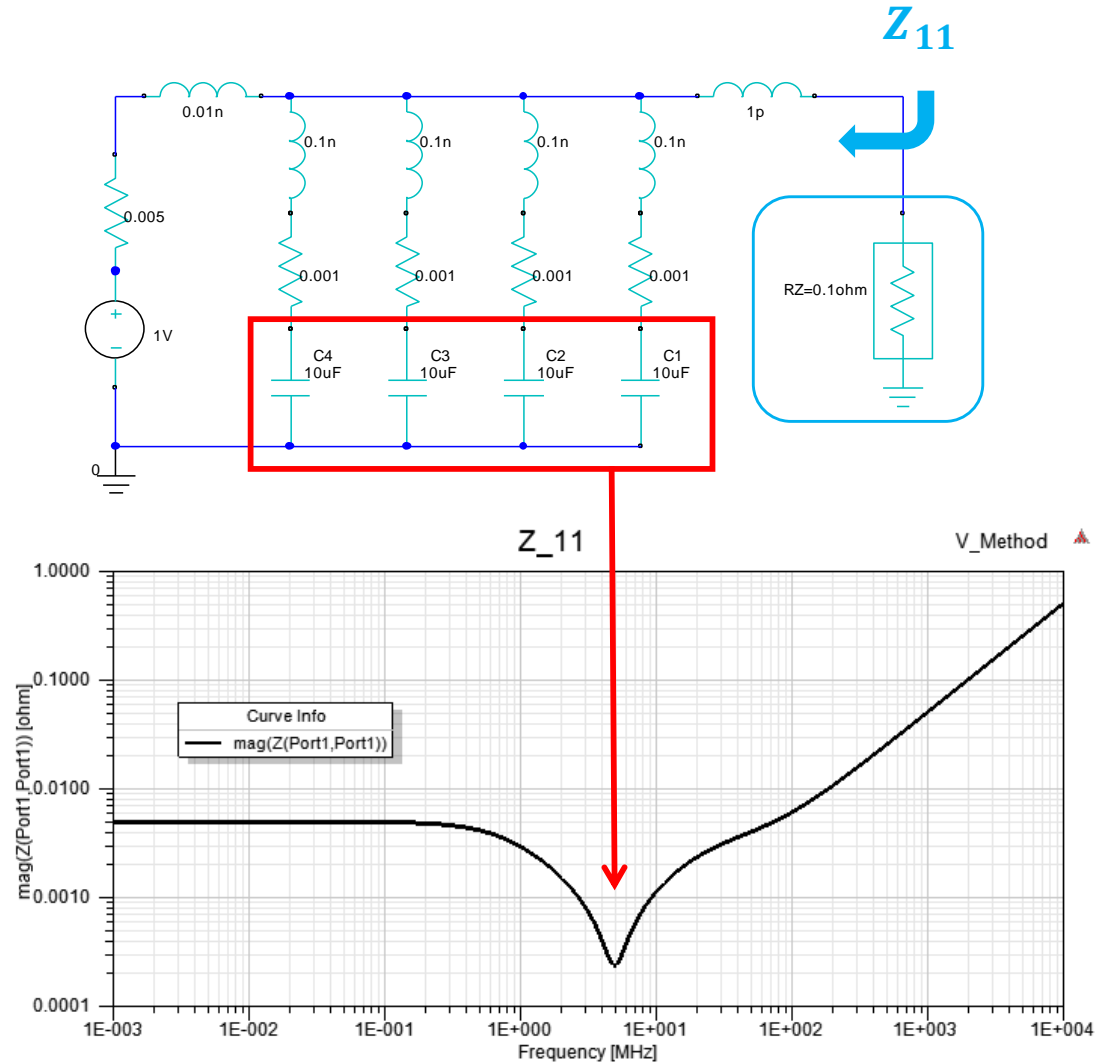


### V Method

- All capacitor values are chosen to be the same in order to lower the impedance magnitude at a specific frequency. The resultant impedance plot resembles a V shape.
- In this example, if a device requires 1A at 5MHz, it will see  $|Z_{11}| = 0.24\text{m}\Omega$ .
- $f_{\text{resonance}} = \frac{1}{2\pi\sqrt{LC}}$
- $f_{\text{resonance}} = \frac{1}{2\pi\sqrt{(0.1\text{nH}+1\text{pH})*10\mu\text{F}}}$
- $f_{\text{resonance}} = 5.01\text{MHz}$

### Example

- $V_{\text{ripple}} = I (5 \text{ MHz}) * Z (5 \text{ MHz})$
- $V_{\text{ripple}} = 1\text{A} * 0.24\text{m}\Omega$
- $V_{\text{ripple}} = 0.24\text{mV} = 0.48\text{mV}_{\text{pk-pk}}$



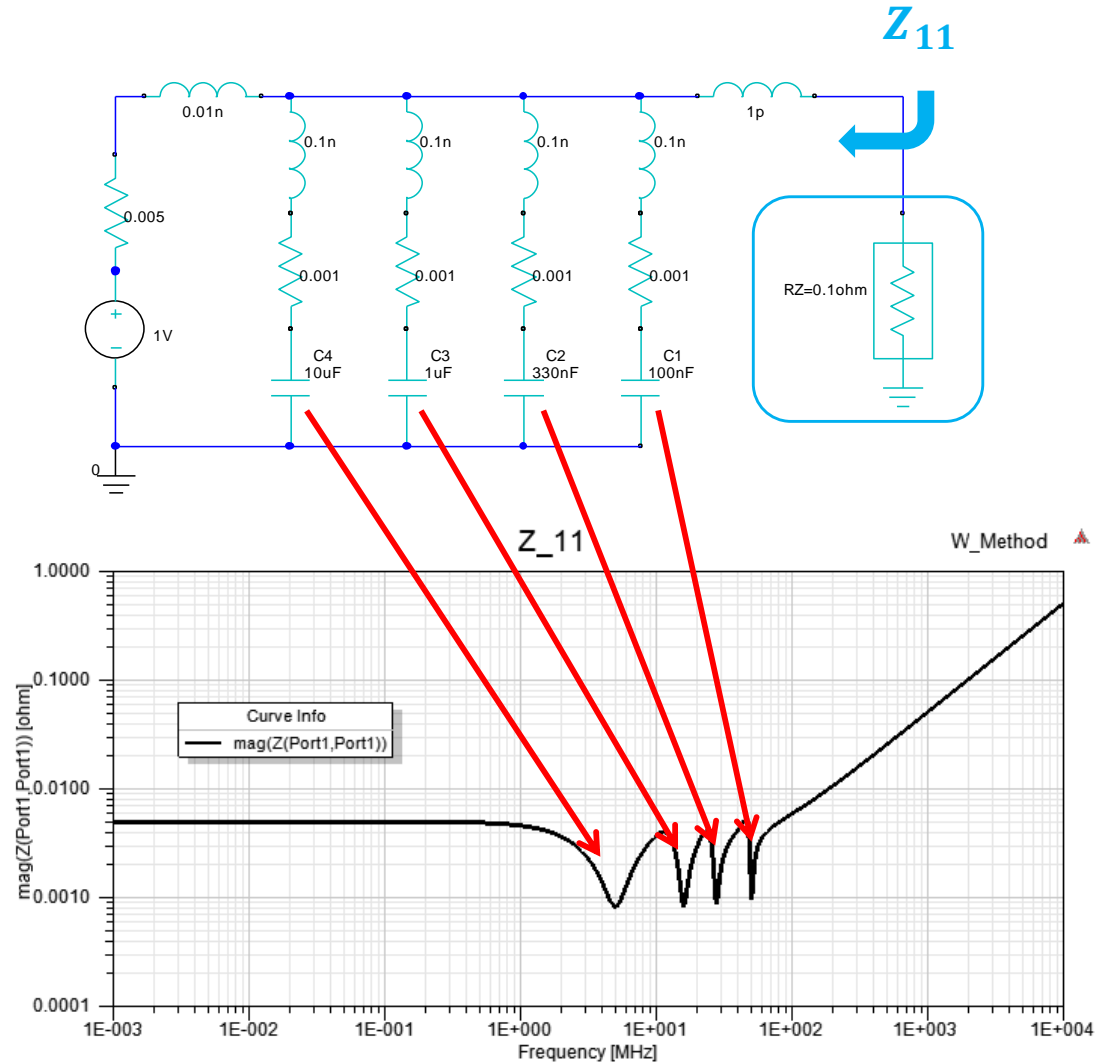


## W Method

- Choose different capacitor values to be more effective across a broad range of frequencies. The resultant impedance plot resembles a W shape.
- $f_{res,C4} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{101pH*10\mu F}} = 5.01 \text{ MHz}$
- $f_{res,C3} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{101pH*1\mu F}} = 15.8 \text{ MHz}$
- $f_{res,C2} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{101pH*330nF}} = 27.6 \text{ MHz}$
- $f_{res,C1} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{101pH*10nF}} = 158 \text{ MHz}$

## Example

- $V_{ripple} = I(5 \text{ MHz}) * Z(5 \text{ MHz})$
- $V_{ripple} = 1A * 0.832m\Omega$
- $V_{ripple} = 0.832mV = 1.664mV_{pk-pk}$



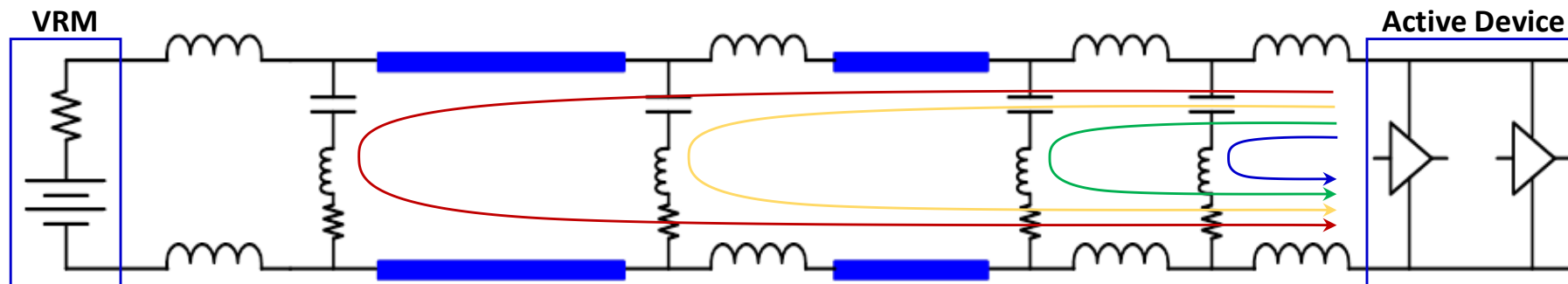
## Circuit Simulation vs. Electromagnetic Field Solvers

- Real, physical designs have many more inductive loops, capacitive planes, and resistive paths which were not depicted in the previous example circuit. In order to account for all of the effects of physical layout and geometry complexities, a field solver such as SIwave, Sentinel-PSI, or HFSS must be used.
- In any of the methods shown, loop inductance plays a vital role in determining the frequency of effectiveness. The L-C combination dictates the resonant frequency of adding or changing a capacitor value at a specific location.

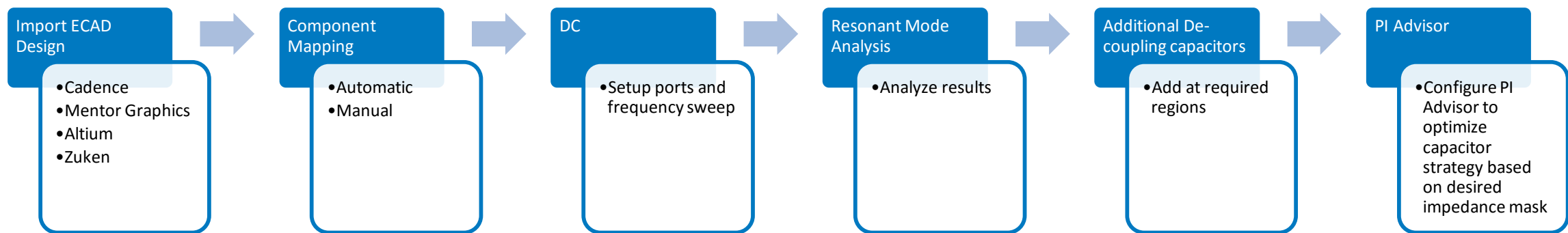
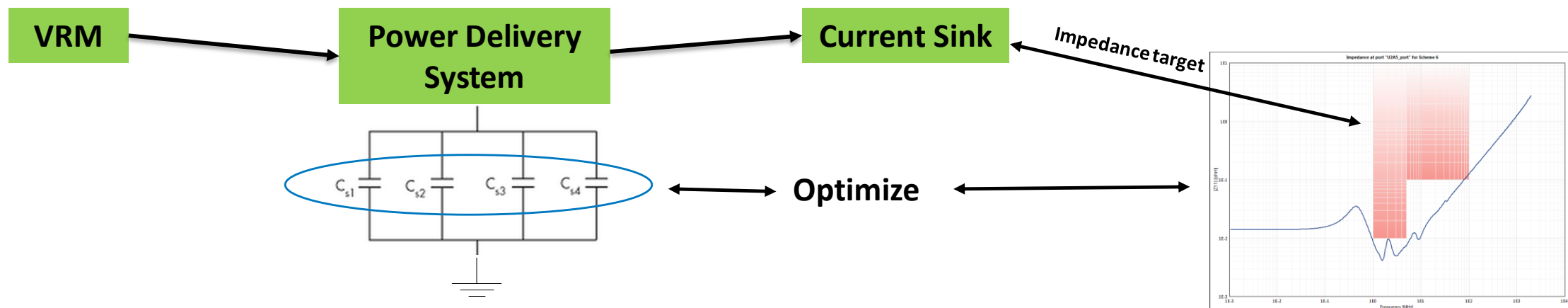
$$f_{resonance} = \frac{1}{2\pi\sqrt{LC}}$$

- Equivalent Series Resistance (ESR) and conductor path resistance affects the quality factor (Q) of the placed component.

$$Q = \frac{\left| \frac{1}{2\pi f C} \right|}{ESR}$$



# Capacitor Optimization Simulation Flow





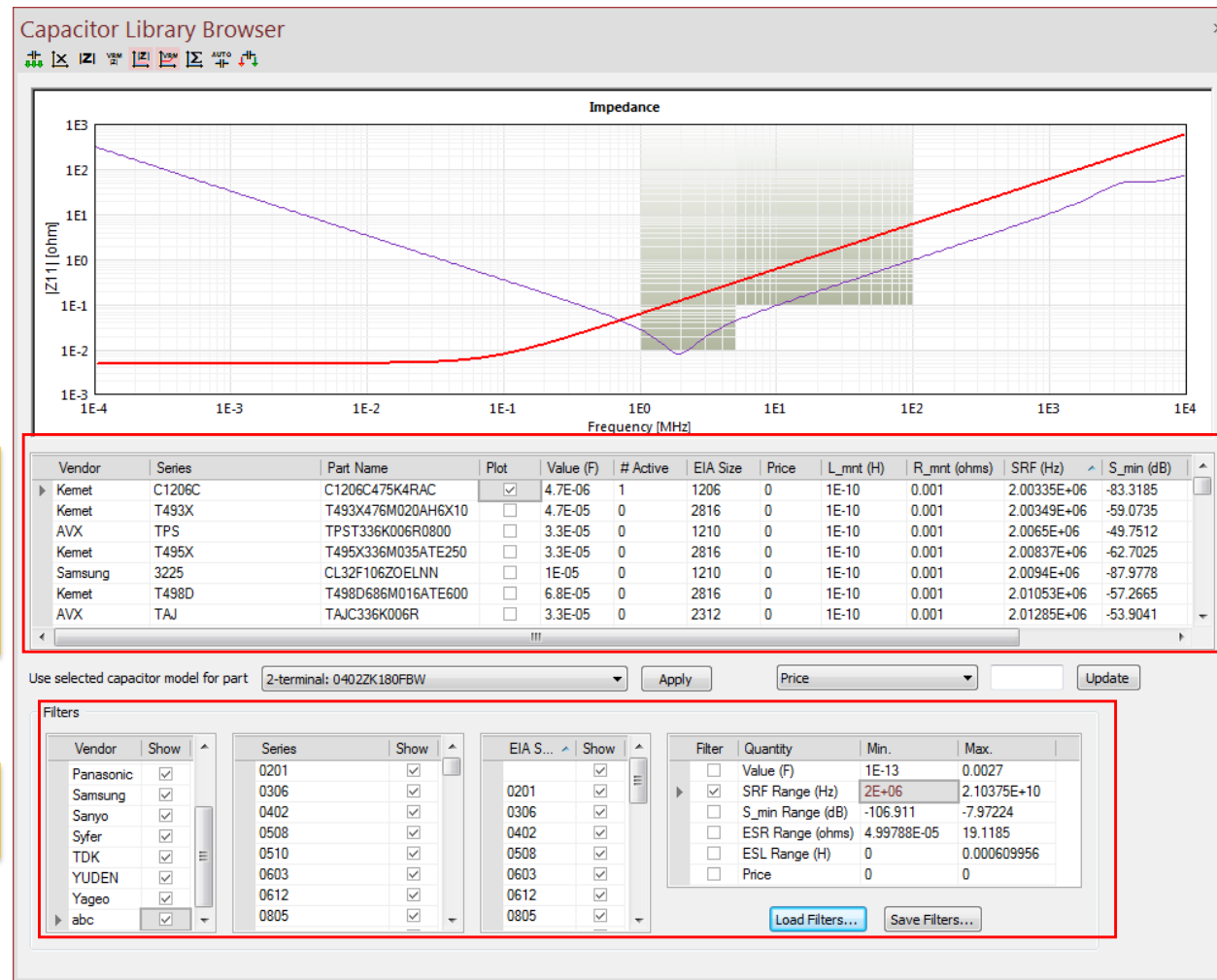
## Vendor Components support

- Siwave provides **20,000+ vendor supplied 2-port S-parameters for R, L and C's**
- You can also attach an imported N-port S-parameter model or Spice model onto specific components
- **Capacitor Library Browser** can be used to filter the custom and vendor components

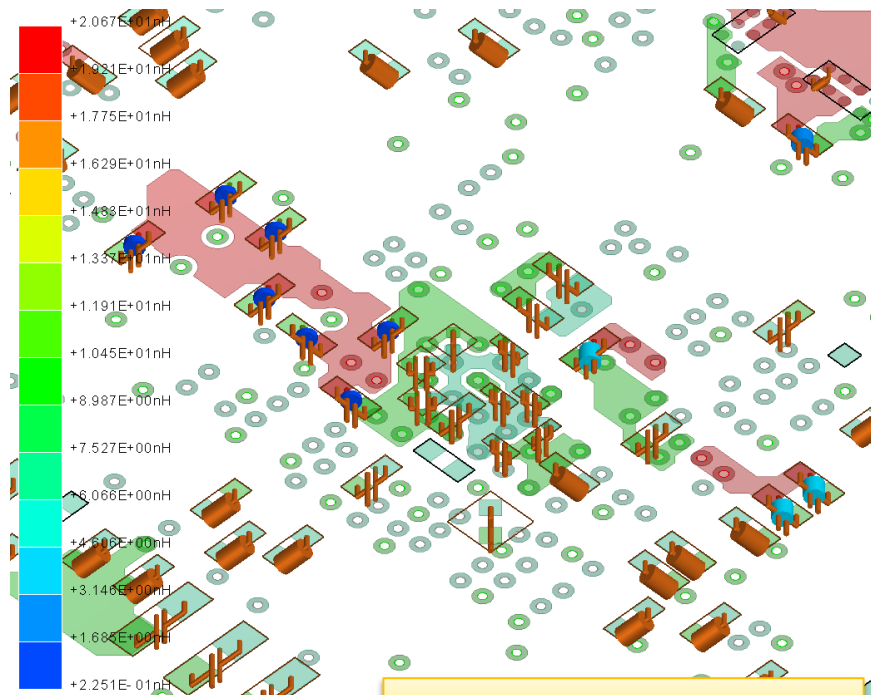
Choose to plot Z11 of selected component  
From the impedance mask you can

1. Estimate capacitor type
2. Number of capacitors to use to meet impedance spec

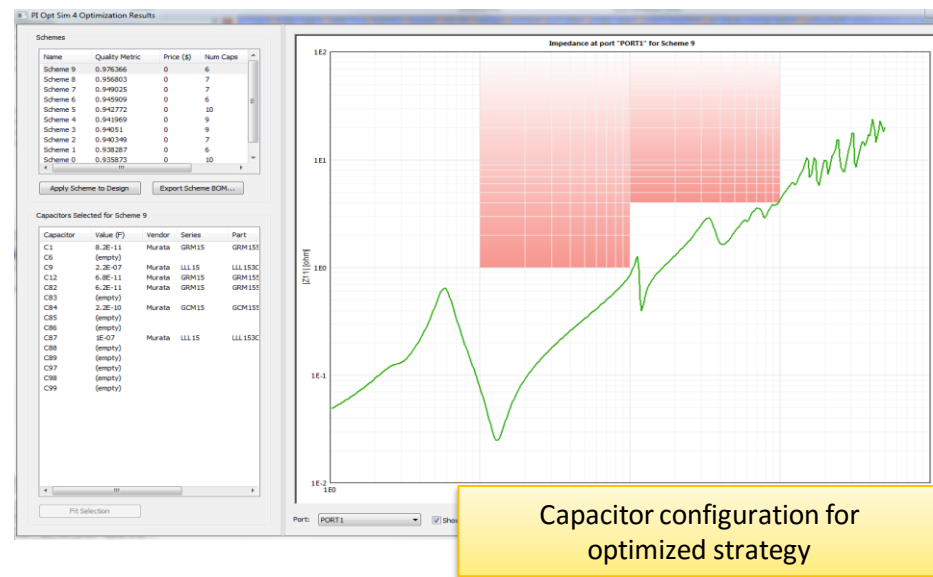
Filter Components based on desired specifications



- PI Advisor is an in-built tool that automatically **optimizes De-coupling Capacitor Strategy** for packages and boards.
- Quick calculation for determining optimal capacitor values
- Optimization based on given impedance mask
- Genetic algorithm handles vast solution space: 10s/100s of capacitors with 100s/1000s of candidates each
- View selected Capacitor Schemes against the defined profile.
- Loop Inductance from an Active Device location to each associated Capacitor location.



Capacitor Loop inductance



Capacitor configuration for optimized strategy

