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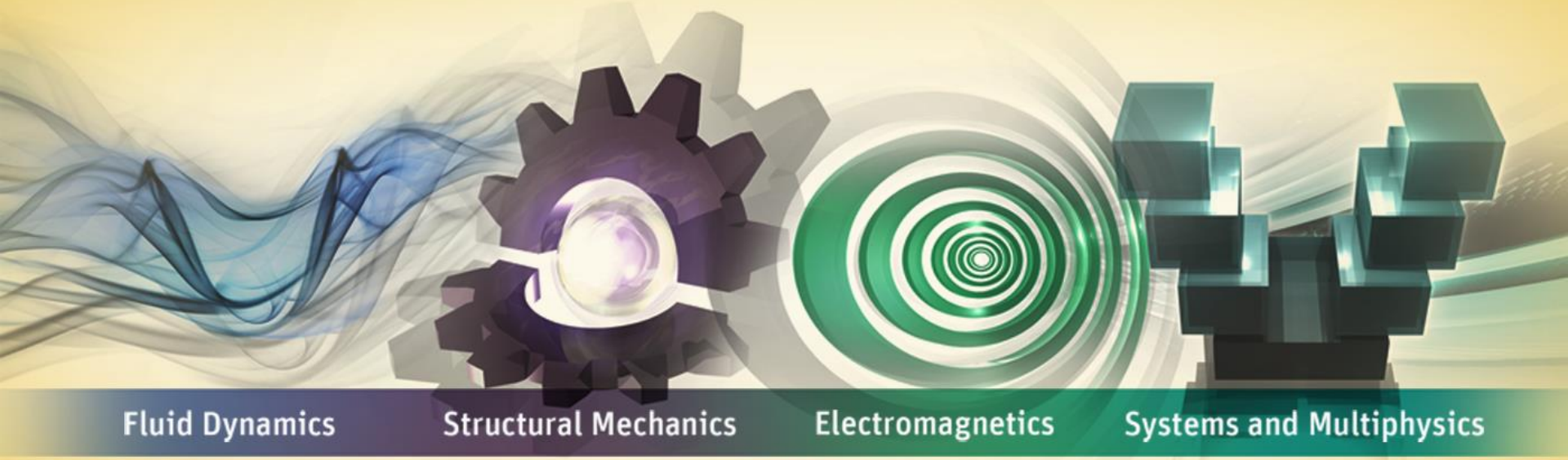
Design Flow Methodologies for High-Speed Printed Circuit Board



Agenda

- Introduction
- Simulation Requirements
- ANSYS Solution
- Example
- Conclusion

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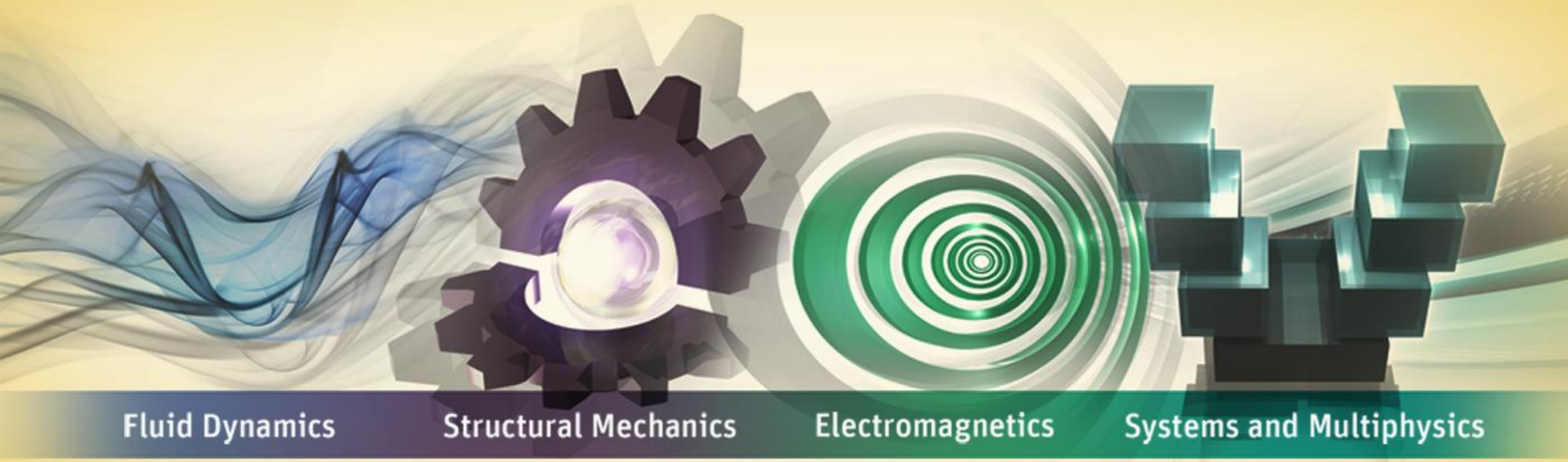
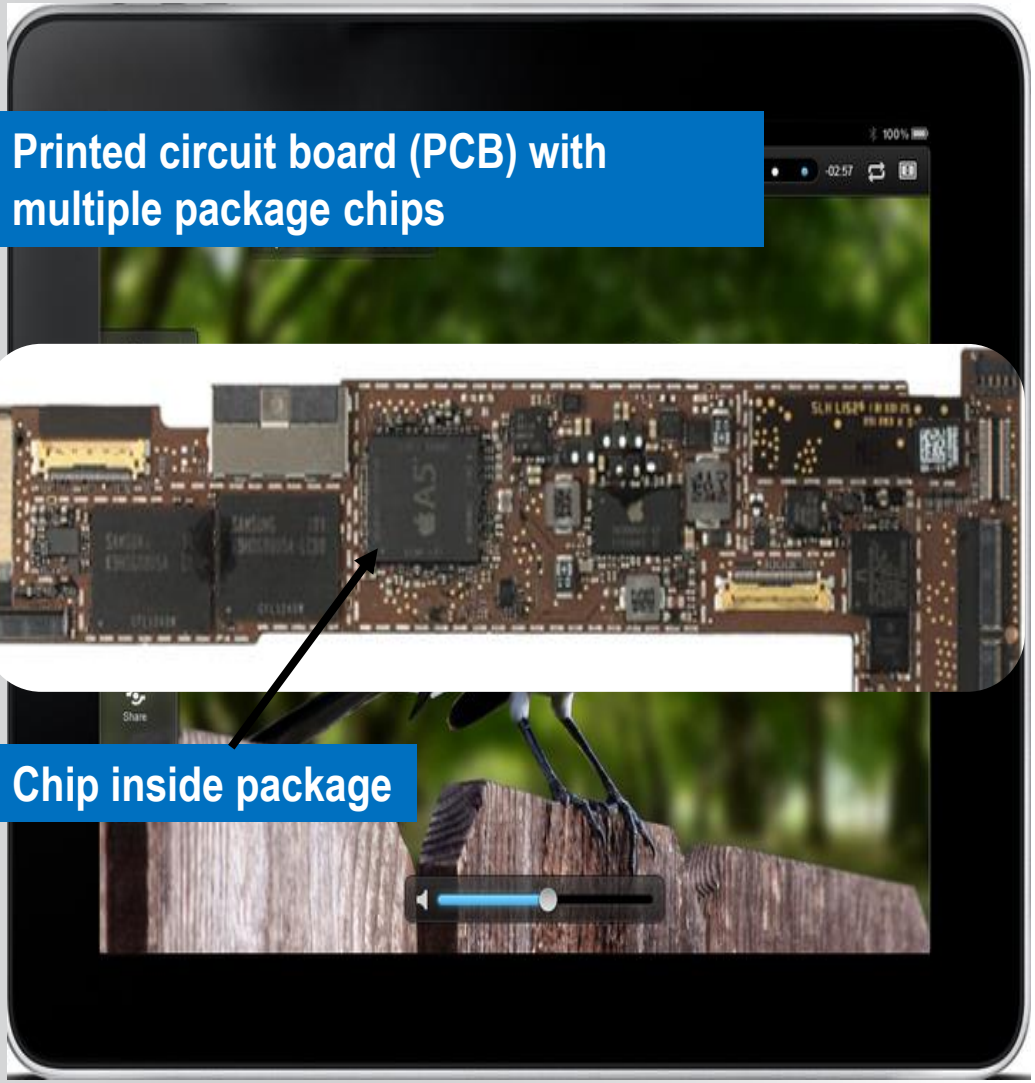
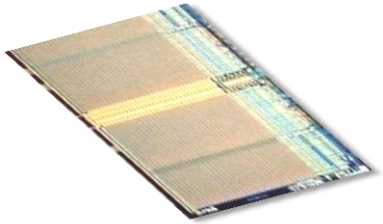
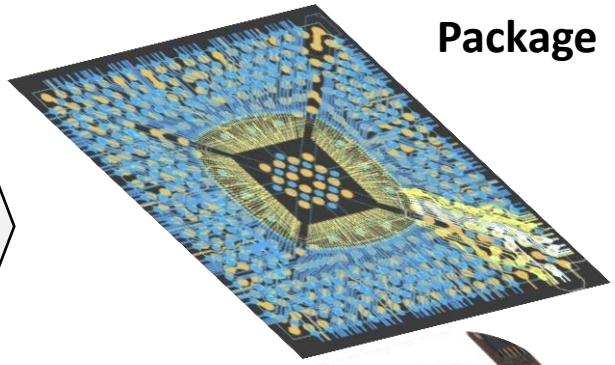
Introduction

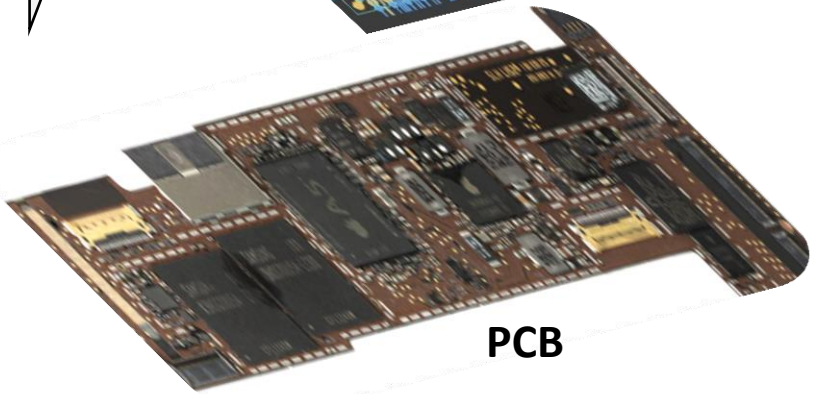


Components in Electronics Systems

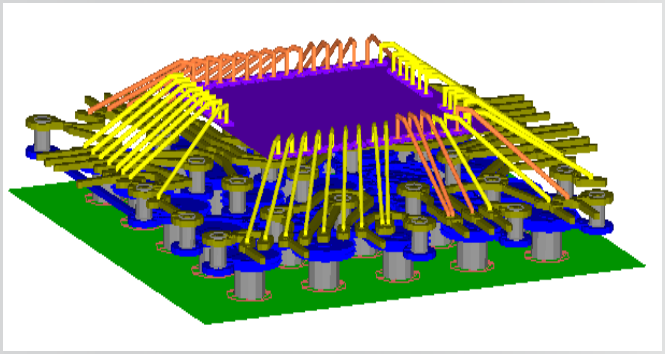


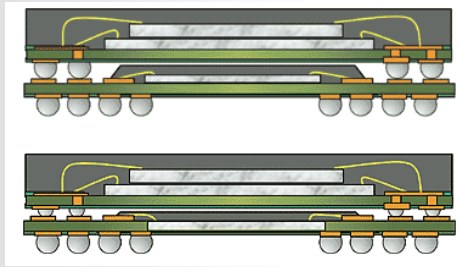


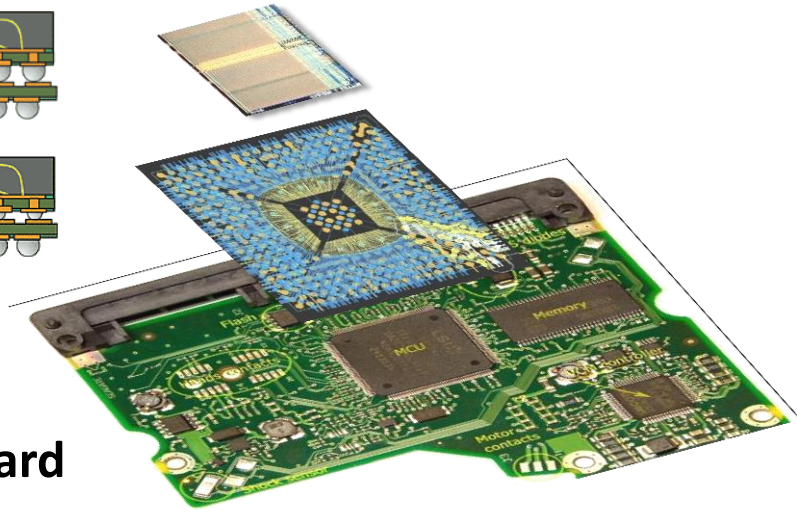




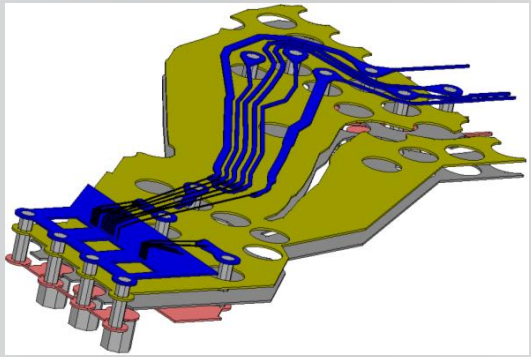
Applications

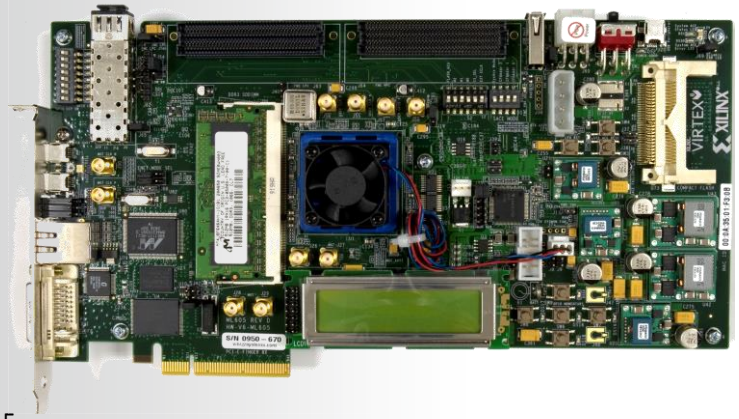




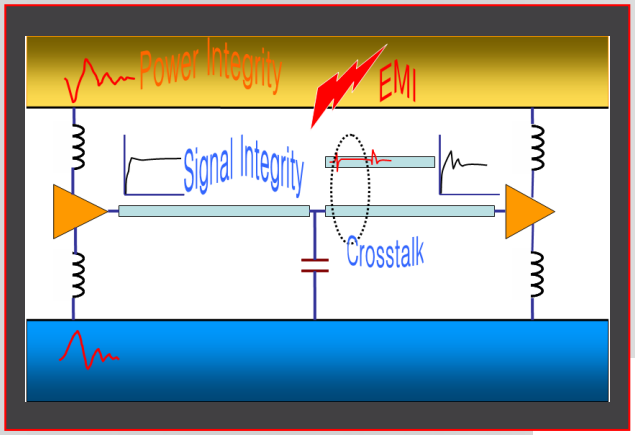


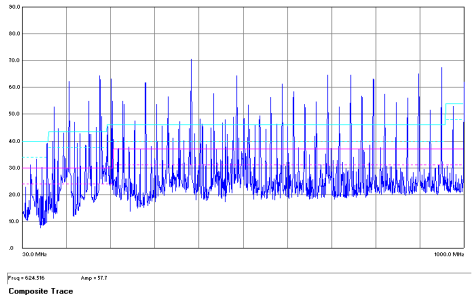
- Package
- High Speed board
- DDR3
- PCI-E
- …





High Speed Digital Design Issues





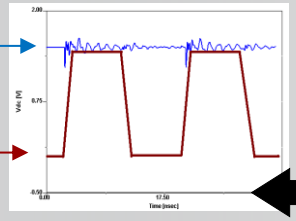
EMI/EMC
- Common mode radiation
- Differential mode radiation

Display Panel

Driver IC

Pwr Noise

Signal



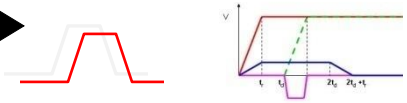
Control IC

Memory

PCB

Power Supplies

Power Integrity
- Switching Noise (SSO/SSN)
- Impedance Profile
- Power/Gnd Plane Resonance
- Return Path discontinuities

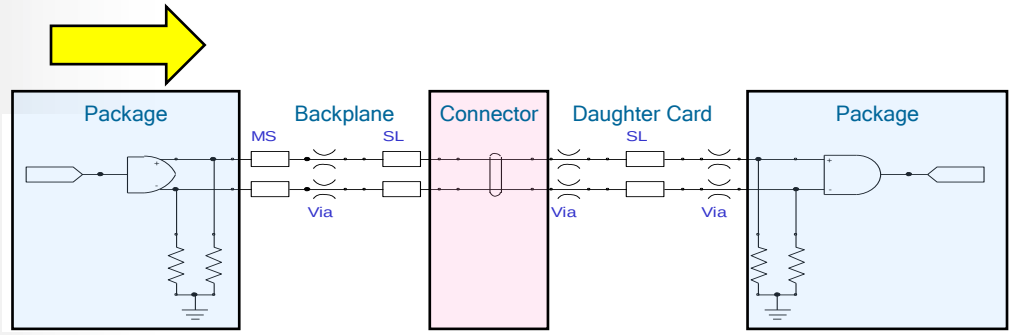


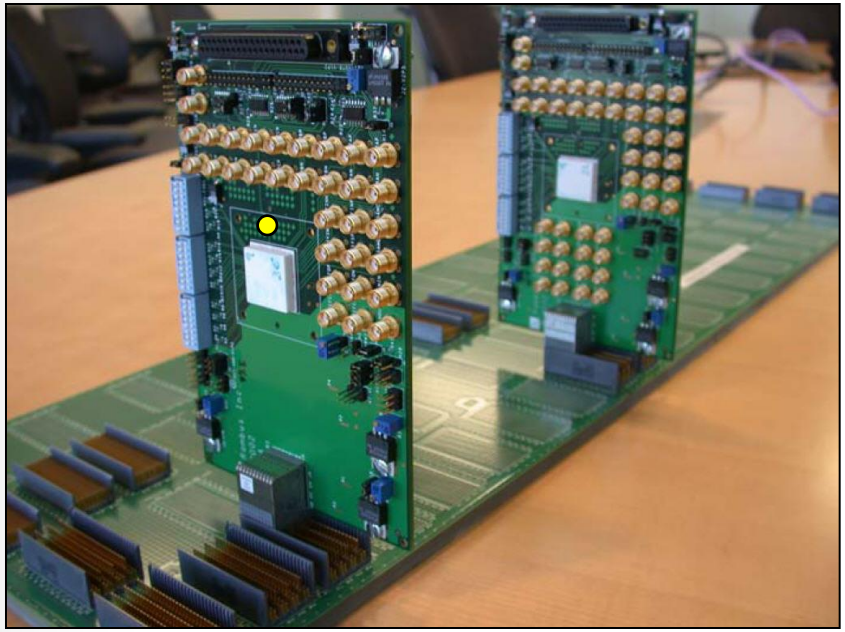
Signal Integrity
- Impedance
- Crosstalk
- Reflection
- Termination
- Dielectric Losses

Trends Requiring Chip Aware System Design

The die-to-die system is extremely complex:

- Silicon driver/receiver
- 3D component interconnect
- Chip to package
- Package to daughter card
- Daughter card to backplane
- Power delivery network effects





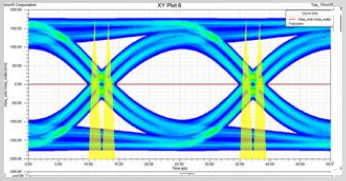
Complex problems

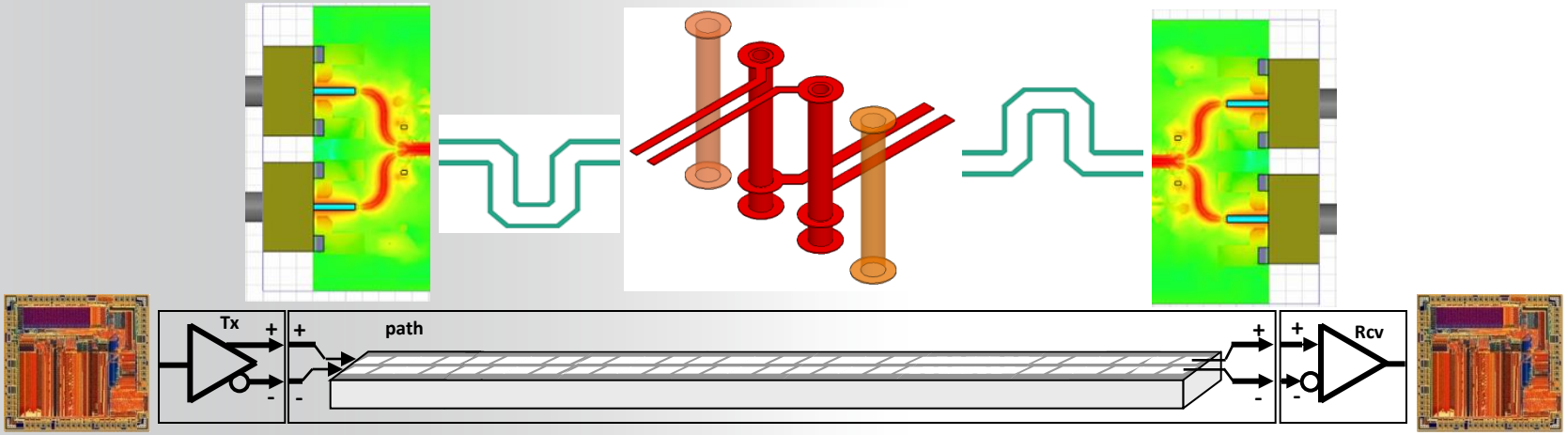
- High risk
  - New unfamiliar phenomena?
- High cost of design errors

Solving them is requiring new strategies and simulation tools.

Channel Discontinuities

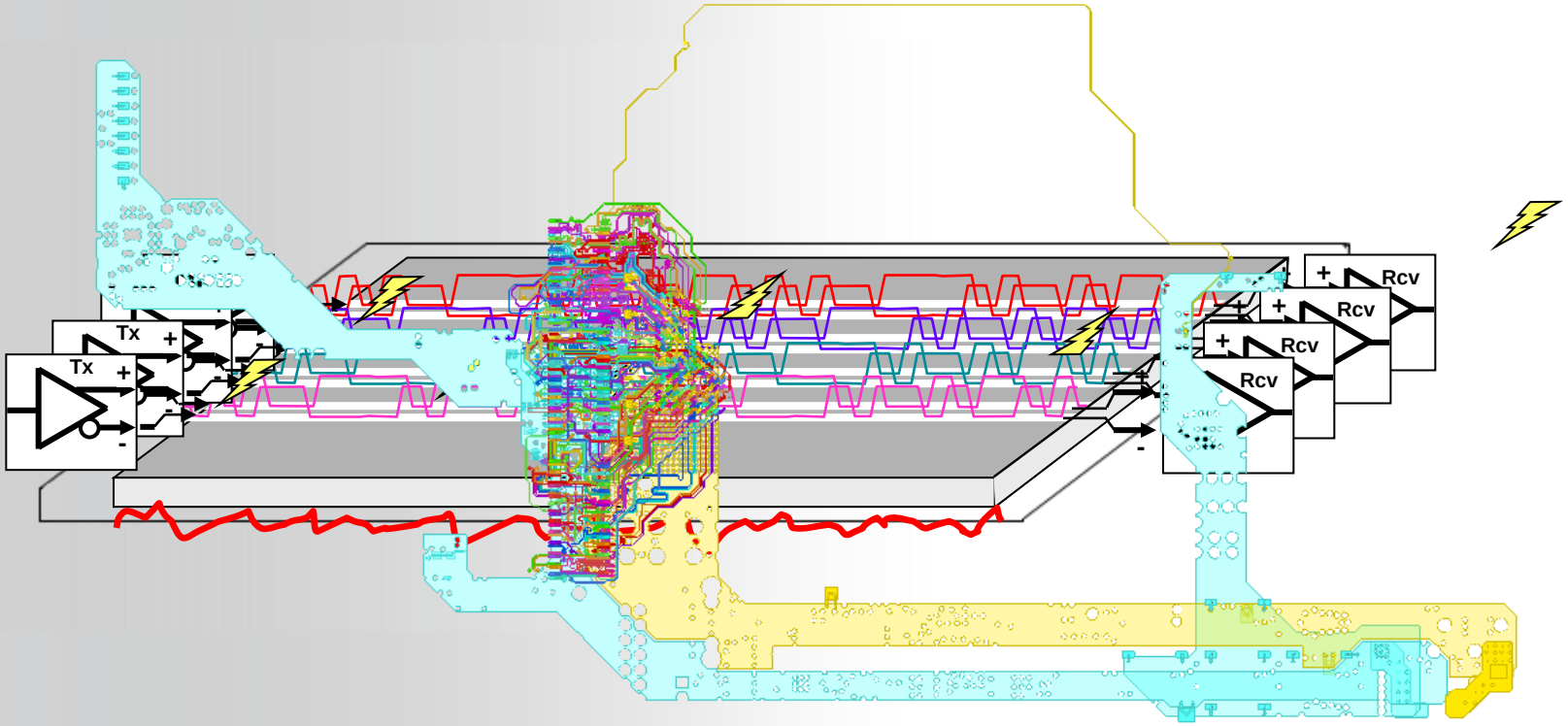
- Signal will see many discontinuities in its path
- Discontinuities will distort signal quality and reduce overall bandwidth of the system





Crosstalk

- Generally there are multiple “lanes” of serial data running side by side; these can CROSSTALK with each other.
- Power/Ground Bounce and Coupling to Signal Nets

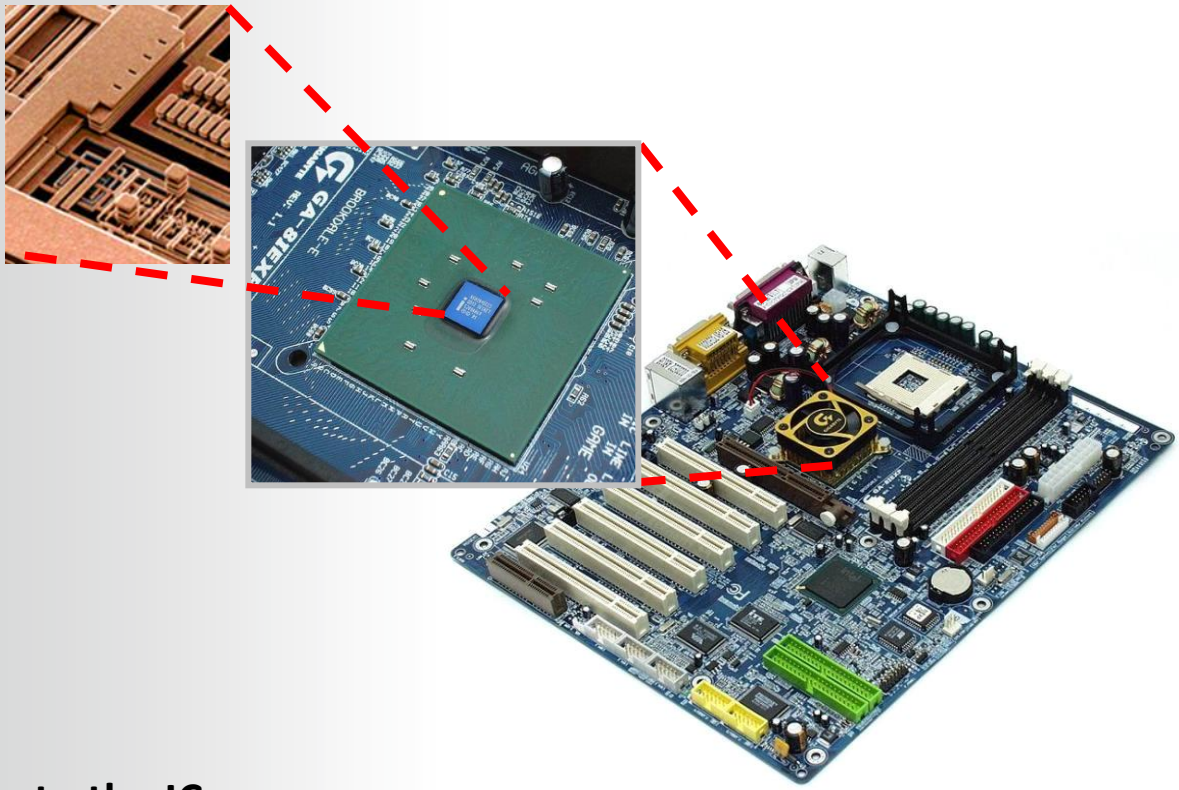


What is a Power Distribution Network (PDN)?

Complex multi-stage network supplying power to all devices in a system.

For typical products the PDN includes:

- **Voltage regulator module (VRM)**
- **Board power/ground planes and decoupling capacitors**
- **Package power/ground planes and decoupling capacitors**
- **Chip power/ground structures and capacitance**



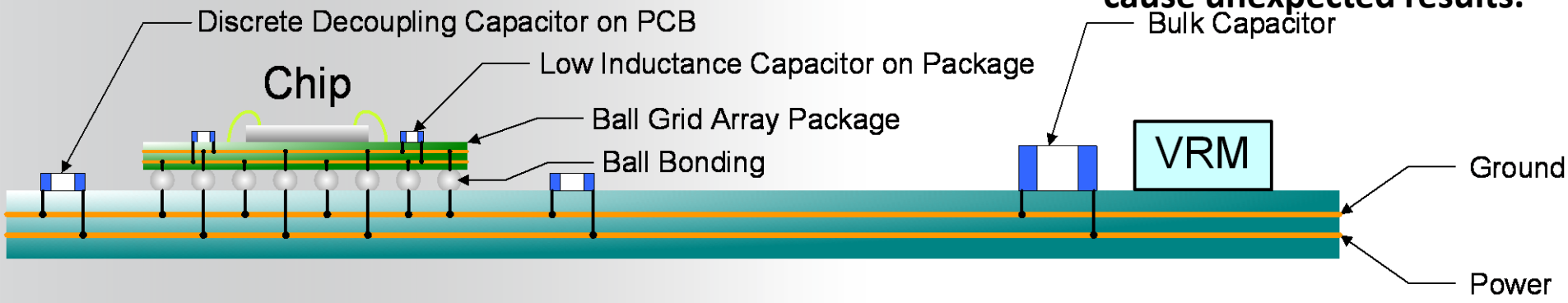
PDN Requirements:

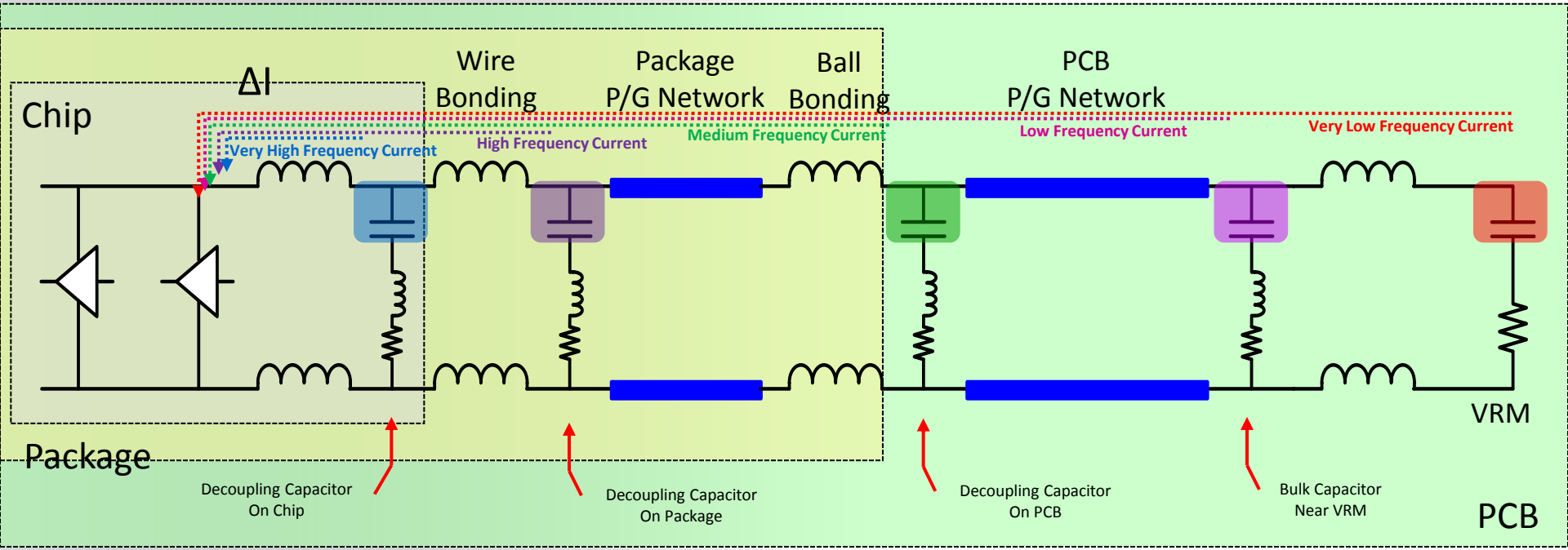
- **Must deliver clean power to the ICs**
- **Must provide low impedance, low noise reference path for signals**
- **Must not contribute excessive EMI**

Board Level Power Integrity?

It's important to consider the entire PDN when simulating. Interactions between components can cause unexpected results.

Full PDN





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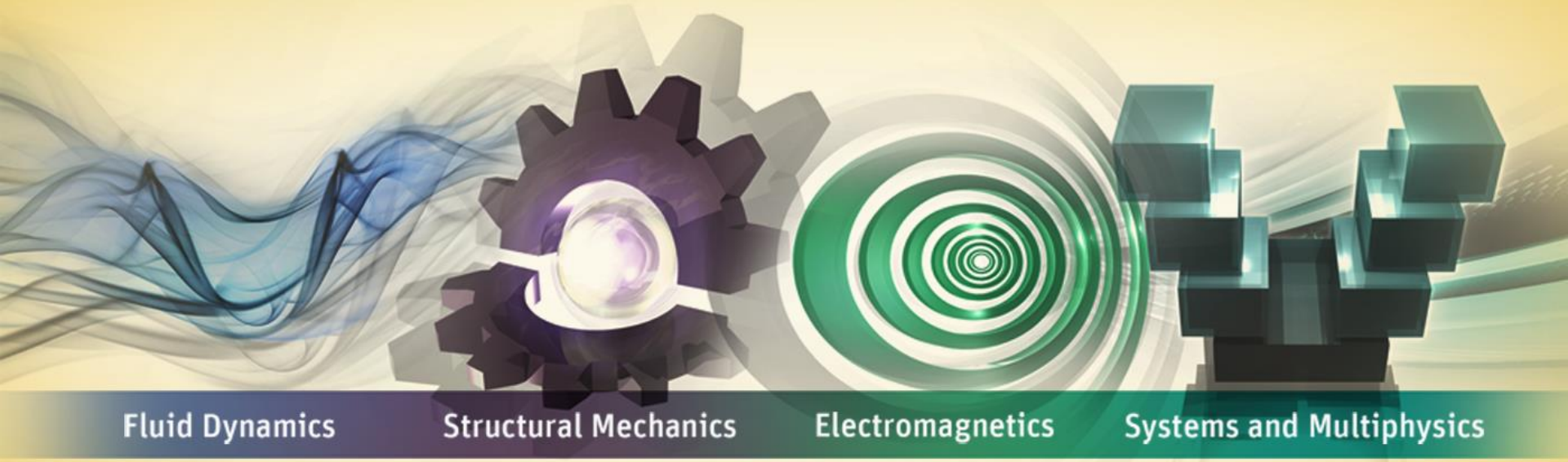
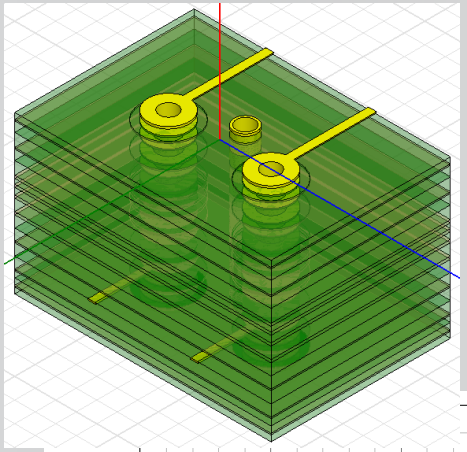
Simulation Requirements

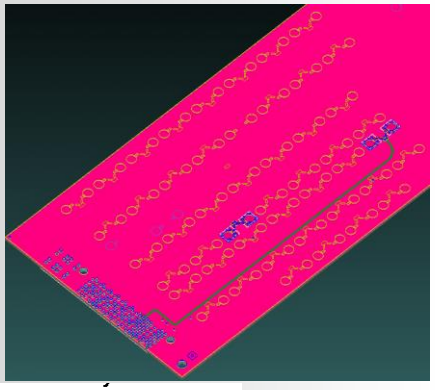


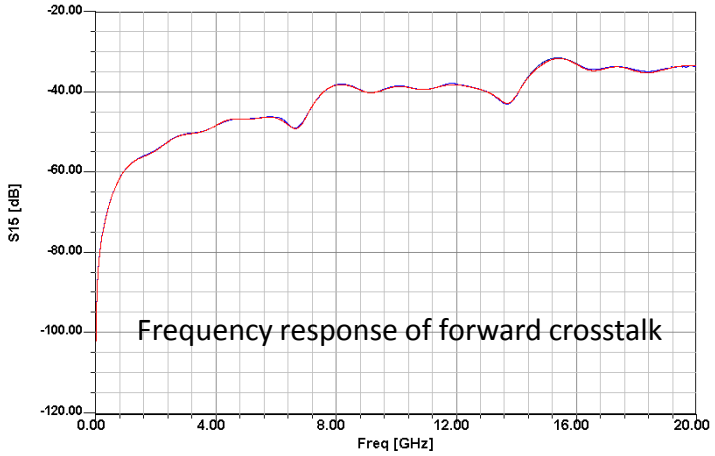
Simulation Requirements

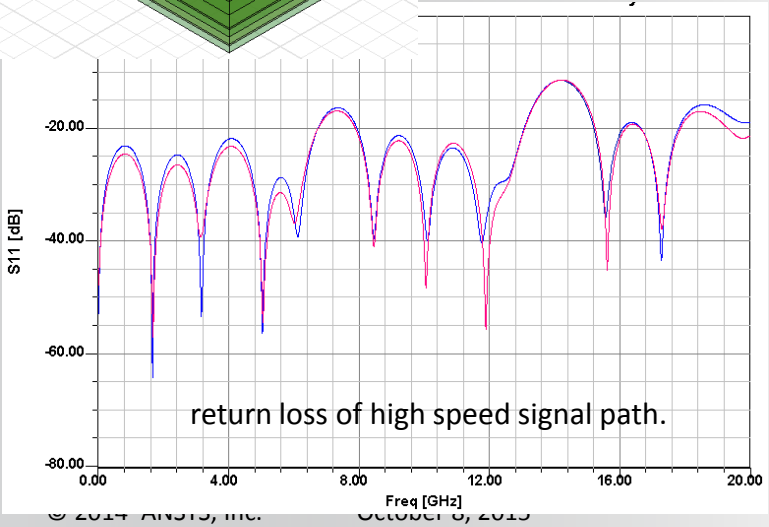
Components must be modeled using full-wave S-parameters

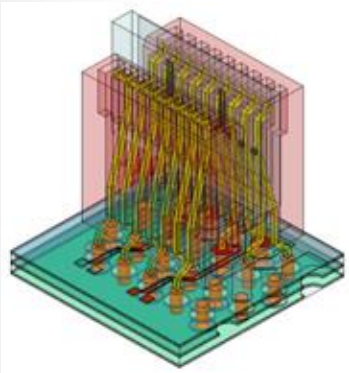
- **S-parameters provide the best representation of the electrical characteristics of very high-speed interconnects.**

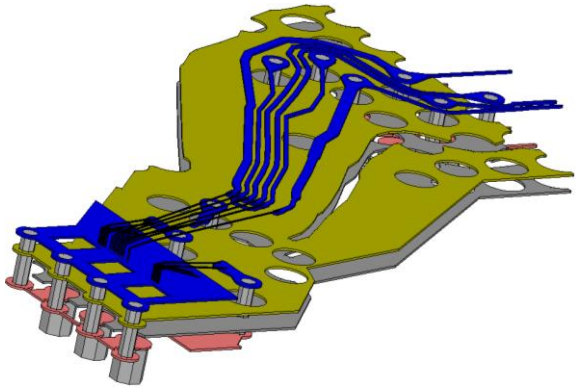








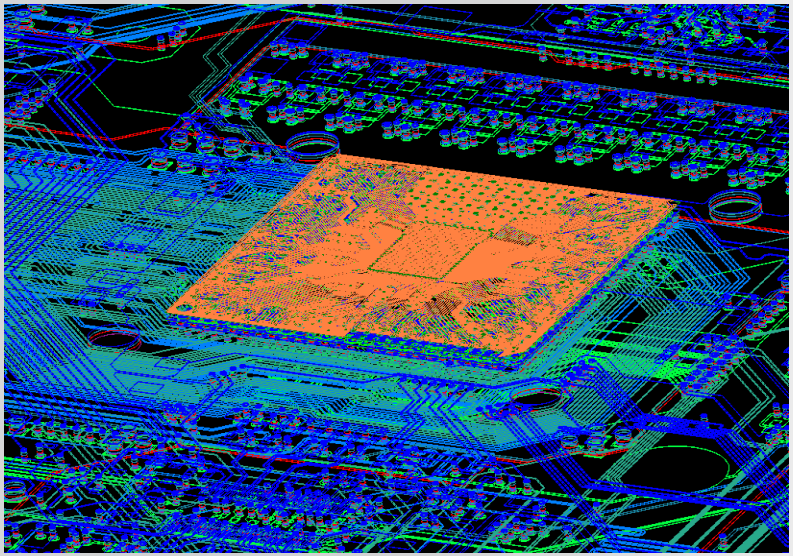


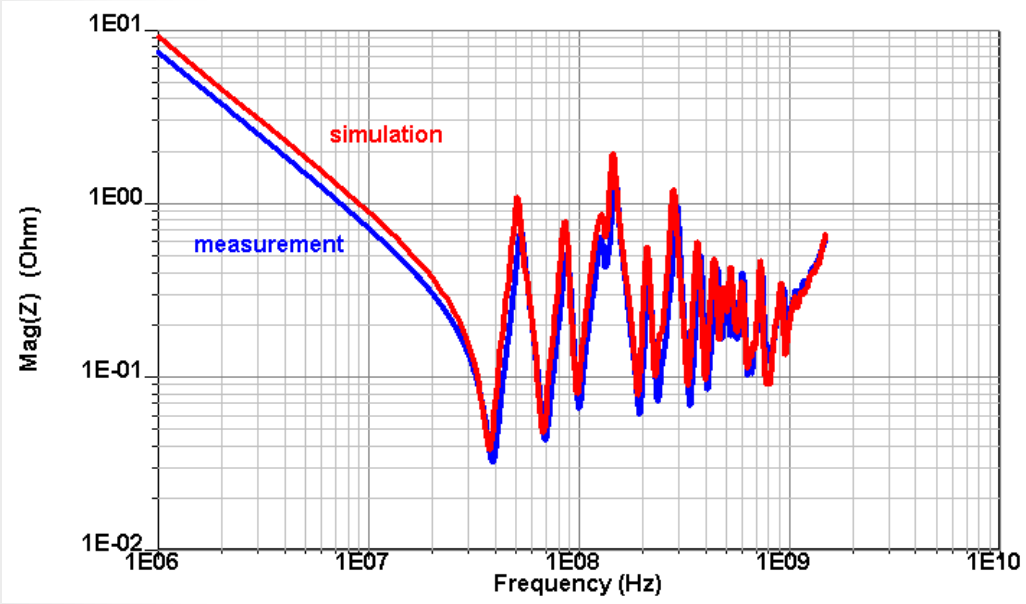


Simulation Requirements

Chip/Package/PCB must meet complex power-delivery requirements

- High package pin count and GHz-speed data rates translate into extremely fast I/O switching and high transient power sinking. Concurrently, PCB size is decreasing, power density is increasing, and power-delivery requirements are tightening.

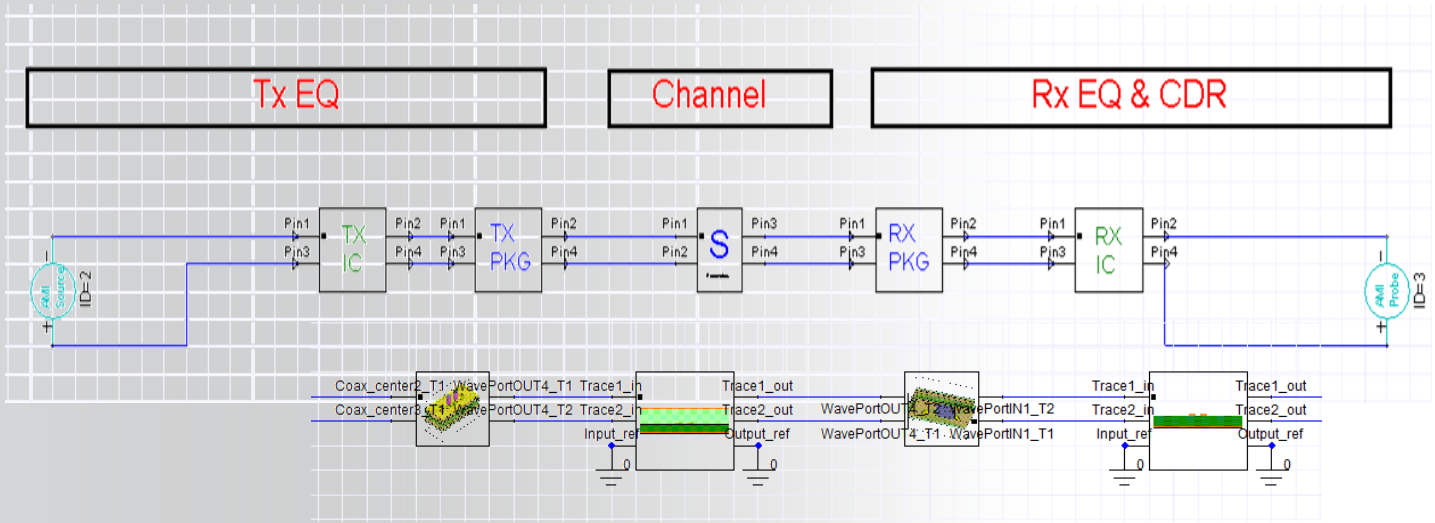


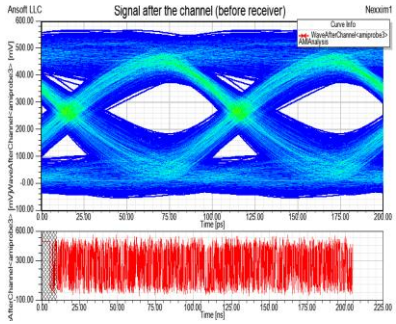


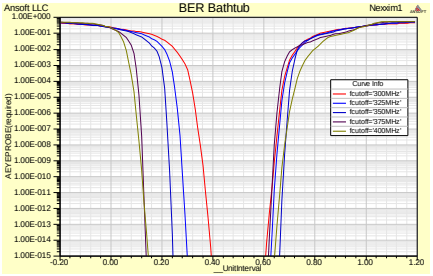
Simulation Requirements

Simulator must provide reliability and capacity for multi-gigabit channel modeling

- **Including S-parameters in transient simulations**
- **Maintaining passivity and causality**
- **Address multiple channel paths**
- **Combine transistor-level models of transceivers, pre-emphasis circuits and equalizers with extracted full-wave parasitic.**



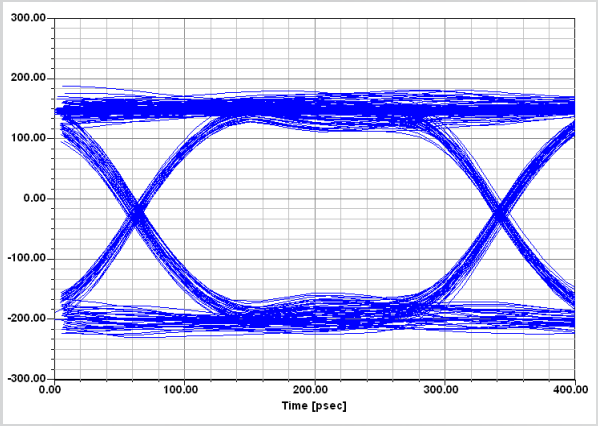


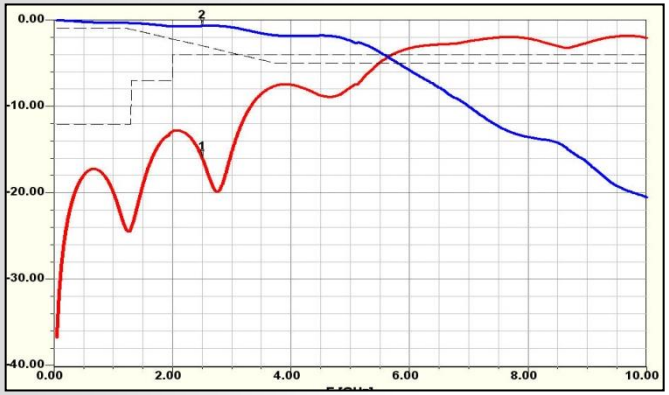


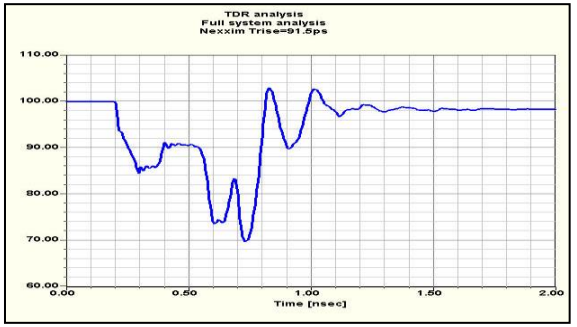
Simulation Requirements

Designs must include frequency- and-time domain simulations to correctly predict system performance

- High-performance electronic designs often include operating specifications for signal integrity in the time domain and for power integrity in the frequency domain.







Common time-domain parameters, such as eye diagrams, jitter, TDR measurements and SSN as well as frequency-domain metrics, such as resonances, phase-noise margins, power plane impedance, and insertion loss appear within the same spec sheet.

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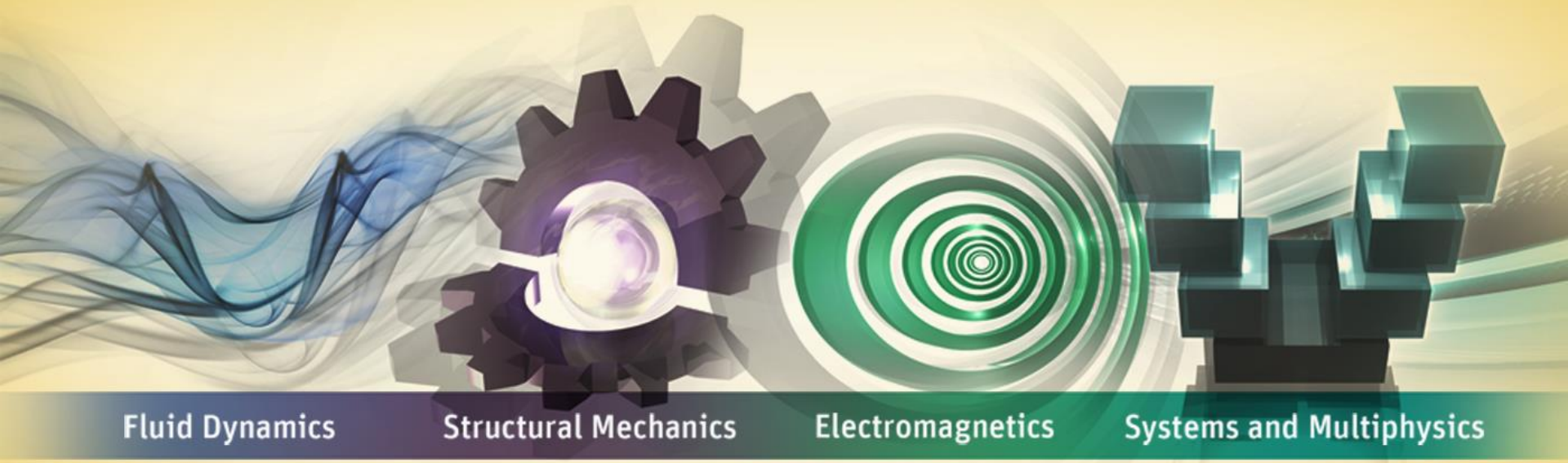
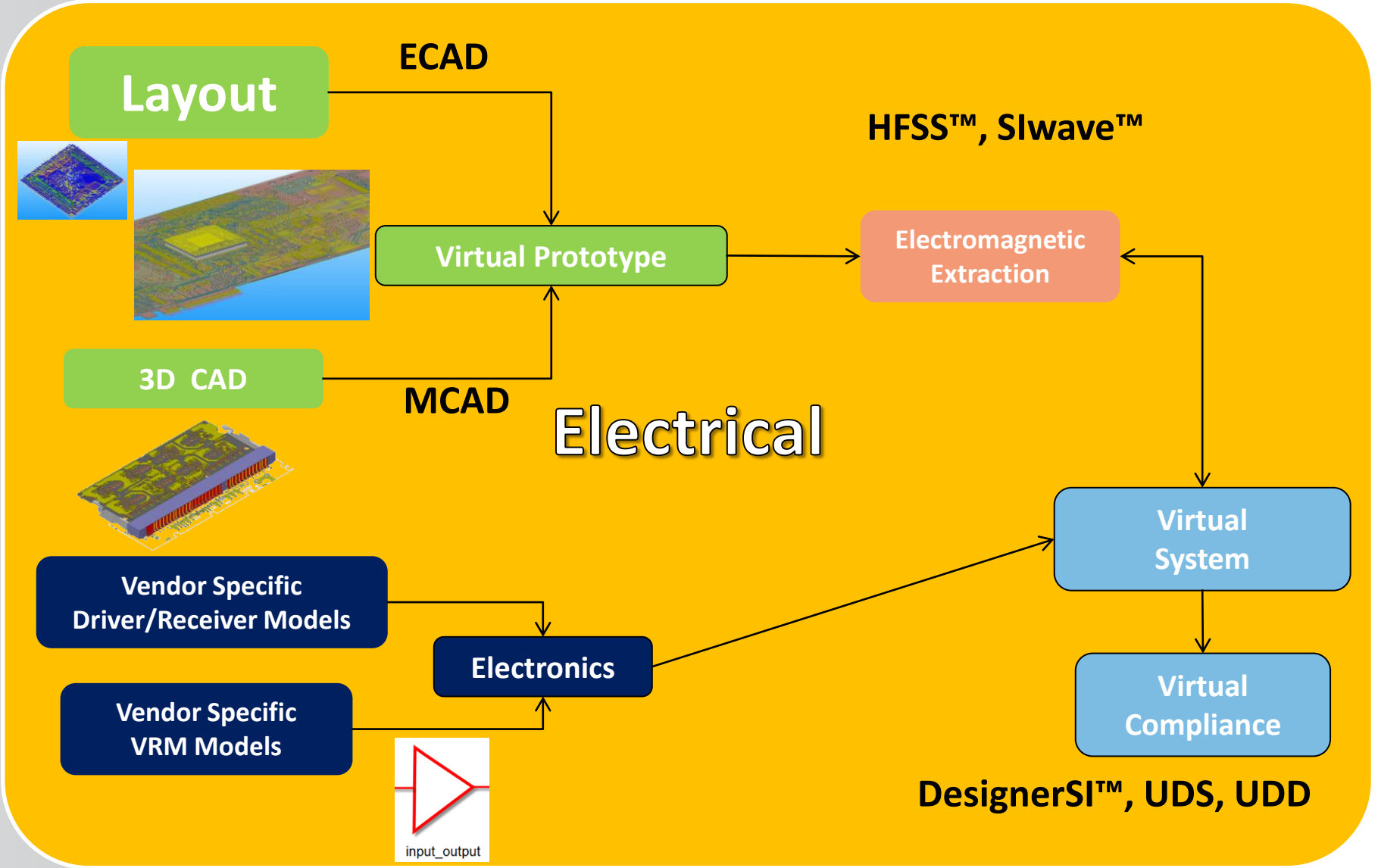
ANSYS Solution



Virtual System Prototyping

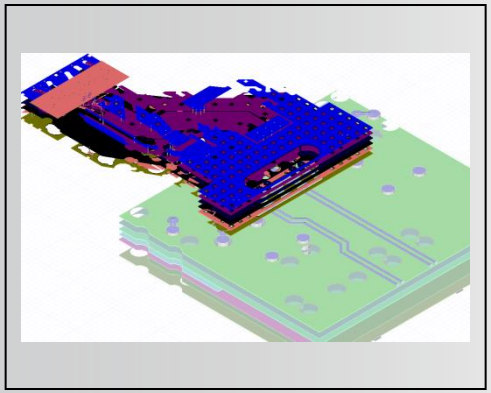


ANSYS Package/Board Solvers

Arbitrary 3D → **Hybrid** → **SPEED**

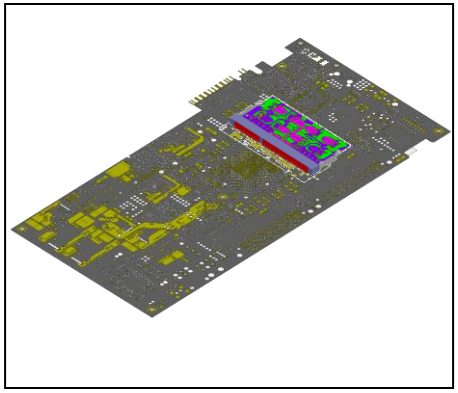
Arbitrary 3D Electromagnetics — Board + Package

HFSS for ECAD



- Golden Accuracy Simulator
- Solves Any 3D geometry
- Powerful for Critical Nets
- Layout Front-end for HFSS

SIwave



- FAST Hybrid method for PKG/BRD
- Handles many, but not all 3D effects

Any Geometry
Gold Standard Accuracy

Fast
SI, PI, and EMI hybrid solution

What is HFSS for ECAD?

Highly automated layout design environment

- Primitives = traces, pads, bondwires, vias
- Net name definition
- Automated boundary and port setups

Significantly reduce engineering time interacting with software

- Intuitive layout design entry for HFSS

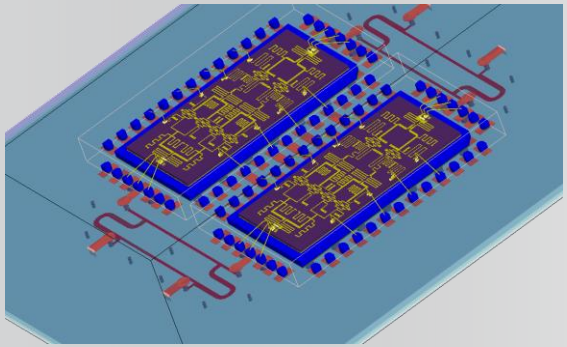
Lightweight interface for geometrically complex structures

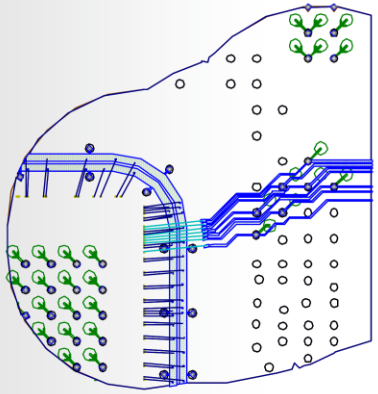
Direct HFSS solve from within the Cadence environment

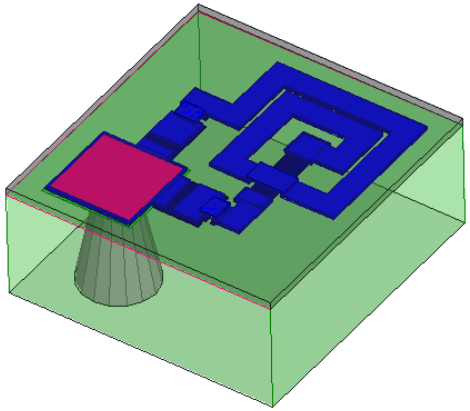
- **Virtuoso, Allegro, APD, and SiP**

Direct import of Cadence products using Cadence Extracta

- **Allegro, APD, and SiP**







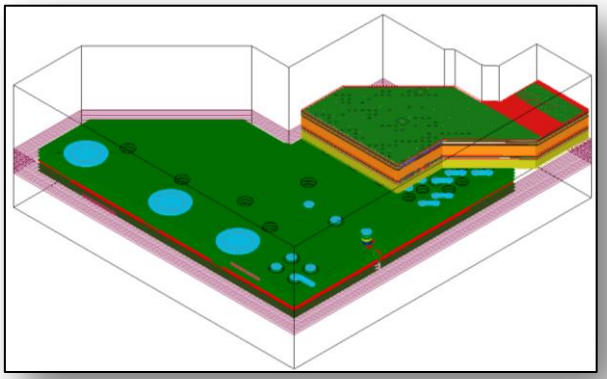
Advantages and existing Automation

HFSS Solver on Demand for Layout :

- For package, board or IC designs in Cadence and ODB++
  - Lumped port, PEC Boundary, or RLC Boundary on any pin definition
  - HFSS Solution Setup
    - Adaptive passes with convergence criteria
    - Solution basis
    - Frequency Sweep
  - Air box created around geometry, Radiation Boundary on air box

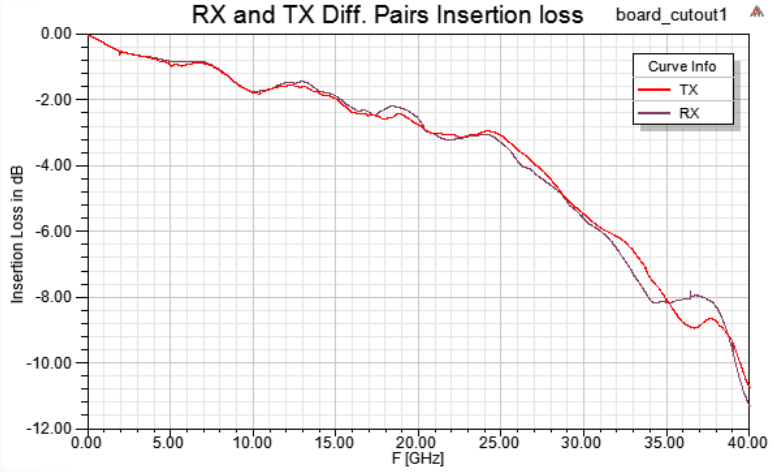
Benefits :

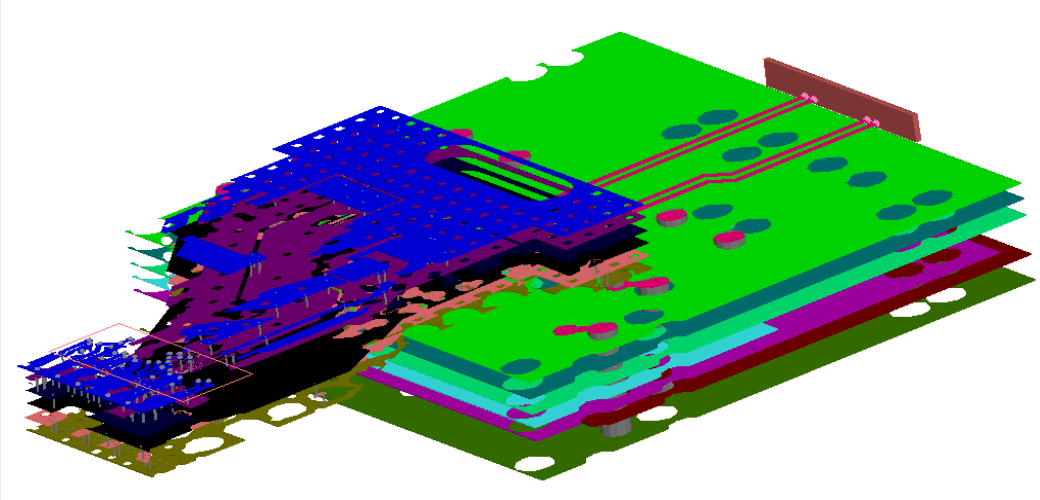
- Allows hierarchical stacked geometry to be created very quickly/easily
  - Allows packages and boards to be merged
- Parameterization
  - Trace Width, etching factor, Padstack Editors
- Layer stackup optimization
- Automated Geometry Clipping
- Surface Roughness
- Easy lumped port and waveport creation
- Maintain Trace Characteristics and Nets from Layout



Package and/on Board Example

- Intel Xeon @ 2.40 GHz, 16 cores
- Simulation from 0 to 40GHz, 4001 Frequencies, Interpolating sweep
- Initial mesh in 4min32
- 3rd pass in 16 mn with a value of +/- 10% to the final solution
- 7 passes to converge in ~1 hour
- 16 Frequency points solved in // using 16 core each in 6h12mn
- 8 Frequency points solved in // using 8 cores each in 10h



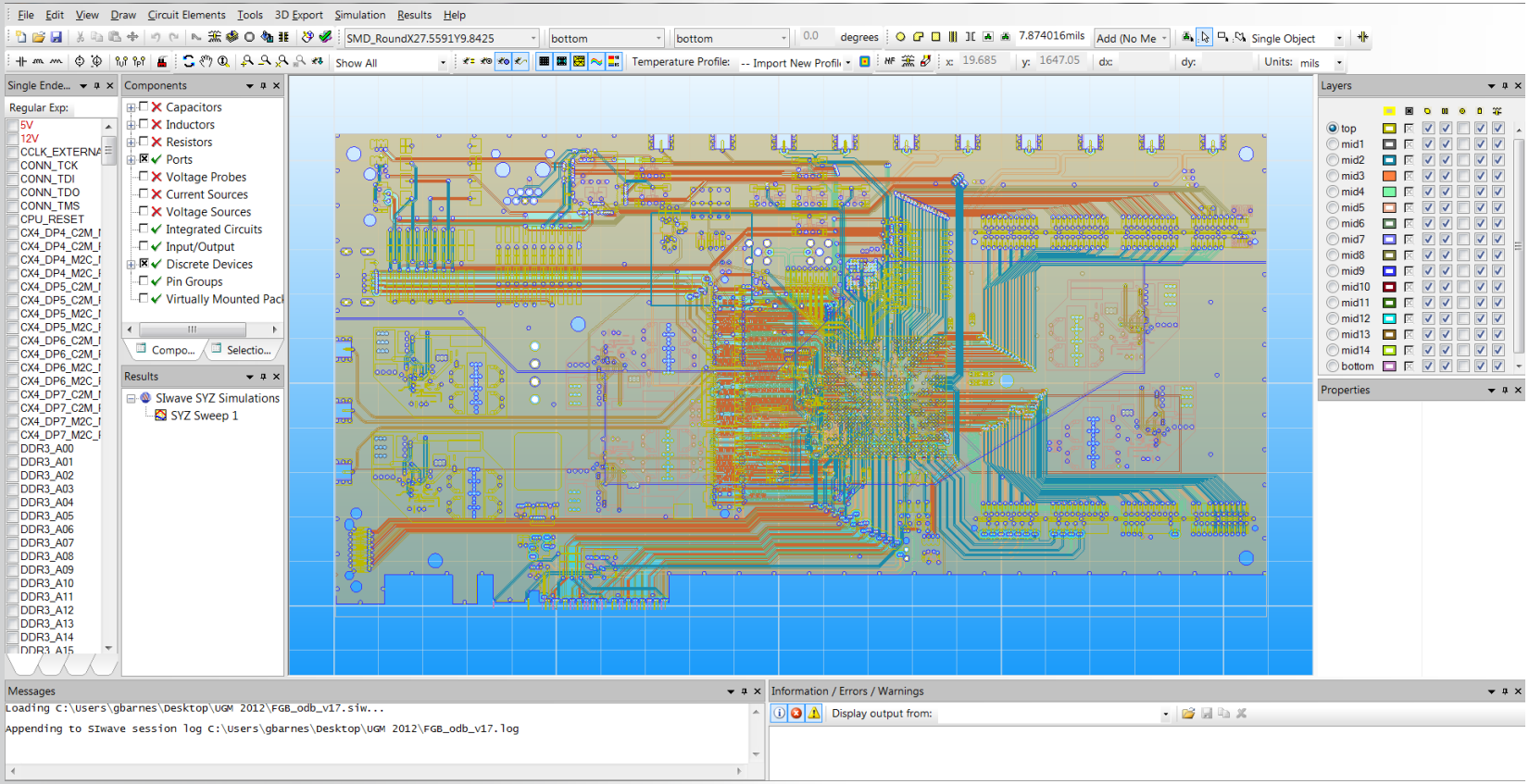


What is SIwave?

- **ANSYS SIwave evaluates designs from entire package or board or package on board. SIwave does so including all effects of coupling between traces, packages, and board.**

•Advanced Signal- and Power-Integrity Analysis
•Easy Layout Extraction (S,Y,Z)
•Automated Decoupling Capacitor Optimization
•Impedance Calculator
•Integrated and Automated DC I^2R Reporting

•Sophisticated EMI/EMC Capability
•Advanced Broadband SPICE Model Generation
•Highly Accurate Macro Modeling
•High-Performance Computing
•Comprehensive Multi-physics (Icepak)



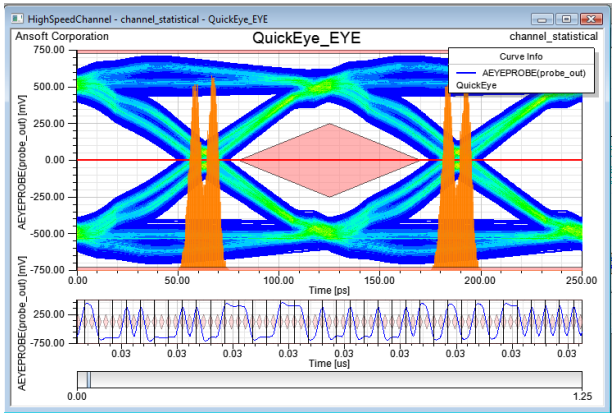
Designer SI - Circuit Simulation -

- **Schematic entry GUI or Netlist entry (user choice)**

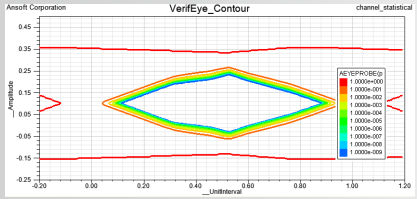
Supports

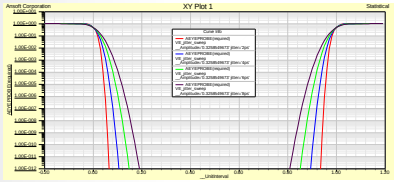
- **HSPICE netlists, Spectre netlists, and Spectre RF netlists**

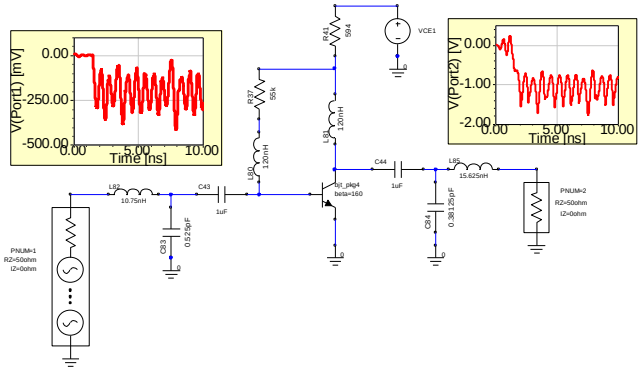
Simulation Engines(SI focused analyses)



- **Linear network analysis (SYZ network analysis)**
  - Causality checking and enforcement
  - Passivity checking and enforcement
  - TouchStone viewing and matrix reduction
- **Traditional Transient**
- **QuickEye (Convolution bit pattern based approach)**
  - Eye diagrams , Including Peak Distortion Analysis (determines channel worst case bit pattern)
- **VerifEye (Statistical convolution approach)**
  - Bit error rate (BER) contour and bathtub plots
  - Including 8b/10b with disparity algorithm
- **AMI analysis**

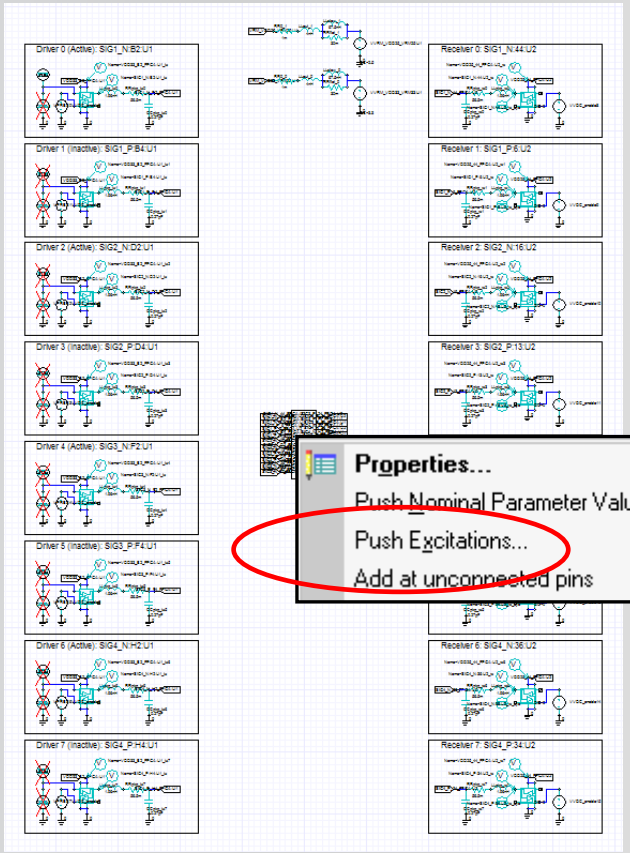


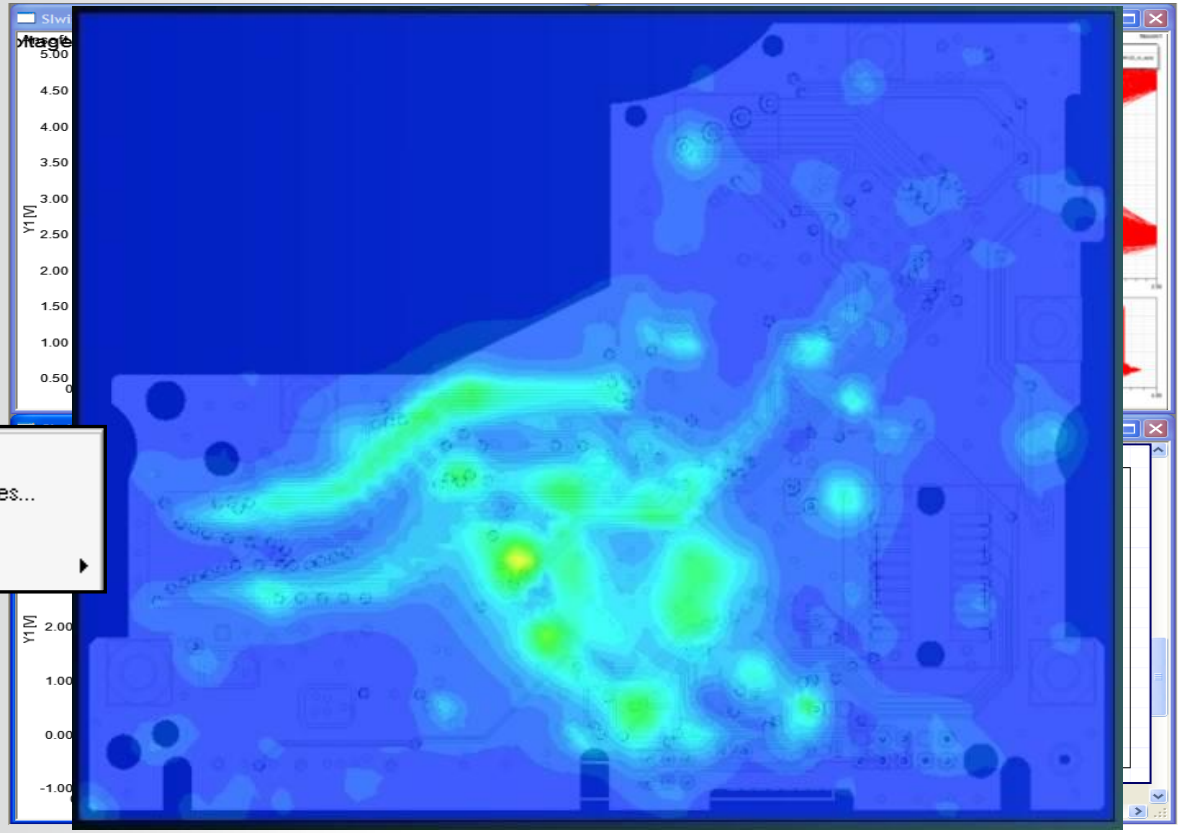




Push Excitations for True EMI/EMI simulation

When Transient Analysis is complete, voltage/currents at the PCB terminals are „pushed“ back to the field solver

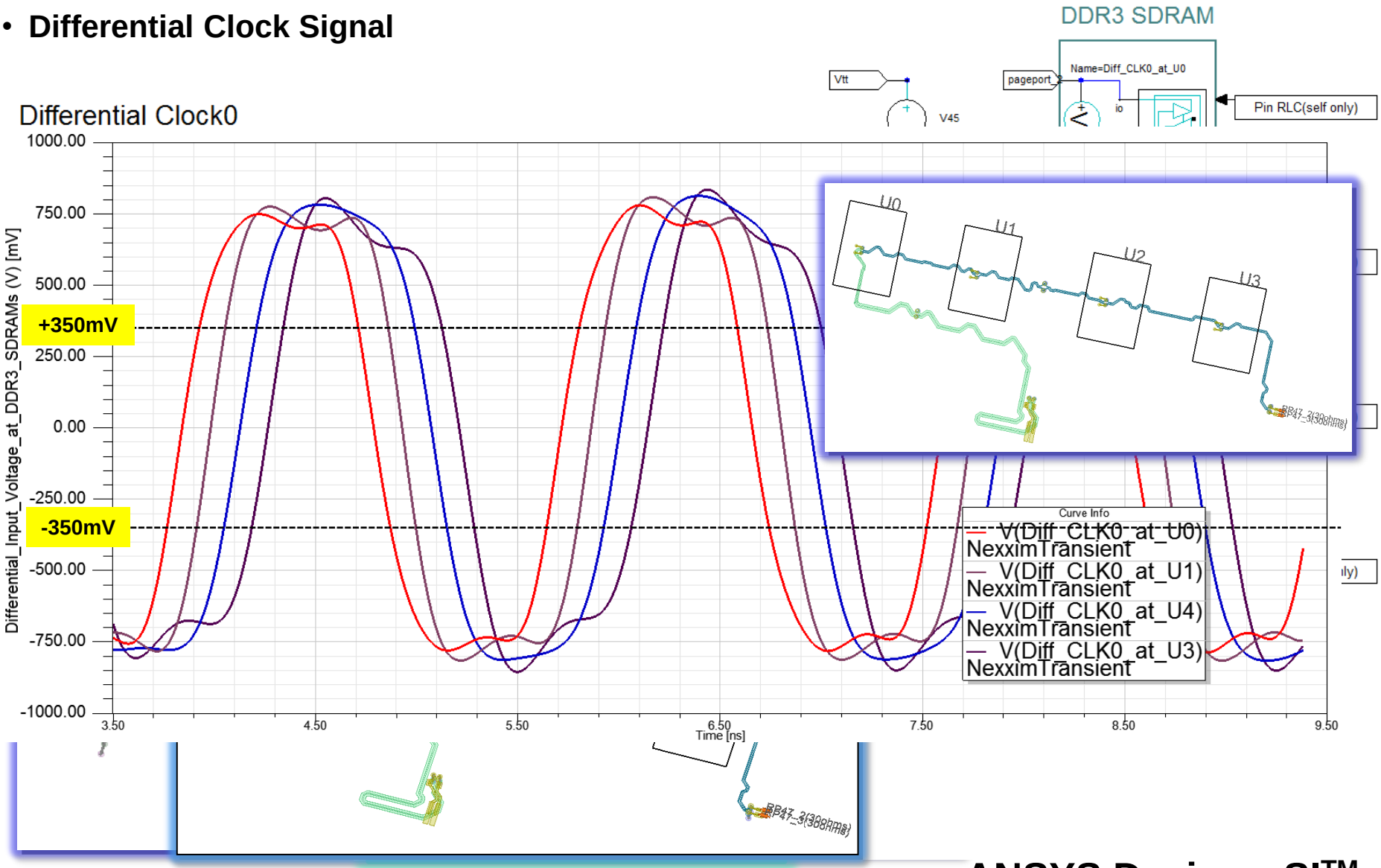




Example 1 :
Signal Integrity – DDR3

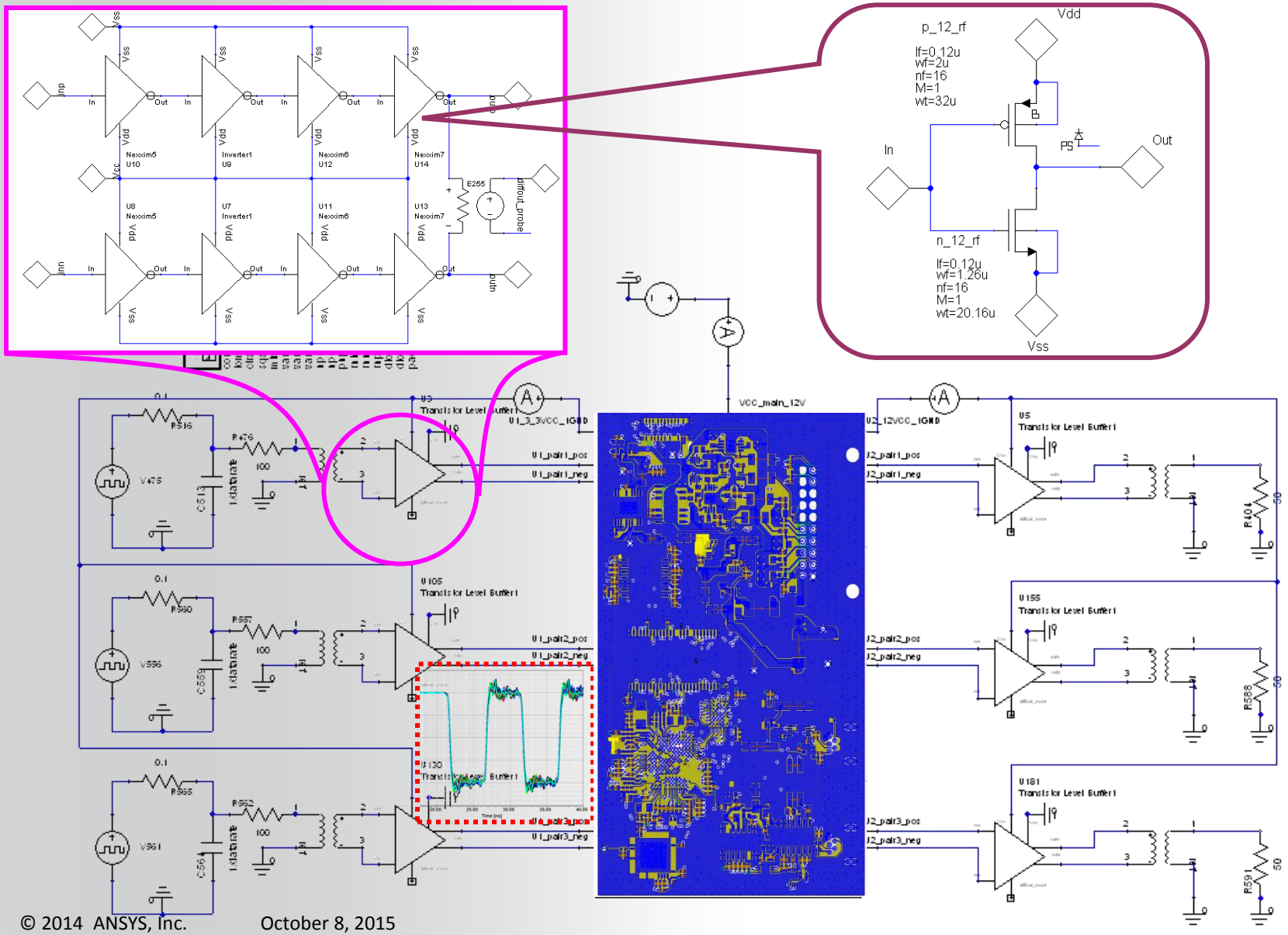
Post Layout Simulation (1066Mbps)

- **Differential Clock Signal**

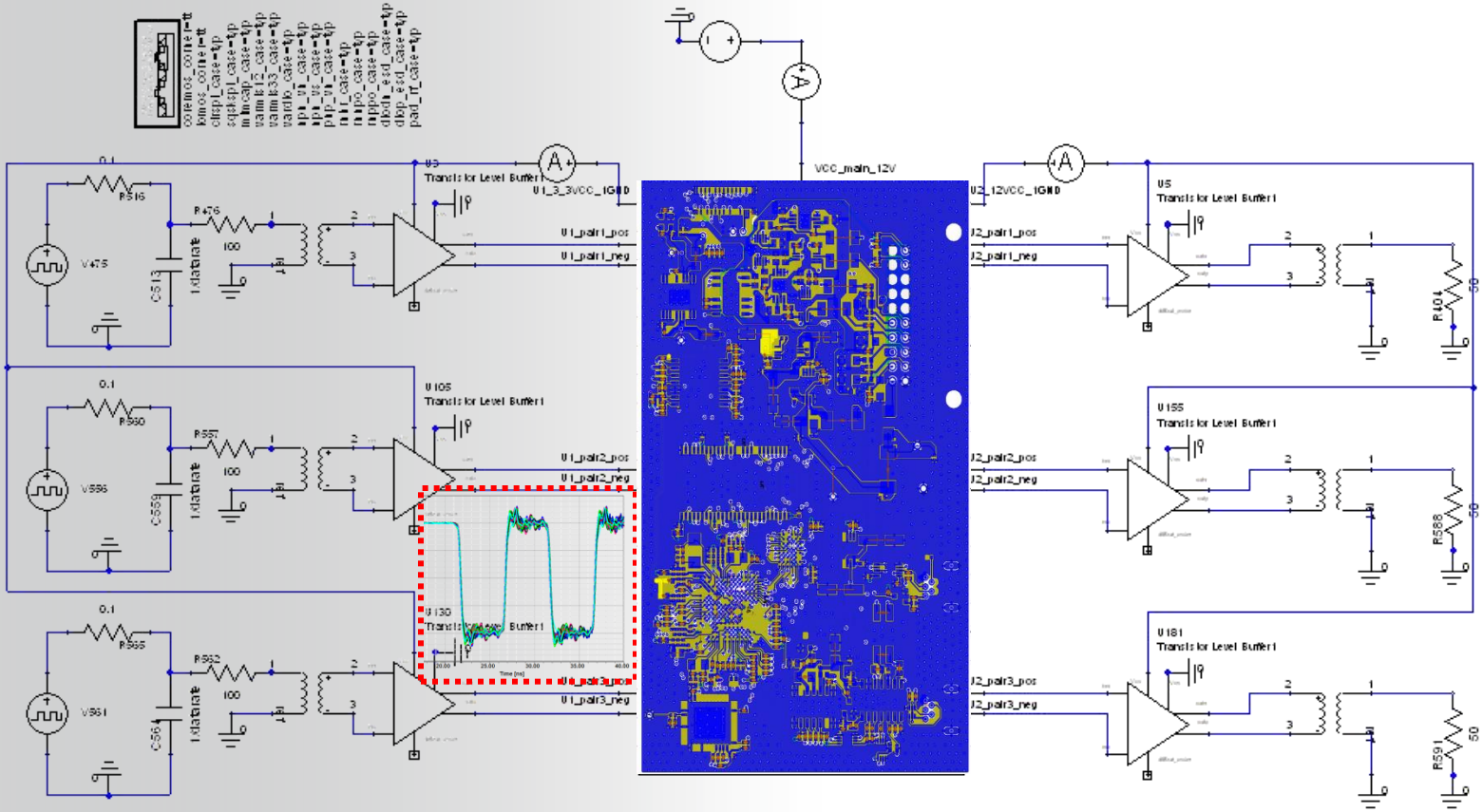


Example 2 :
Total System & Circuit Example

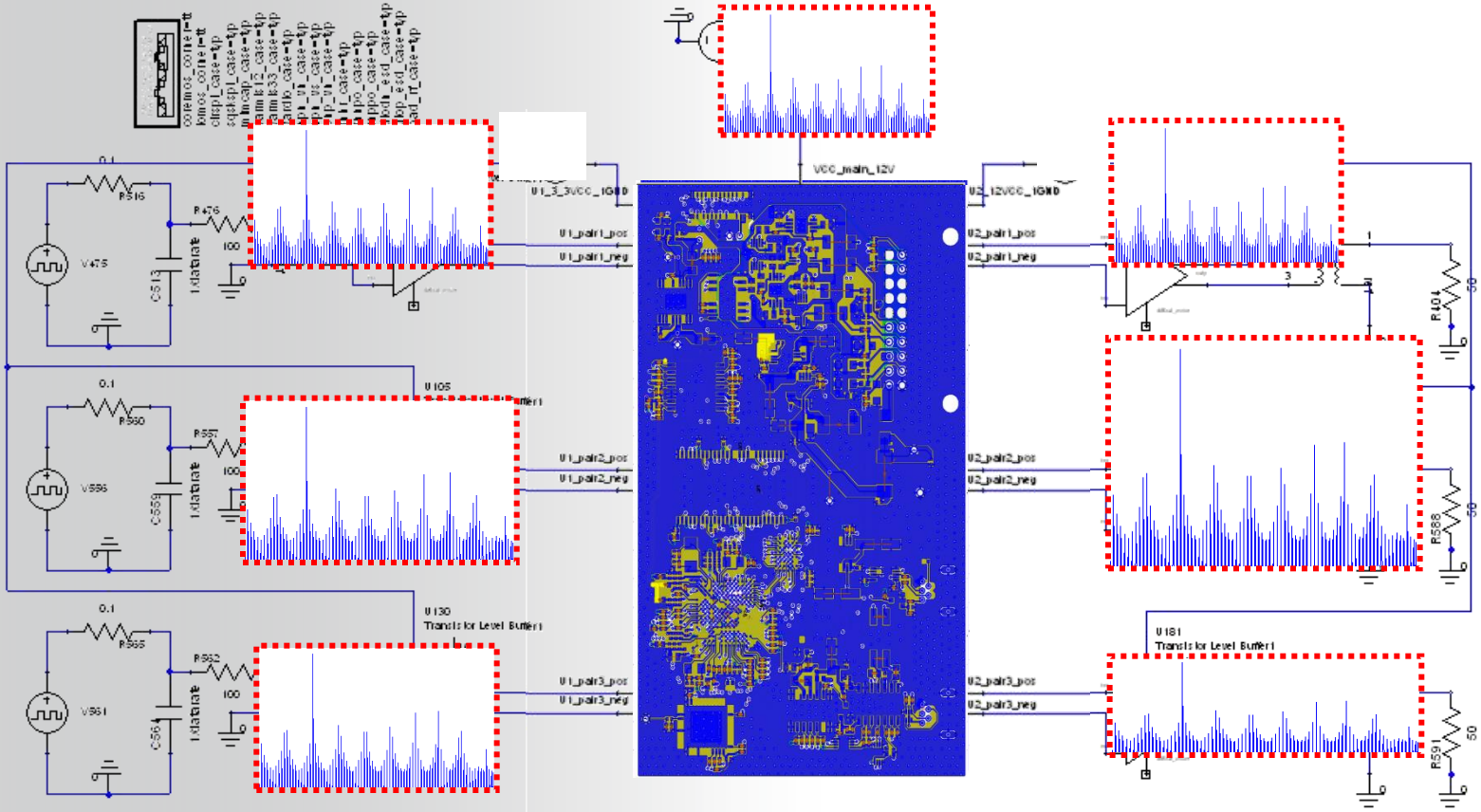
Total System & Circuit Example



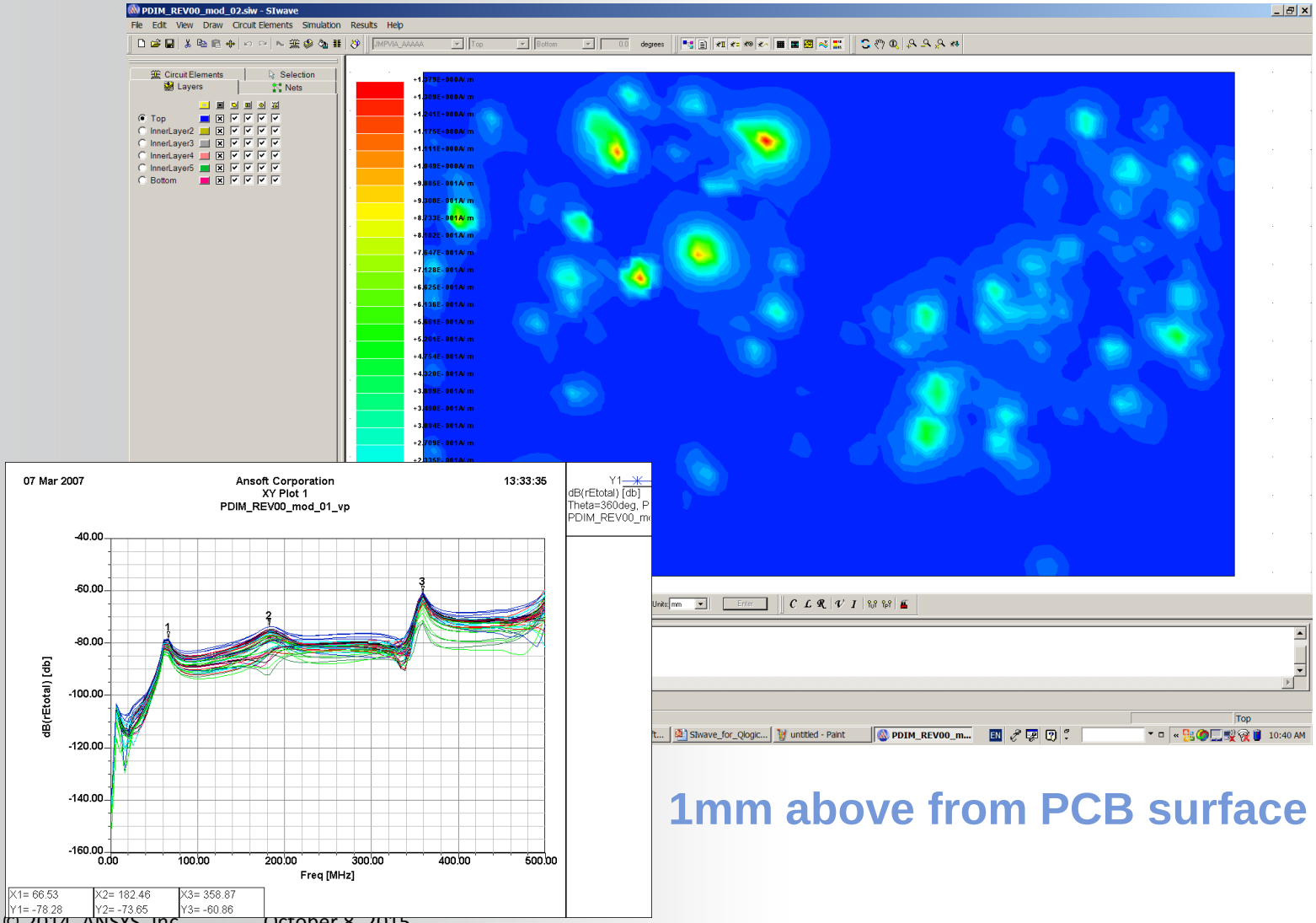
Total System & Circuit Example



Total System & Circuit Example



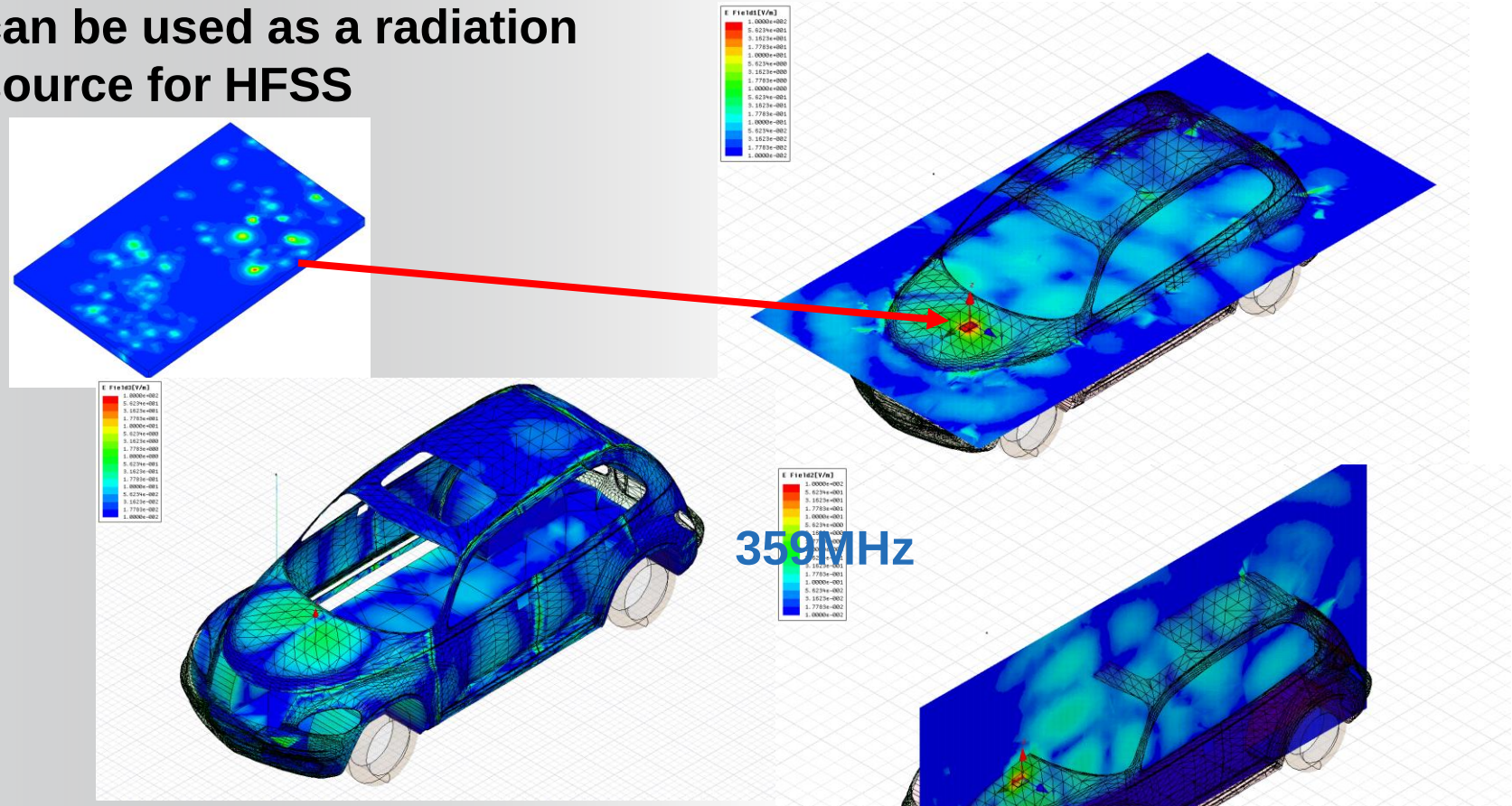
359MHz Near Field Distribution



1mm above from PCB surface

HFSS & SIwave Near Field Link Analysis

SIwave Near field solution can be used as a radiation source for HFSS



Dynamically link SIwave to HFSS to plot the field strengths around the enclosure