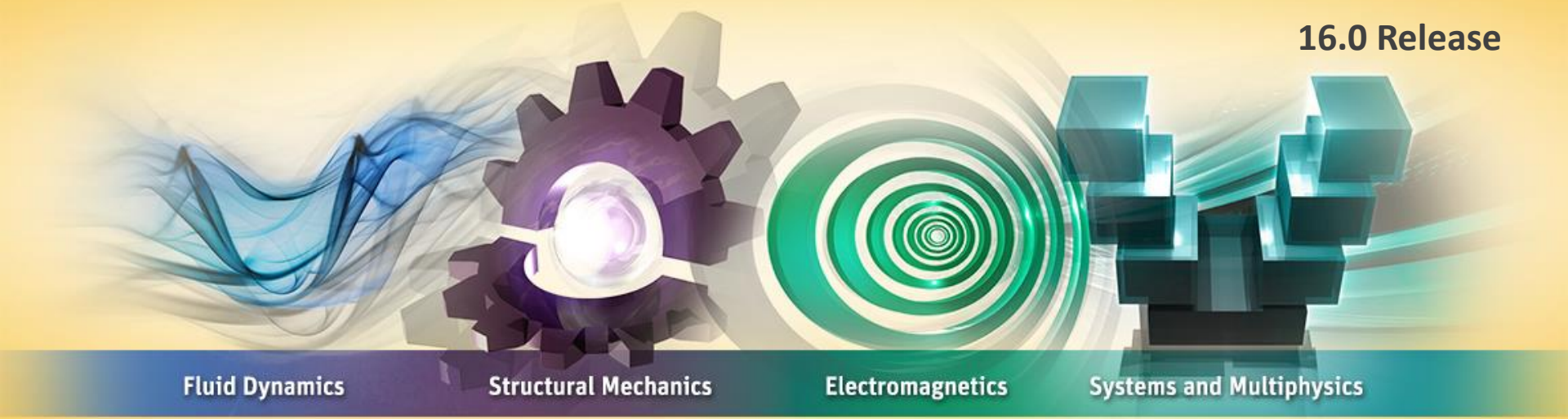
Workshop 2:
SSN

16.0 Release



Introduction to AEDT SI

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  - Schematic Entry
  - IBIS Component Import
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- **Simultaneous Switching Noise (SSN) Overview**
  - Fast switching speeds associated with high data rates can lead to unwanted interference between data channels. This effect is caused by electromagnetic coupling between the physical interconnects, as well as noise generated in the power distribution network.

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- In order to predict switching noise, the properties of the physical channel as well as the driver and receiver must be considered. The driver and receiver circuits are often represented by behavioral IBIS models. These IBIS models encompass the transient properties such as delay, overshoot and slew for the driver as well as impedance of the receiver. The electromagnetic properties of the interconnects can be determined using electromagnetic analysis. The resulting model of the physical channel is represented as scattering or s-parameters. One common format used to represent s-parameters is the HSPICE™ S-element.

- This exercise demonstrates how to set up the transient simulation for an 8-channel data interface that includes the power distribution network. Drivers and receivers are represented using IBIS models, while the physical interface between transmitter and receiver is represented using an s-element model.

- The simulation results are displayed as transient voltage wave forms and as eye diagrams

SSN Example

- **Introduction**

  The goal of this exercise is to learn how to create a schematic, define and run transient analyses, and view simulation results for a high speed interface.

- **Launching ANSYS Electronics Desktop**

  To access ANSYS Electronics Desktop, click the Microsoft Start button, select:

  All Programs > ANSYS Electromagnetics > ANSYS Electromagnetics Suite 16.0 > ANSYS Electronics Desktop 2015

  To open a new project:

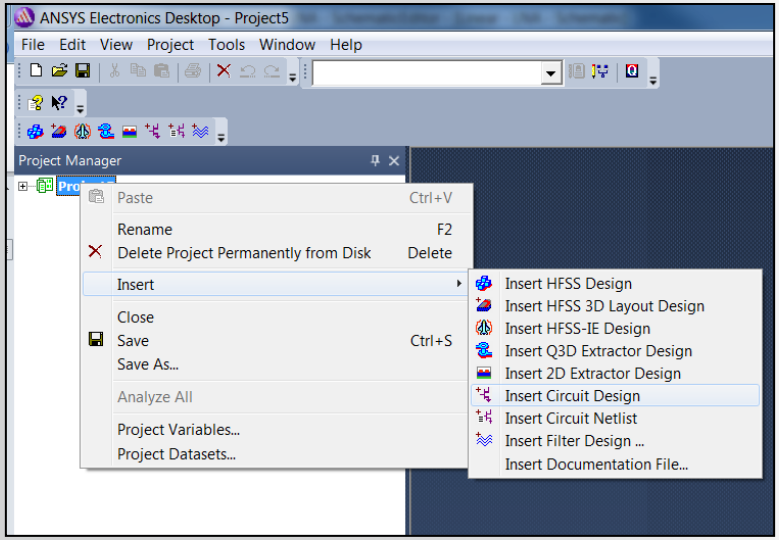
  In an AEDT window, Click the 🗋 On the Standard toolbar, or select the menu item ***File > New.***

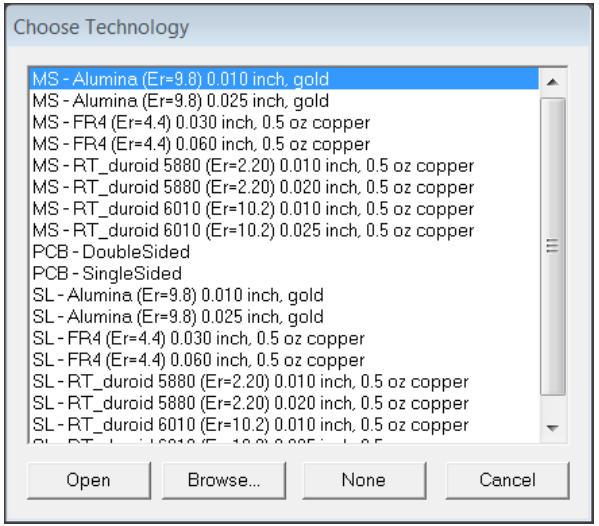
  From the Project menu, select ***Insert Circuit Design*** or **Right Mouse Click** on project folder and select **Insert Circuit Design** . A new window is created for schematic entry.

  Click the **None** button when prompted to Choose Layout Technology.

SSN Example

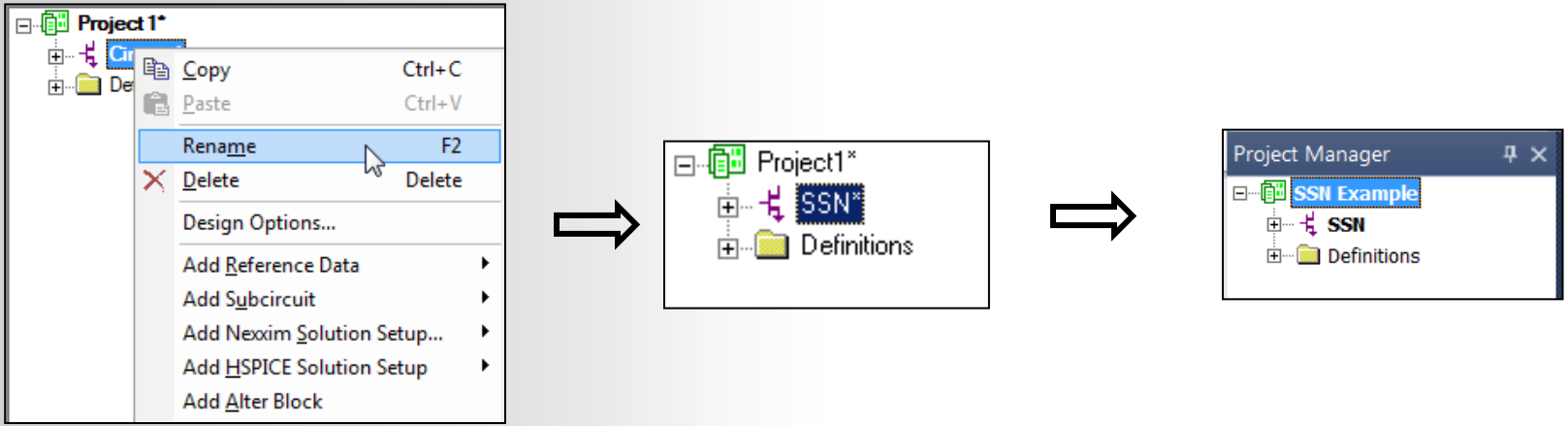
Opening a new project





Save Project

- **Save your project**
  - The main Designer window now contains an empty schematic. Right-click on the design **Circuit1** under the **Project Manager** and select ***Rename*** to rename the design to **SSN**.

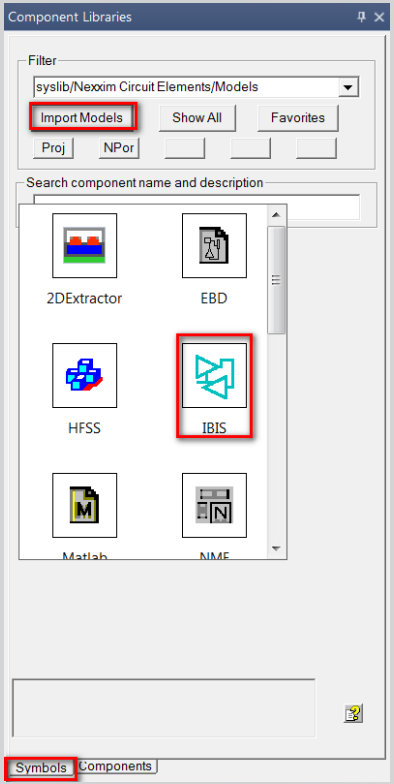


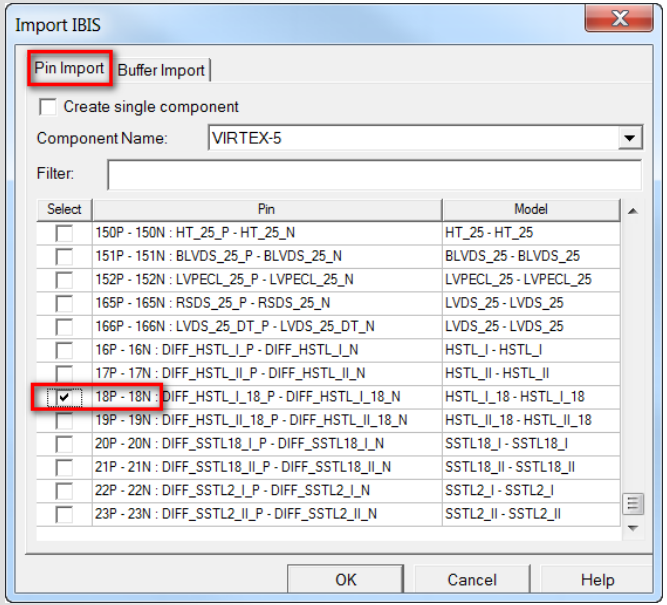
  - Select the menu item ***File > Save*** to save the project as **SSN Example**.
    - This will create a file named: **SSN Example.aedt** in your working directory.

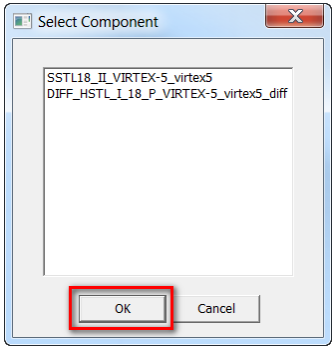
Import IBIS Component: Driver Buffers

- **Importing IBIS transmitter model**
  - Go to the **Component Libraries window** and click on the button **Import Models**
  - In the **Symbols** tab click on the item named **IBIS**
    - In Select File window browse to the **IBIS-AMI_Models** directory and select **virtex5.ibs**
    - Import IBIS Dialog
      - Checkmark **14: SSTL18_II**
      - Scroll down to the very bottom and checkmark **18P-18N**
      - Make sure both pins are present and press **OK**

Import IBIS Component: Driver Buffers

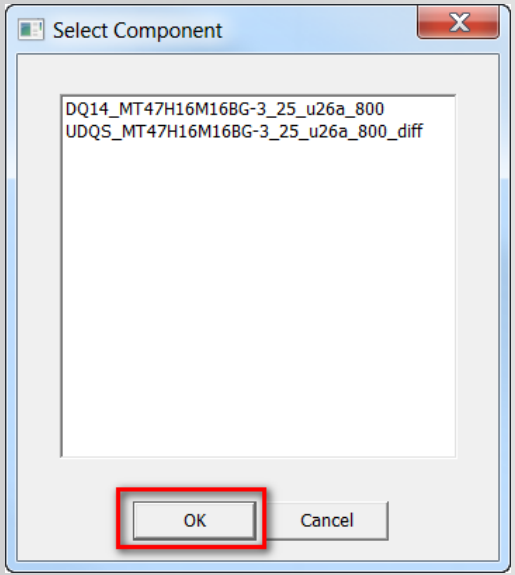


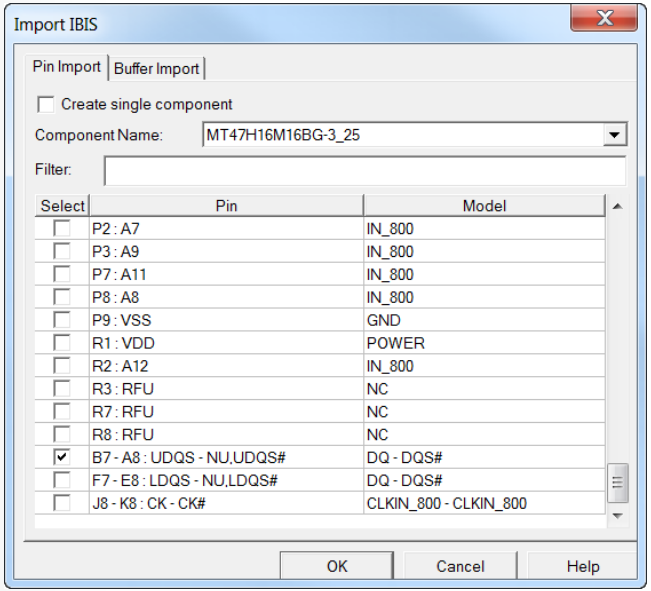




Import IBIS Component: Receiver Buffers

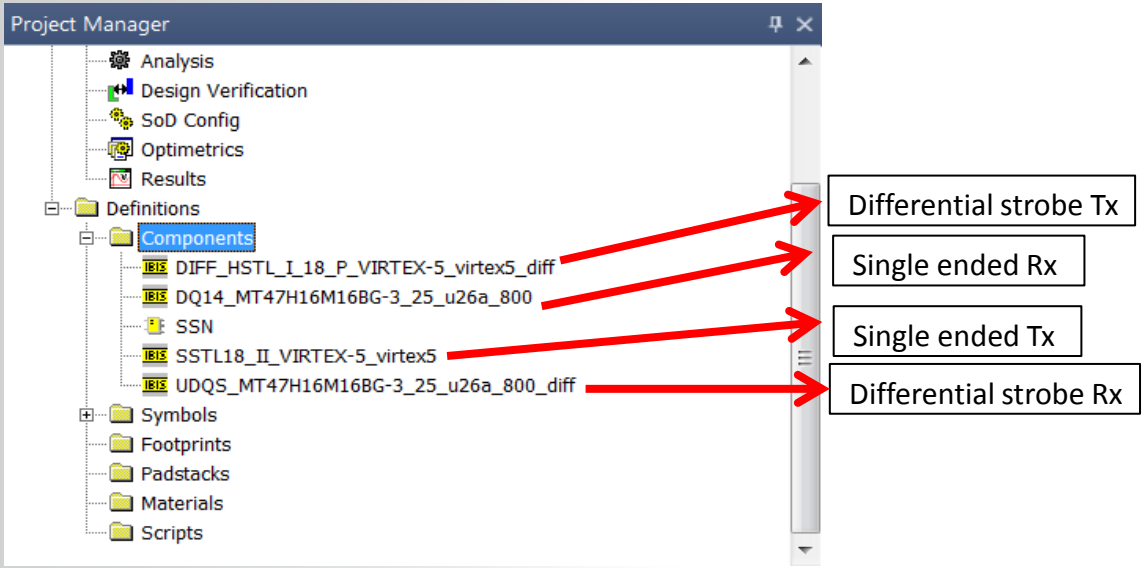
- **Importing IBIS receiver model**
  - Next, repeat the previous process to import the receiver IBIS models. Select the file **u26a_800.ibs** and click **Open**.
  - In the **Import IBIS** dialog window select the checkbox for pin **B1: DQ14.**
  - Scroll to the bottom of the pin list and select the differential pin **B7-A8:UDQS-NU.DQS#**.
  - Click **OK** to import the buffers.





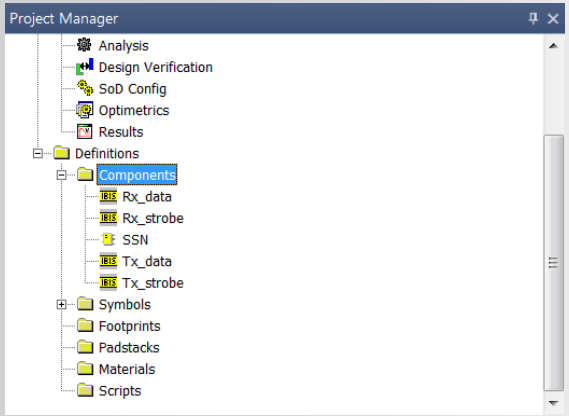
Verify Component Definitions

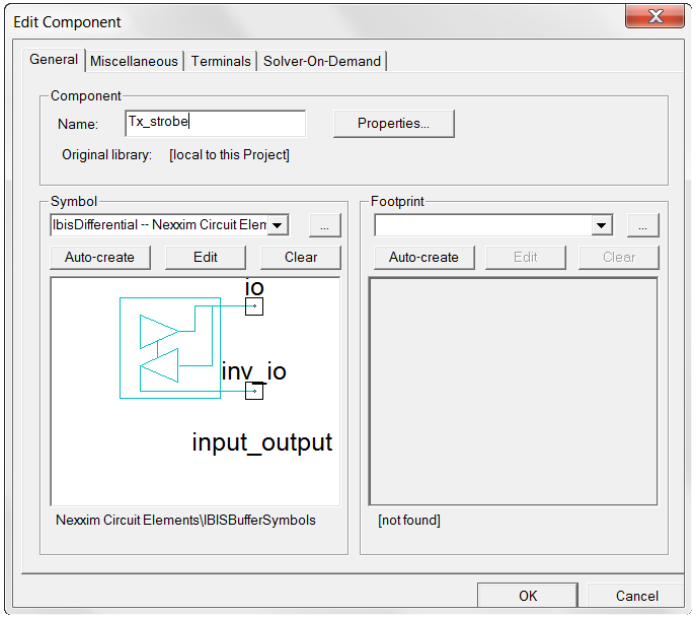
- **Component Definitions**
  - The four IBIS buffers should now appear in in the **Definitions** folder of the **Project Manger** under **Components**.
  - The names are automatically generated based on the IBIS pin and component names



Rename IBIS Components

- Right click on the component named **DIFF_HSTL_I_18_P_VIRTEX-5_virtex5_diff**
  - Select **Edit Component**
  - Change the name to **Tx_strobe**
  - Click **OK**
  - Repeat for the other 3 IBIS components
    - **SSTL18_II_VIRTEX-5_virtex5: Tx_data**
    - **DQ14_MT47H16M16BG-3_25_u26a_800: Rx_data**
    - **UDQS_MT47H16M16BG-3_25_u26a_800_diff: Rx_strobe**



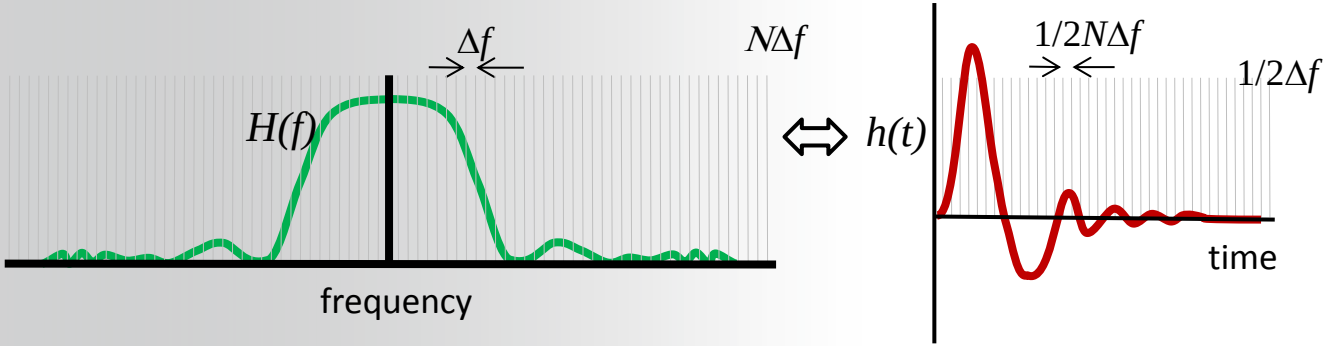


S-Element Model

- **S-Element Model**
  - The S-Element model contains the s-parameters of the data interface. This interface could be comprised of traces, via transitions, connectors and/or the package parasitic contributions. In this example, the data interface consists of multiple coupled traces on a printed circuit board along with the driver/receiver power distribution network. The model was generated using the full-wave electromagnetic solver SIwave™ .
  - Conventional SPICE based primitive components such as inductors, capacitors and resistors are constrained to a predefined frequency response. S-parameters can represent a network of arbitrary frequency response. The s-parameters are a tabular description of a frequency dependent network transfer function, and can therefore describe any linear network over any bandwidth.

S-Element Model

- The challenge for a circuit simulator when dealing with s-parameters is to apply a physically plausible algorithm to interpolate and extrapolate the s-parameter data to frequencies for which no data is provided. Like all circuit simulators, Nexxim uses a variable time-step algorithm. When necessary, the time step may be very small, requiring that the s-parameter model be extrapolated to very high frequency. The total simulation time (for example when many bits are included) may be very long, requiring fine resolution of the frequency samples.

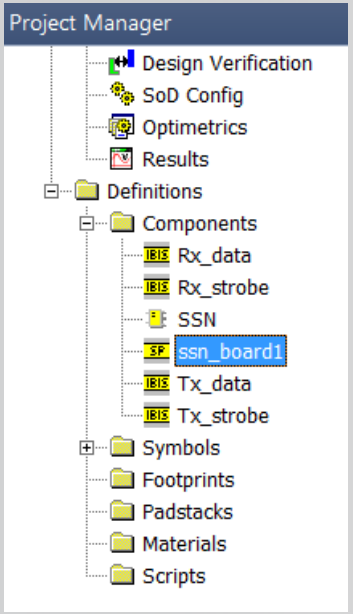


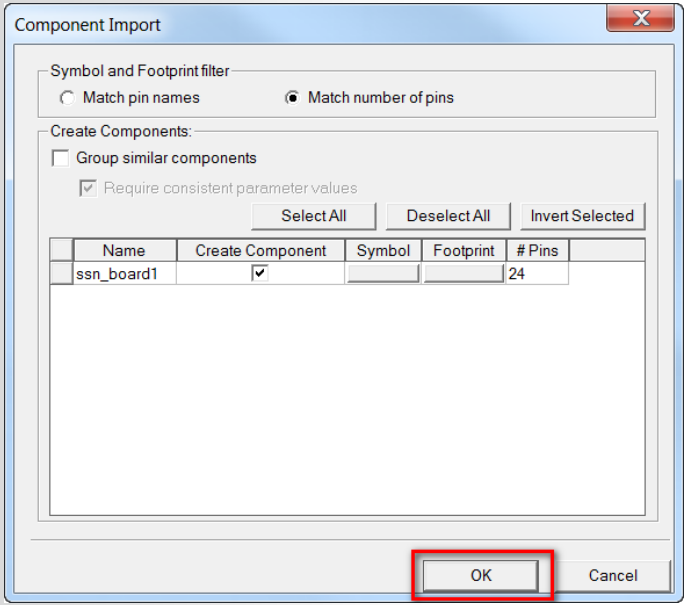
- Nexxim implements unique proprietary algorithms to insure the fidelity of the transient signals when s-parameter models are used in the simulation.

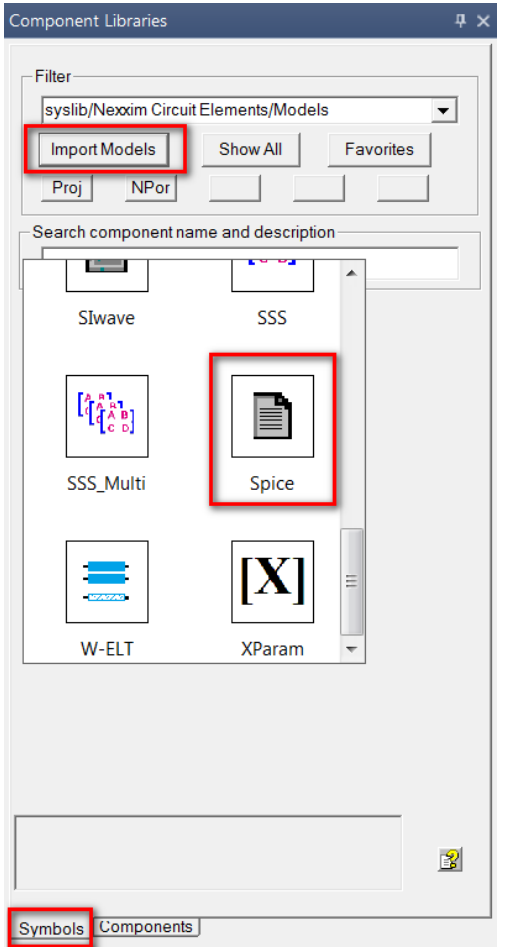
Import S-Element

- **Import S-Element**
  - The S-parameter data for this example was generated using 50 Ohm ports for signal lines and 1 Ohm ports for power planes. This is to ensure sufficient precision is available in the S-parameters for the power planes. ANSYS SIwave was used to generate the S-parameter data and exports a SPICE subcircuit containing the S-parameter data and the port characteristic impedances.
  - Go to the **Component Libraries window** and click on the button **Import Models**
  - In Select File window select **ssn_board1.sp** and press **Open**
  - Select **OK** and place the component on the schematic window
  - Now the component should be seen in the Project Manager window

Import S-Element

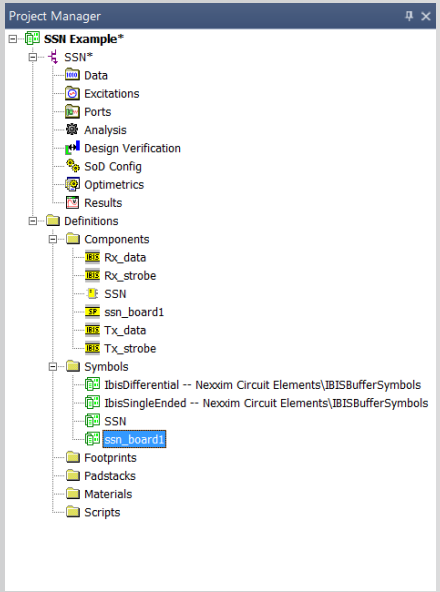


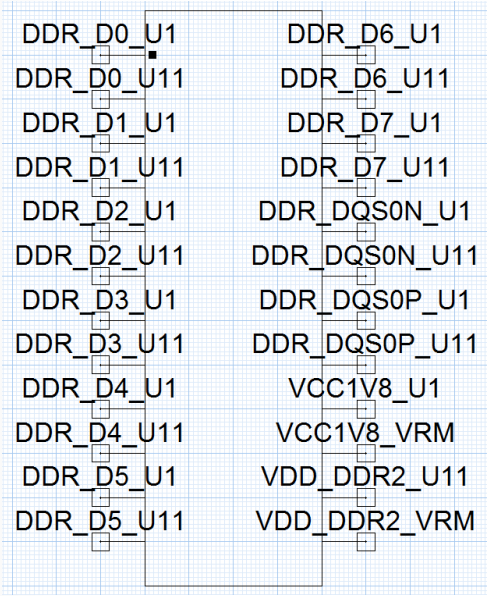




S-Element Symbol

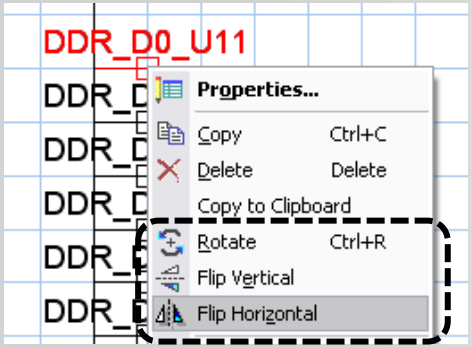
- **Edit S-Element Symbol**
  - In order to make the required connections easier to wire and simplify the resulting schematic, we will need to edit the S-element symbol. In the Project Manager, expand ***Definitions > Symbols*** and double-click on the ssn_board1 symbol entry. This will open the symbol in a symbol editor window in the main Designer SI window.

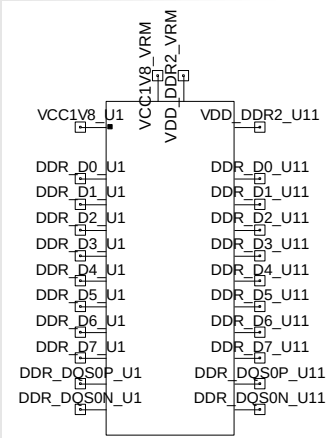


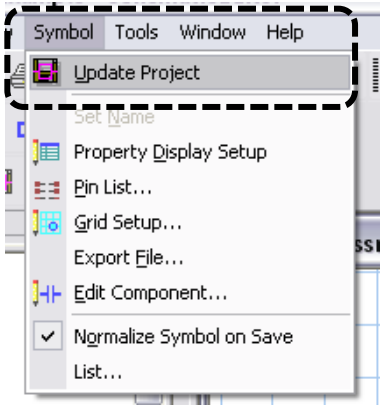


Modify S-Element Symbol

- You can edit the symbol by click-dragging the pins to rearrange them. Right-clicking on a pin and selecting **Flip Horizontal** will allow you to switch which side the pin will attach to. In addition, you can resize the main symbol block by selecting it and click-dragging the handles that appear on the sides and corners. Make the symbol look like this:



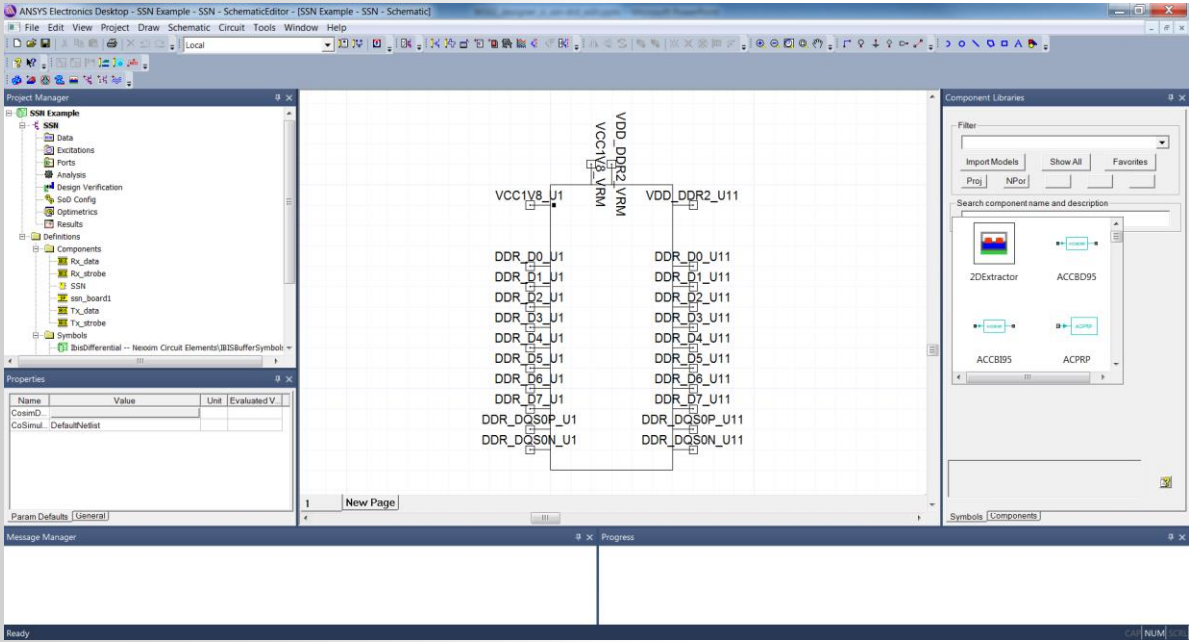




- Select the ***Symbol > Update Project*** menu item to save the changes to the symbol. Double-click on SSN in the Project Manager to return to the schematic.

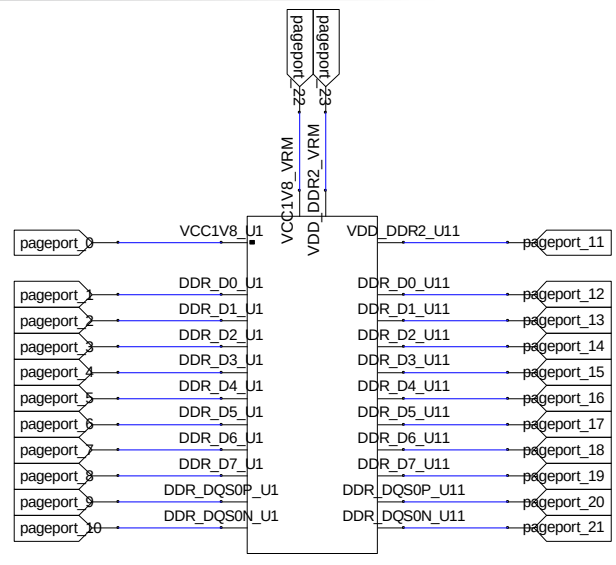
Modify S-Element Component

- **View S-Element Component**
  - Right-click on SSN in the Project Manager window to return to the main window



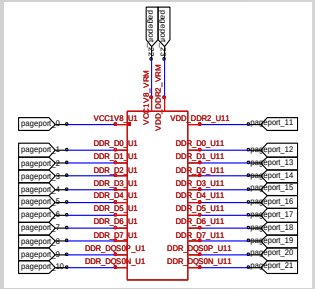
Add Page Connectors

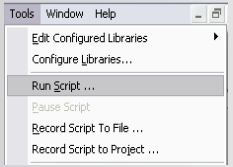
- **Add Page Connectors**
  - Select the ***Draw > Page Connector*** menu item or click the **Page Connector** toolbar icon and connect a page connector to each of the pins on the schematic. You can press the R key on the keyboard to rotate each page connector into the proper orientation before placing it. When finished, right-click in the schematic and select **Finish**. This will help simplify the schematic.

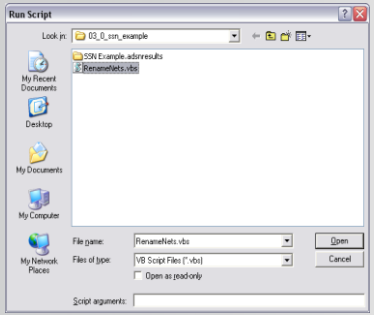


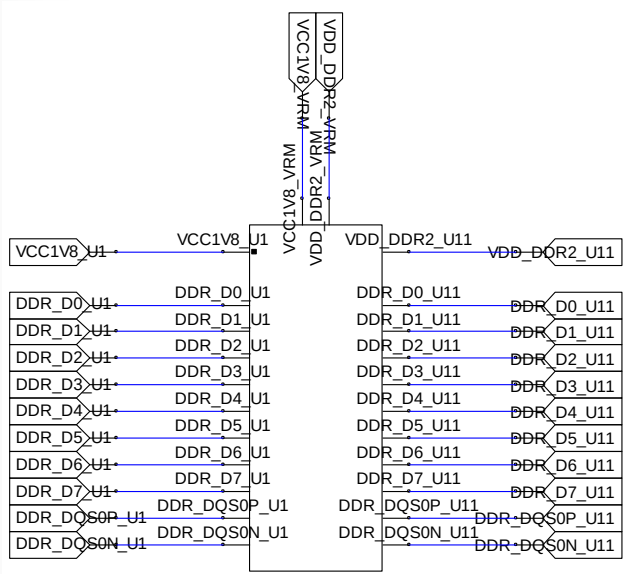
Rename Page Connectors

- **Rename Page Connectors**
  - The page connectors have default names that are not very descriptive. This exercise includes a script to automatically rename the page connectors to the names of the S-Element ports they are connected to. First, **select** the S-Element component in the schematic by clicking on it. Select the ***Tools > Run Script*** menu item, select file **RenameNets.vbs** and click **Open**. The page connectors will be renamed according to the S-Element port names.



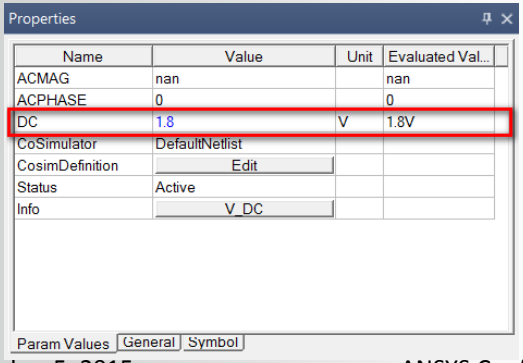


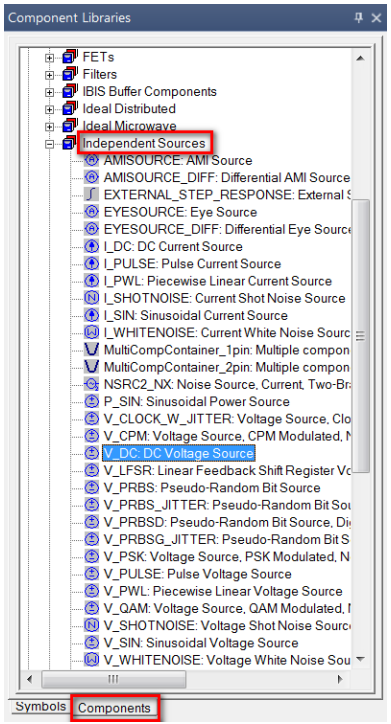




Add VRM

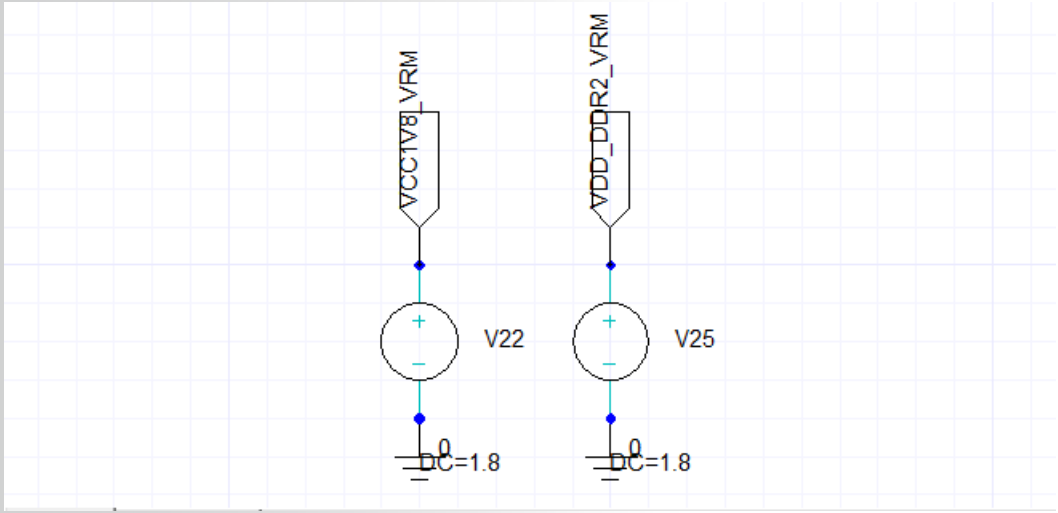
- **Create VRM Circuits**
  - We will need to add VRM models in order to provide power to the drivers through the power planes of the board. We will do this by attaching an ideal voltage source at 1.8 V to the **VCC18V_VRM** and **VDD_DDR2_VRM** ports on the S-element component.
  - Go to the **Component Libraries window** and click on the tab **Components**
  - Expand the **Independent Sources** menu and double click on **V_DC**
  - Place the component on the schematic
  - Click on the component to see its properties in the **Properties** window
  - Set **DC** parameter of component V_DC to **1.8V**
  - Right click on the source, select **Copy**
  - Right click on the schematic, select **Paste** to make a second copy of the source





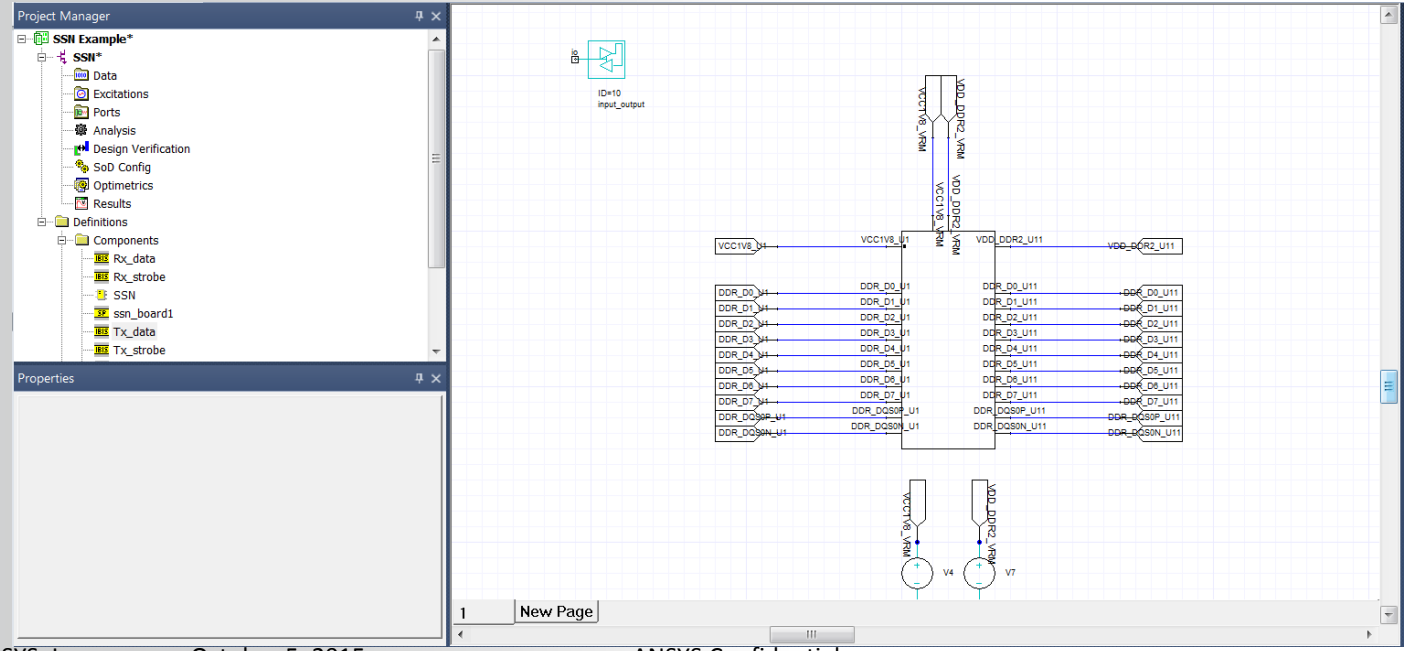
Connect VRM

- Add a ground and connect it to negative pin of the DC sources
- Copy and paste page port **VCC1V8_VRM** and connect it to the positive pin of the first DC source
- Copy and paste page port **VDD_DDR2_VRM** and connect it to the positive pin of the second DC source
- The two sources should now appear as shown below



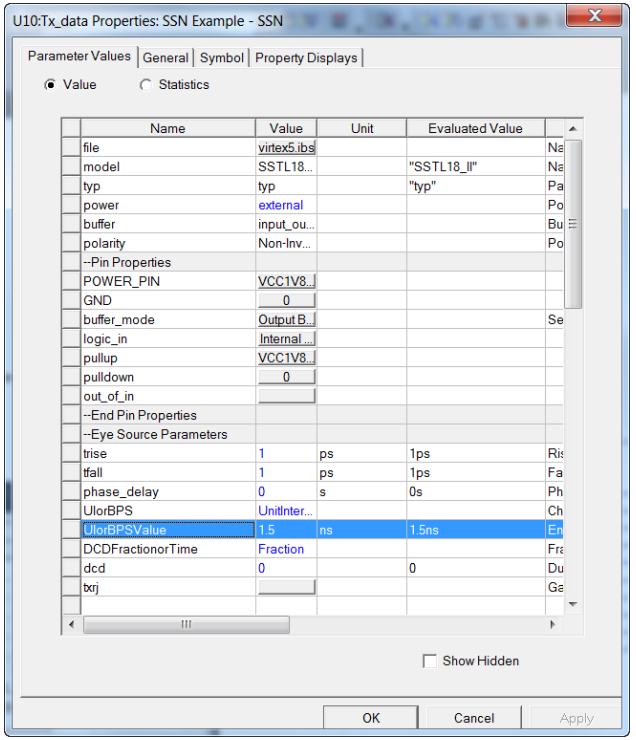
Place Components: Driver

- **Place Driver Components**
  - In the **Project Manager** from folder ***Definitions > Components*** left-click and drag the **Tx_data** component into the schematic and click to place a copy of the component. Right-click in the schematic and select **Finish** to stop placing components.



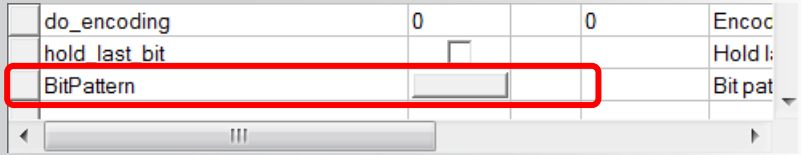
Configure the IBIS model

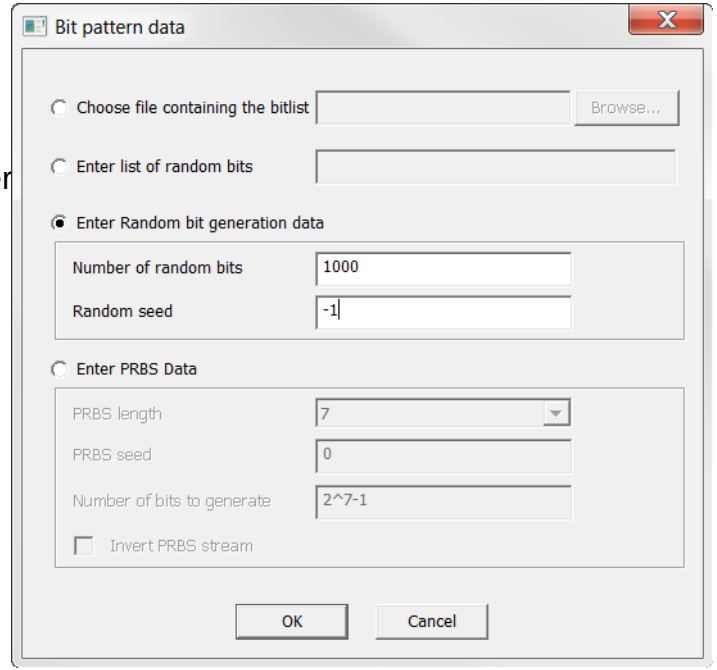
- **Configure the Driver**
  - Double click on the **Tx_data** driver that was placed on the schematic and configure the **Pin Properties** as follows:
    - Click on the grey button in the value field to assign the following nets to model:
      - **power: external**
      - **POWER_PIN: VCC1V8_U1**
      - **GND: 0**
      - **buffer_mode : Output Buffer**
      - **pullup : VCC1V8_U1**
      - **pulldown : 0**
      - Leave the **logic_in** as **Internal Source**
      - **trise: 1ps**
      - **tfall: 1ps**
      - **UI: 1.5ns**
    - Continued on next page



Configure the IBIS model

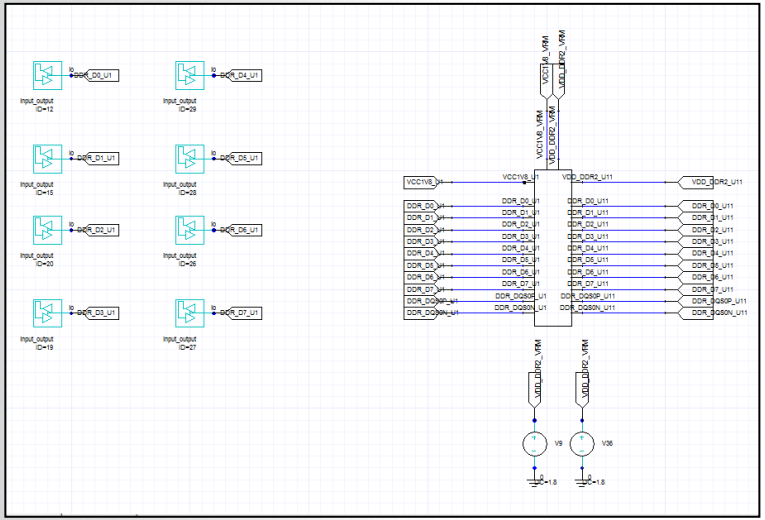
- **Configure the Driver**
  - Next we will configure the bit pattern for the IBIS driver
    - Click on the grey box next to the **BitPattern Property**
      - **Select Random bit generation**
      - **Number of random bits: 1000**
      - **Random Seed: -1**
    - A Random Seed of -1 will provide a unique bit pattern for each driver
    - Click **OK** twice to exit both forms





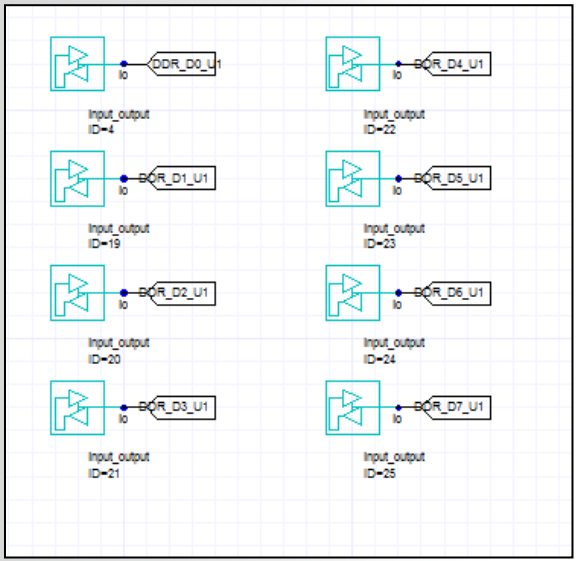
Create Driver Copies

- Select the **SSLT18_II_virtex5** driver element that was placed in the schematic earlier and select the following menu item: **Edit > Copy.**
- Click anywhere in empty schematic space to unselect the driver.
- Select **Edit > Paste** and repeat until 7 more drivers have been placed on the schematic.
  - **Note:** It may be necessary to move the drivers to create an orderly schematic, also the driver can be rotated using **Ctrl + r** to position the parts in the desired location and orientation.
- The schematic should look like the image below when finished.



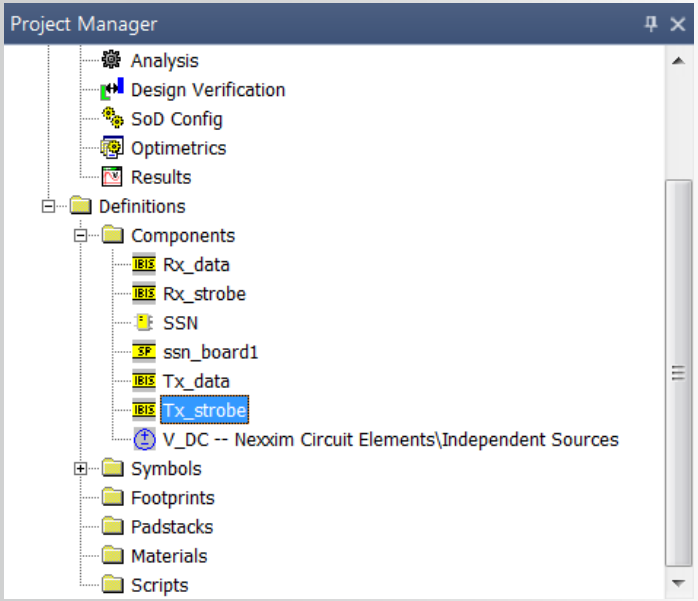
Connect the Drivers

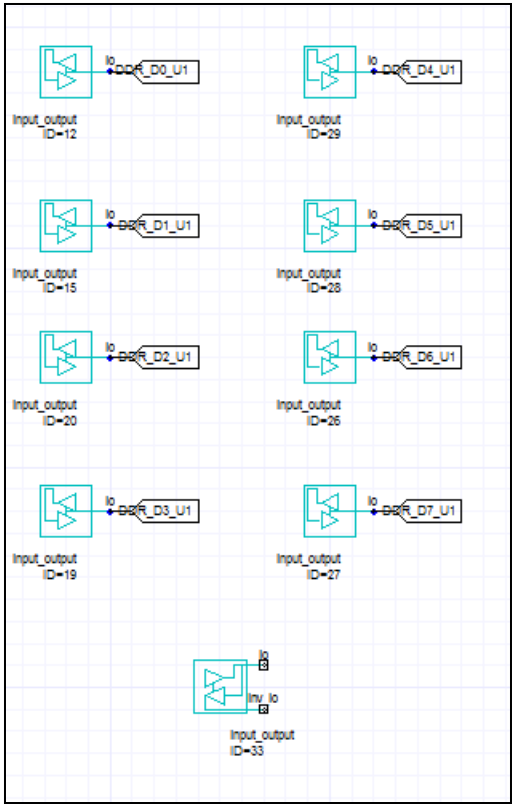
- The next step is to connect the output of the driver to proper ports on the **ssn_board1** symbol.
- Copy each of the **Page Connectors: DDR_D0_U1** through **DDR_D7_U1** and connect the copy to one of the available drivers.
  - An easy way to do this is to hold down the **Ctrl** button and click on the symbol that needs to be copied and will holding the **Ctrl and Left Mouse Button** drag the object to make a copy.
  - Once the copy has been made it can be rotated and connected to the appropriate driver.



Add Differential Strobe Driver

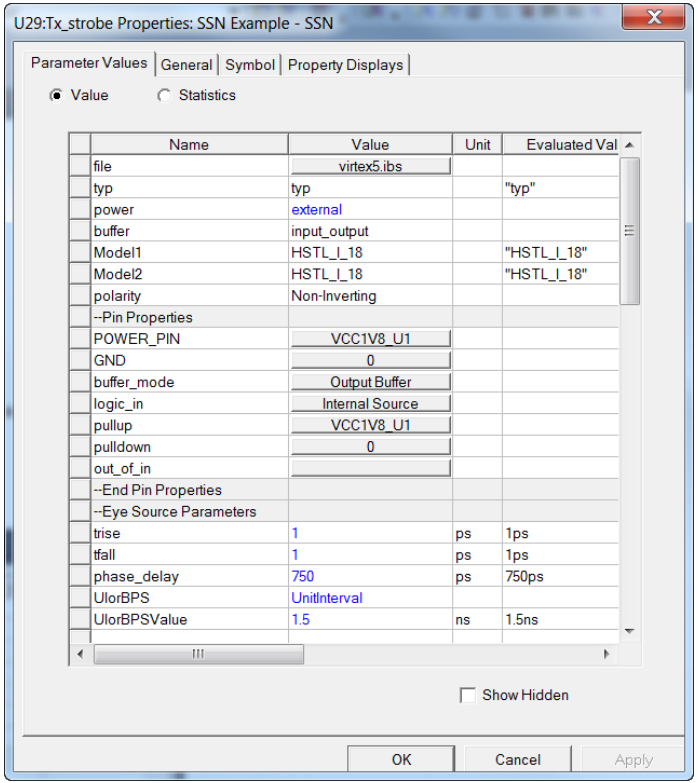
- **Create Strobe Driver Circuit**
  - Select the differential IBIS model **Tx_strobe**
  - Place it on the schematic below the single ended driver

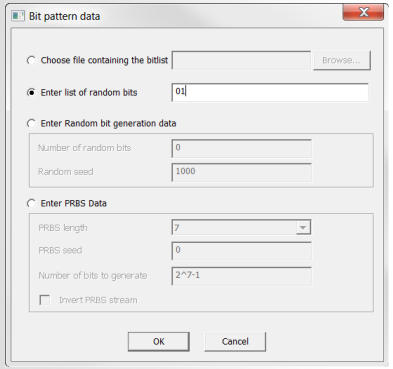




Differential Strobe Driver Setup

- **Create Strobe Driver Circuit (Continued)**
  - Set the IBIS strobe properties as follows
    - **power:** external
    - **POWER_PIN/pullup: VCC1V8_U1**
    - **GND/pulldown: 0**
    - **trise/tfall**: 1 ps
    - **Phase_delay:** 750 ps (½ bit period)
    - **UI:** 1.5ns
  - Click the grey box next to **Bit Pattern**
    - Select the option for “list of random bits”
    - Enter “**01**”
- Click **OK** twice to exit both forms

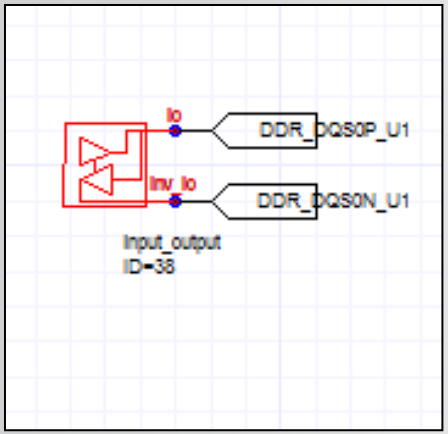


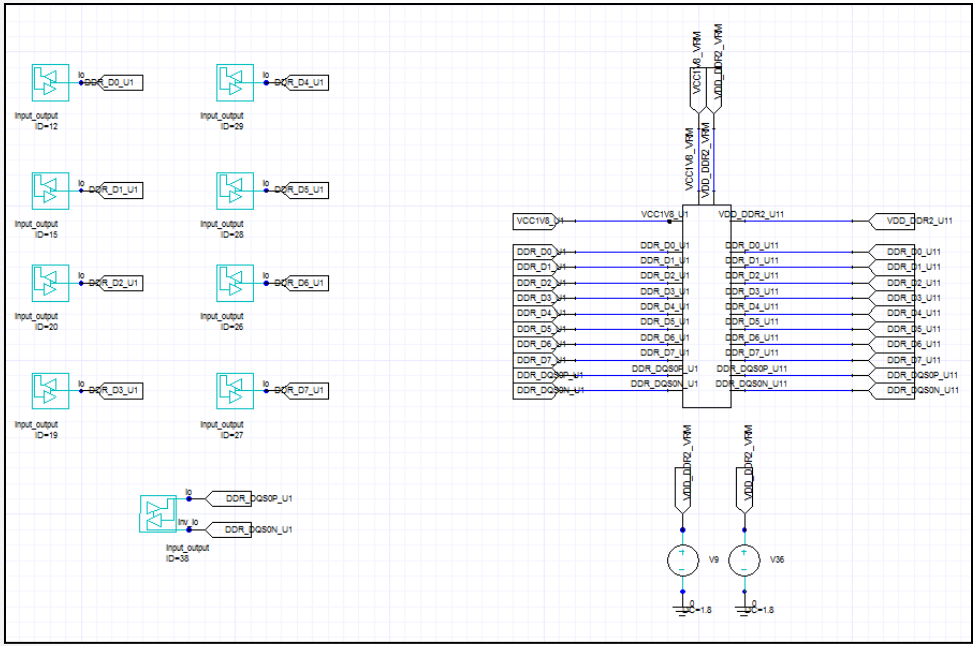


Connect Strobe Driver

- **Create Strobe Driver Circuit (Continued)**
  - Copy the below page ports from the s-parameter components and connect them as shown on the right
    - **DDR_DQS0P_U1**
    - **DDR_DQS0N_U1**

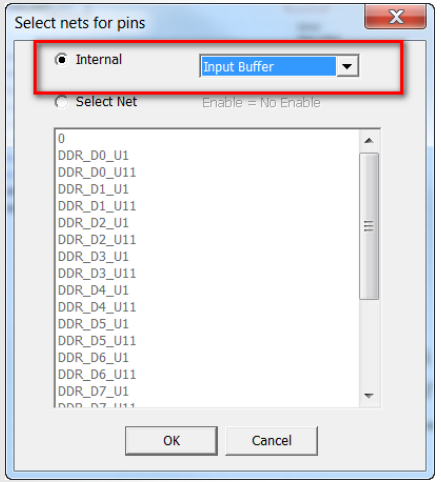
- The full circuit should now appear as here

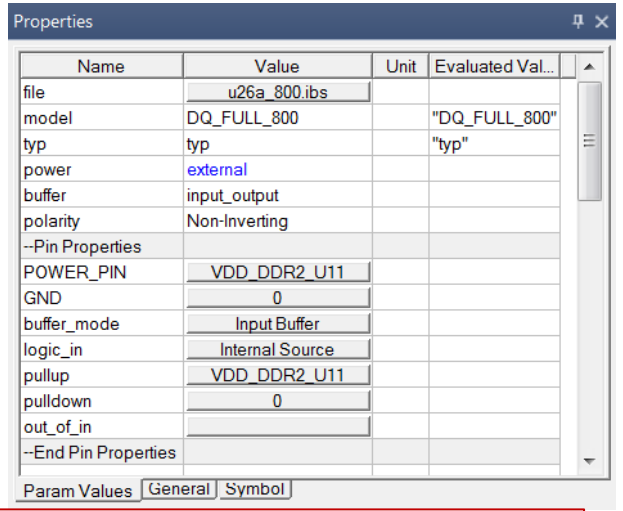




Receiver

- **Create Receiver Circuits**
  - Using the same techniques as before, we can create a receiver circuit using the DQ_u26a_800 (data line) and DQS#_u26a_800 (strobe) components. Place eight **Rx_data** components and one **Rx_strobe** component onto the schematic.
  - Select all of the reciever components by windowing around the group.
  - Change the following settings:
    - **power : external**
    - **POWER_PIN : VDD_DDR2_U11**
    - **GND : 0**
    - **buffer_mode : Input Buffer**
    - **pullup : VDD_DDR2_U11**
    - **pulldown : 0**

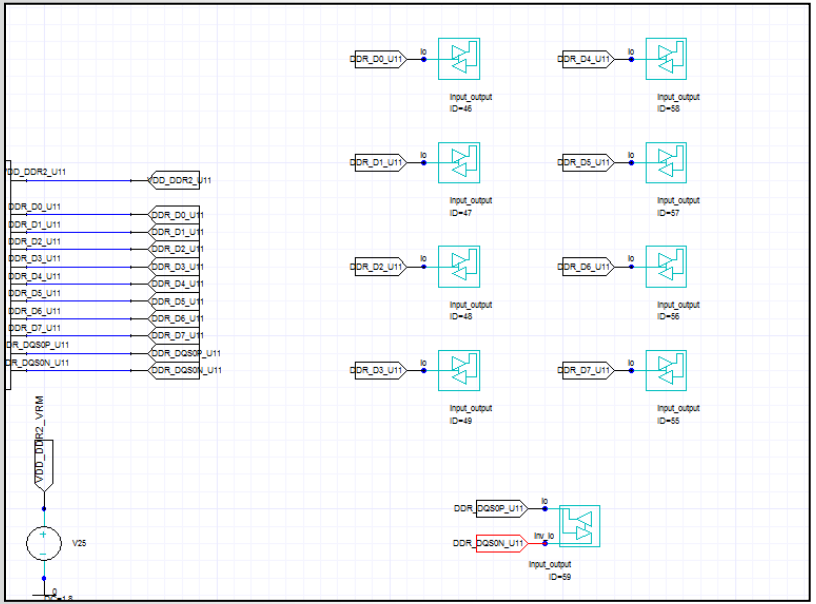




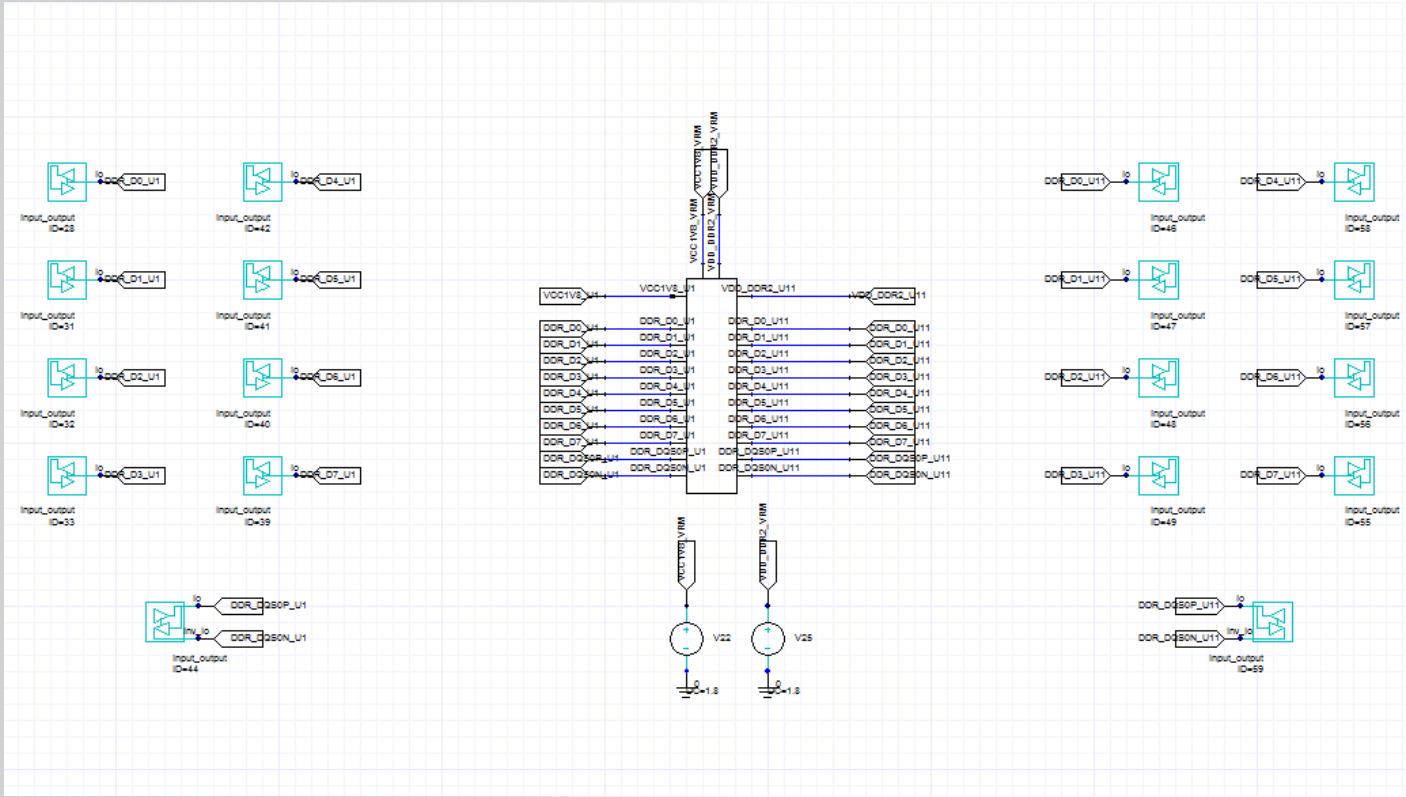
The input buffer models have utilize an IBIS model selector in order to specify different termination schemes. By default they are set to “DQ_FULL_800” with disabled ODT.

Receiver

- Now that the input buffers have been created it is time to assign the input signals to the buffers.
- Select all of the **Page Connectors** on the right side of the **ssn_board1** component, except **VDD_DD2_U11,** and copy and paste them onto an open area of the schematic.
- Take each of the **Page Connectors** and connect them to a receiver model as shown below. Make sure that the DQS models are connected to the correct **Page Connectors.**

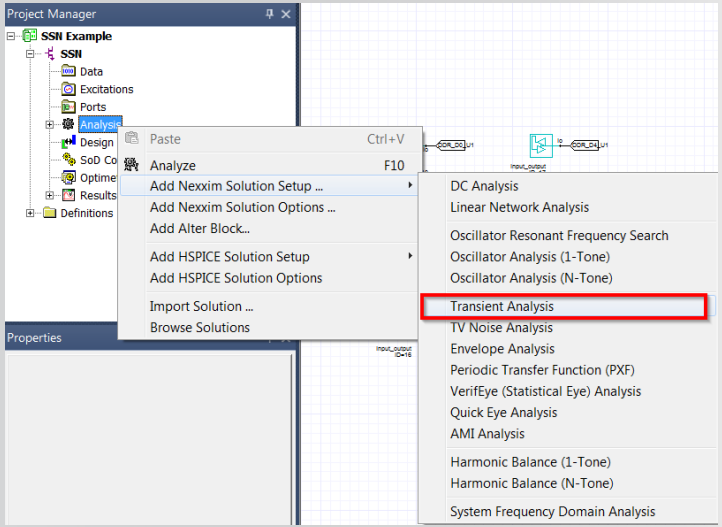


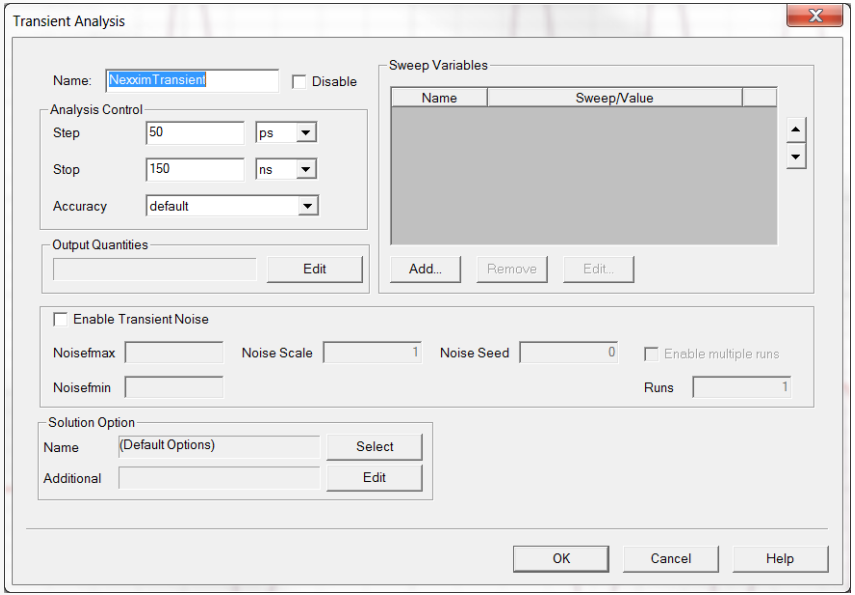
Final Schematic



Add Transient Analysis

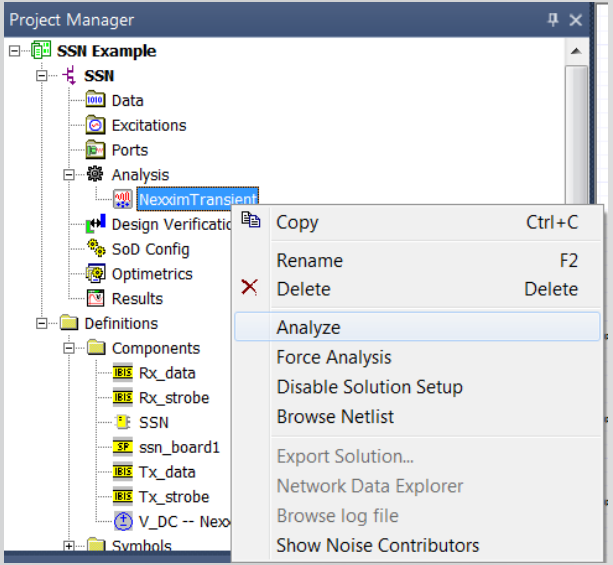
- **Transient Simulation Setup**
  - To add a transient simulation setup, right-click on **Analysis** under **SSN Example > SSN** in the Project Manager and select ***Add Neximm Solution Setup > Transient Analysis***. Set up a step time of 50 ps and a stop time of 150 ns. This will run 100 bits through the lines. Click **OK** to save the transient setup.

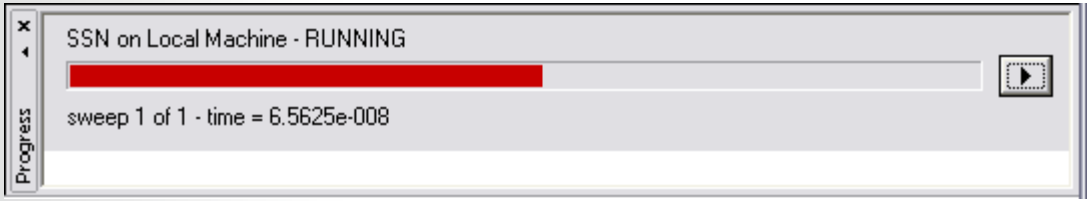


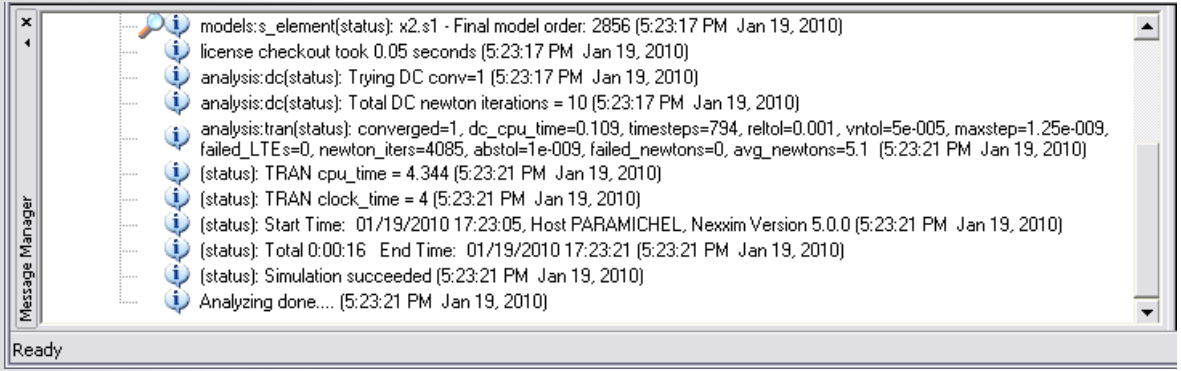


Run Analysis

- **Run Transient Simulation**
  - In the **Project Manager** under ***SSN Example > SSN > Analysis***, right-click on **Transient** and select **Analyze** to begin the transient simulation. A progress bar will appear in the Progress window and messages about the simulation will appear in the Message Manager.

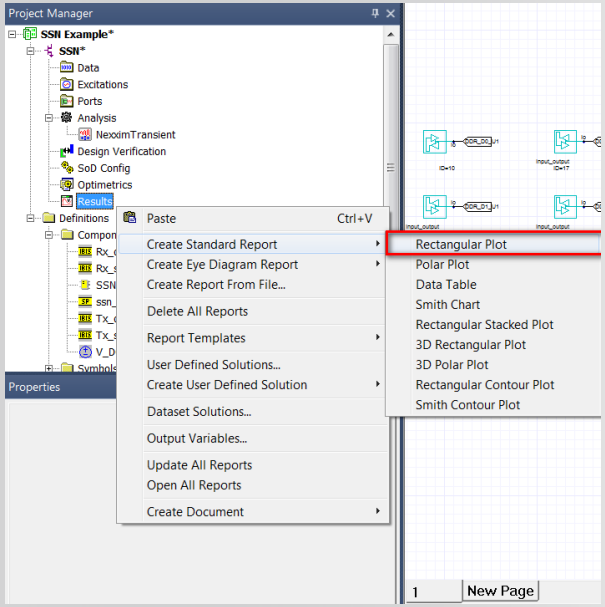


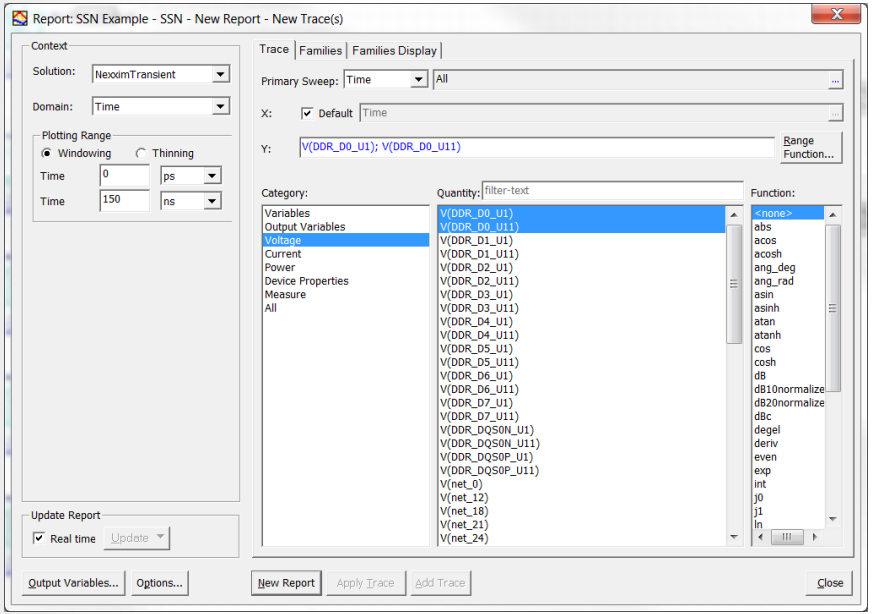




Create Plot

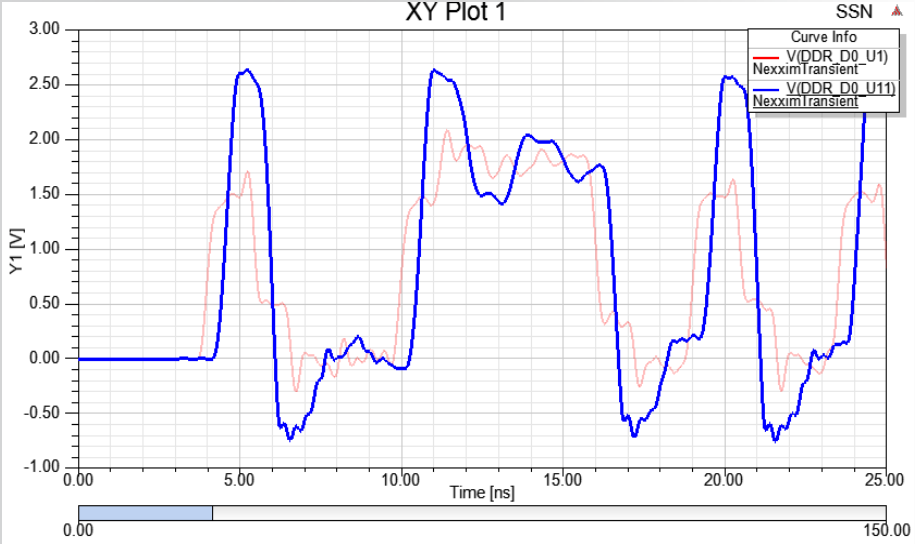
- **Create Time-Voltage Report**
  - When the simulation is finished, right-click on **Results** in the **Project Manager** under ***SSN Example > SSN*** and select ***Create Standard Report > Rectangular Plot***. In the New Report dialog box, select **Voltage** under **Category** and **V(DDR_D0_U1)** and **V(DDR_D0_U11)** under **Quantity**. Click **New Report** to create the plot and **Close** to close the dialog.

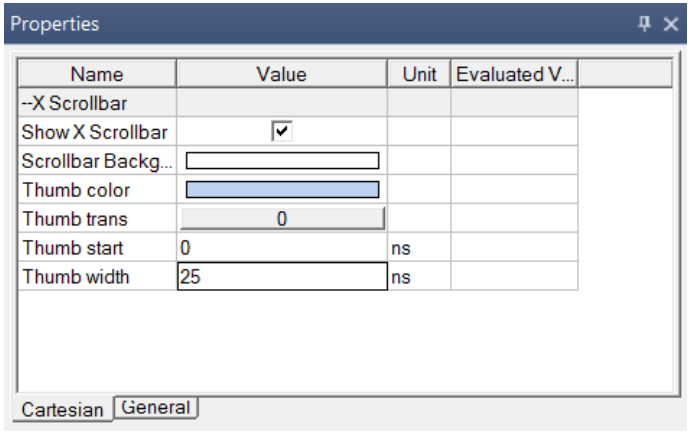




View Plot

– In the plot window that appears, click in the background of the plot and then check the **Show X Scrollbar** checkbox in the properties window. Set the **Thumb width** property to 25 ns.





When ODT was disabled, the receiver has extremely large overshoot/undershoot due to reflection.

Report Editor

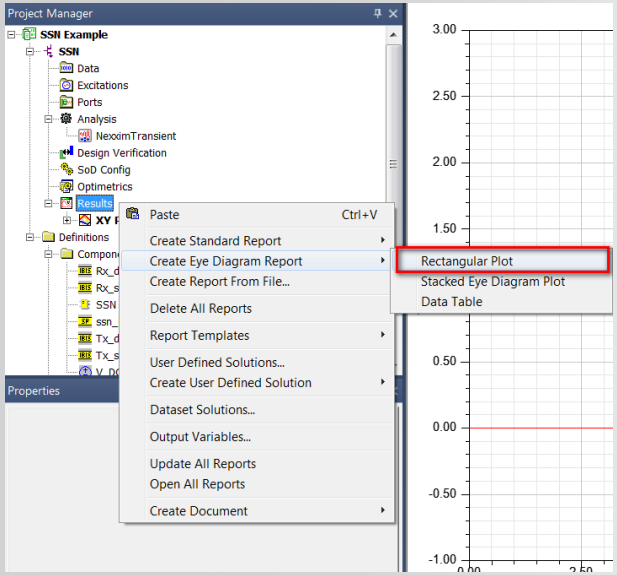
- **Report Editor Dialog Details**
  - **Context**
    - *Solution* – if the design has multiple analysis setups, select the desired analysis
    - *Domain* – plotting in different domains are available depending on the solution, including frequency domain, time domain, and sweep domain.
  - **Update Report**
    - *Real Time checked* – enable real time updates for all reports, otherwise traces are updated to latest data available when you click **Update > Update This/All Reports** or after solution is completely finished
  - **Trace Tab**
    - *X (Primary Sweep) section* – this contains a dropdown menu for selecting the value(s) and a browse button for selecting from a list of the swept values for the selected primary variable.

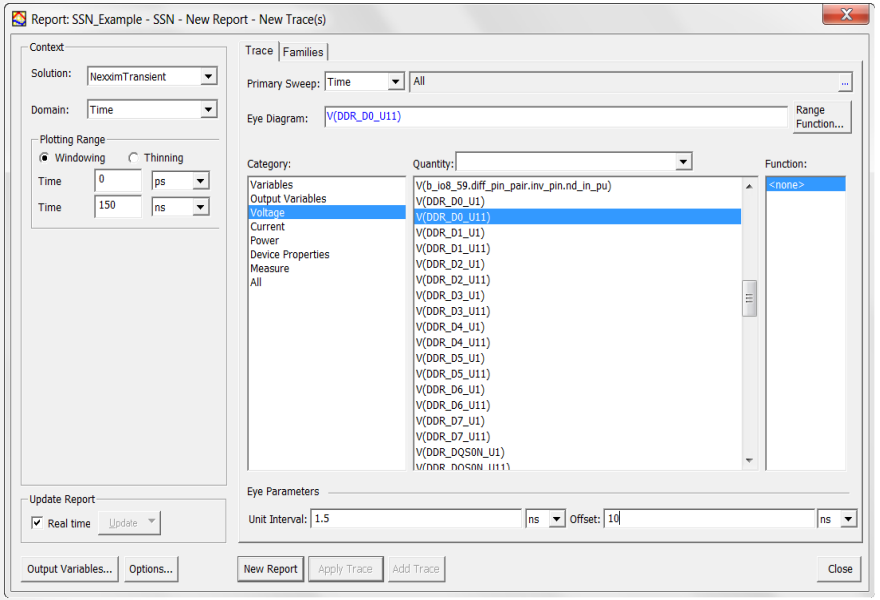
Report Editor

- **Report Editor Dialog Details**
  - **Trace Tab**
    - *Y section*
      - *Category* – these depend on the solution type and the design and lets you specify the category of information for the Y component.
      - *Quantity* – quantity to plot on the Y axis; these will vary by the category selected.
      - *Function* – function to apply to selected quantity when plotting.
      - *Y* value field displays the currently selected quantity and function.
      - **Range function** – opens the Set Range Function dialog that allows the calculation of minimum, maximum, and other derived quantities from the plotted data; for example, if a sweep of a W-element length variable was simulated, the maximum loss at any frequency could be plotted versus the W-element length.
  - **Families Tab**
    - Used to select which variations of a parameter sweep other than frequency you would like to include in a plot; this allows easy creation of a single plot containing traces with one or more variations of the swept variables

Create Eye Diagram Plot

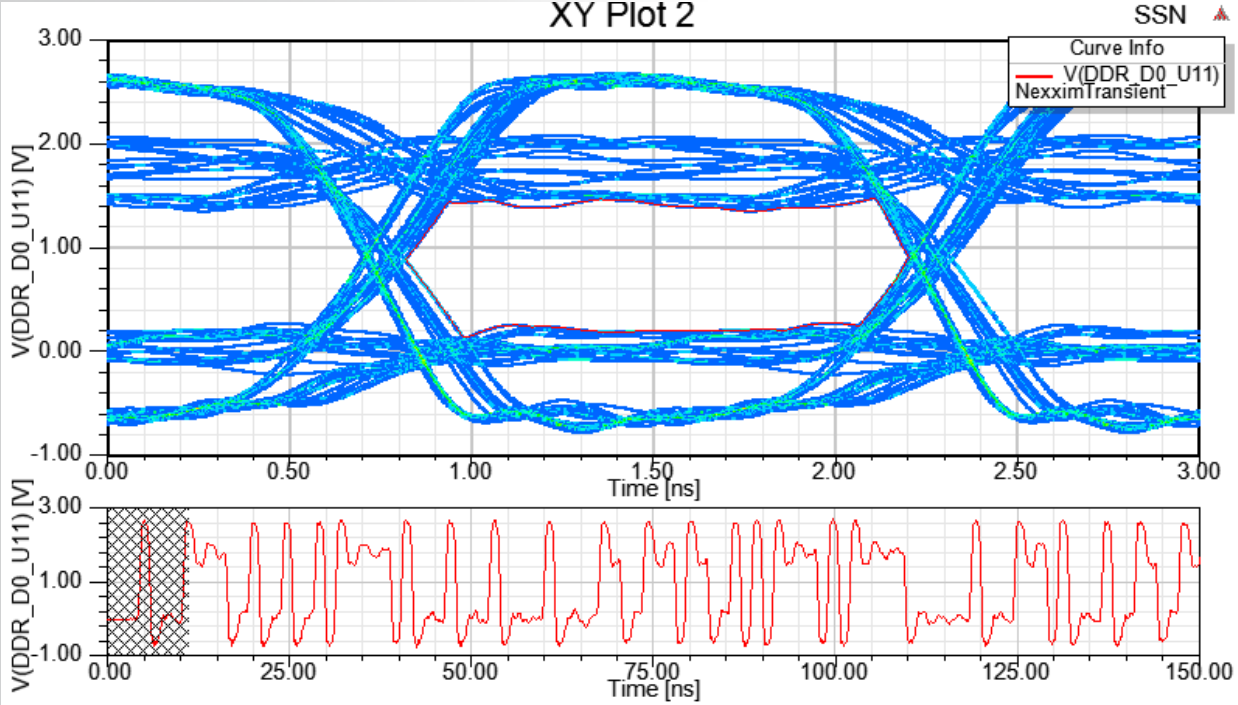
- **Create Eye Diagram Report**
  - Right-click on **Results** in the **Project Manager** under ***SSN Example > SSN*** and select ***Create Eye Diagram Report > Rectangular Plot***. In the New Report dialog box, select Voltage under **Category** and **V(DDR_D0_U11)** under **Quantity**. Enter **1.5 ns** in the **Unit Interval** text box for 667Mbps. Set the **Offset** box to 10ns to ignore and initial transient behavior. Click **New Report** to create the plot and **Close** to close the dialog.





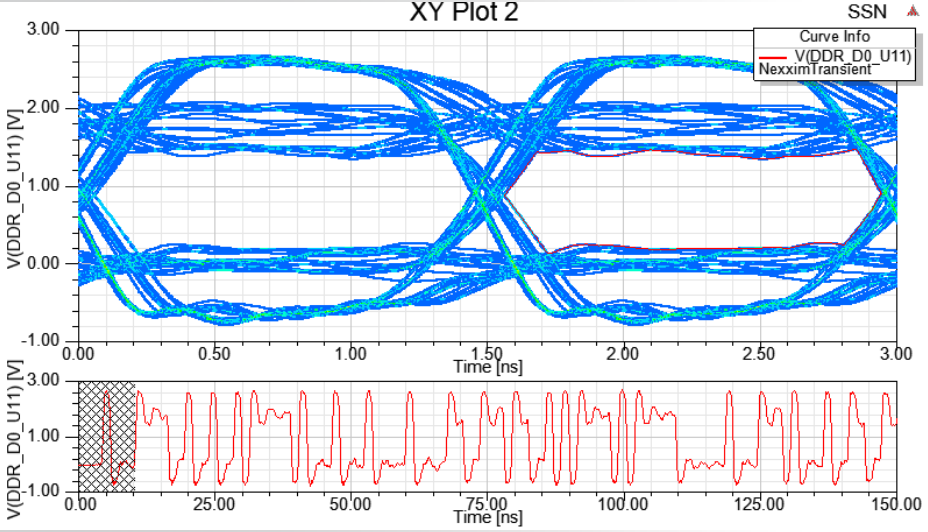
View Eye Diagram Plot

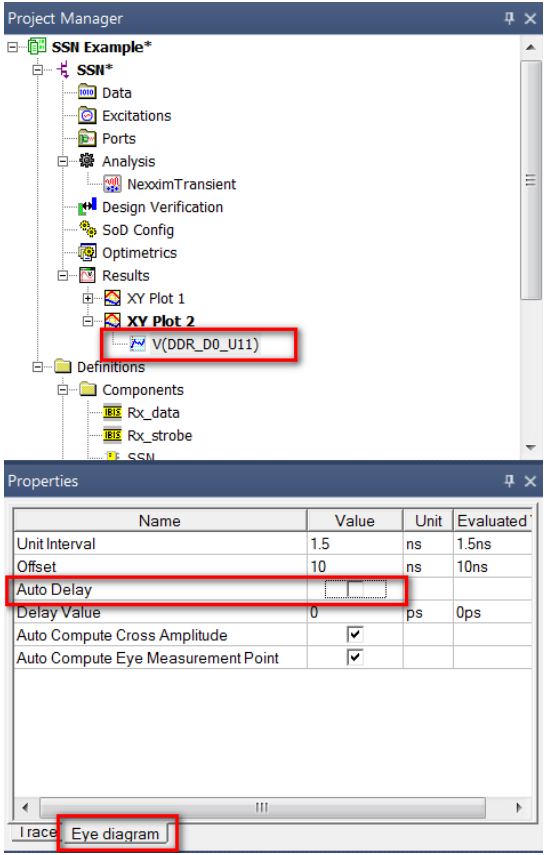
- This eye diagram shows the effect of nearby lines switching but is fairly clean. We can also check the timing of this line with respect to the strobe by overlaying the strobe eye over the data eye.



View Eye Diagram Plot

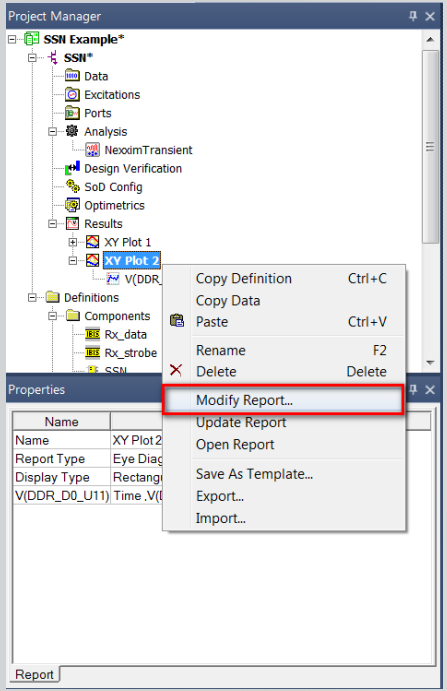
- The first step in overlaying the two plots is to turn off the **Auto Delay** feature.
- Click on the following in the **Project Manager:**
  - **SSN Example > SSN > Results > XY Plot 2 > V(DDR_DO_U11)**
- In the **Properties** explorer select the **Eye Diagram** tab
- Unselect the **Auto Delay** check box.
- Notice that the eye is no longer centered

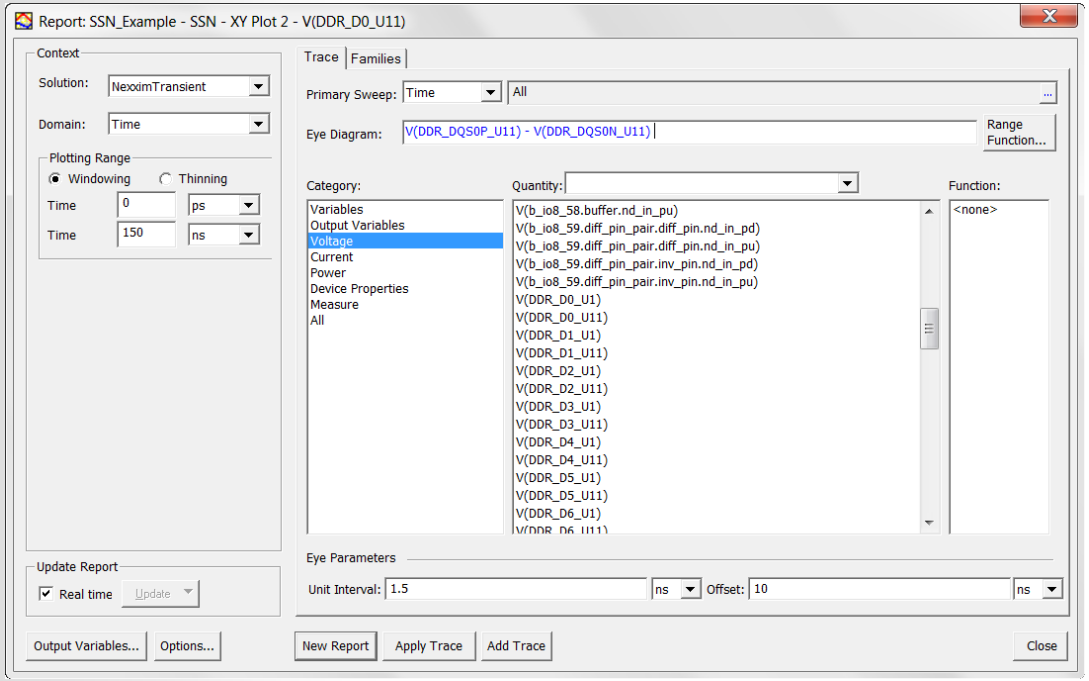




Create Strobe Eye

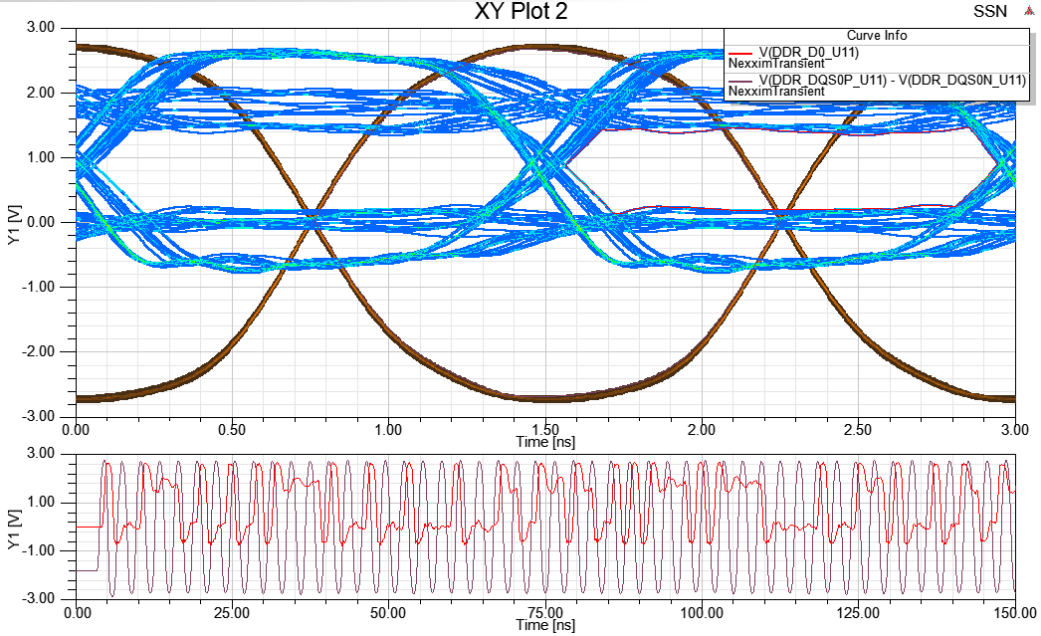
– Right-click on **XY Plot 2** in the **Project Manager** under ***SSN Example > SSN > Results*** and select **Modify Report**. In the New Report dialog box, select Voltage under **Category** and enter **V(DDR_DQS0P_U11) - V(DDR_DQS0N_U11)** in the **Eye Diagram** text box. Click **Add Trace** to create the plot and **Close** to close the dialog.





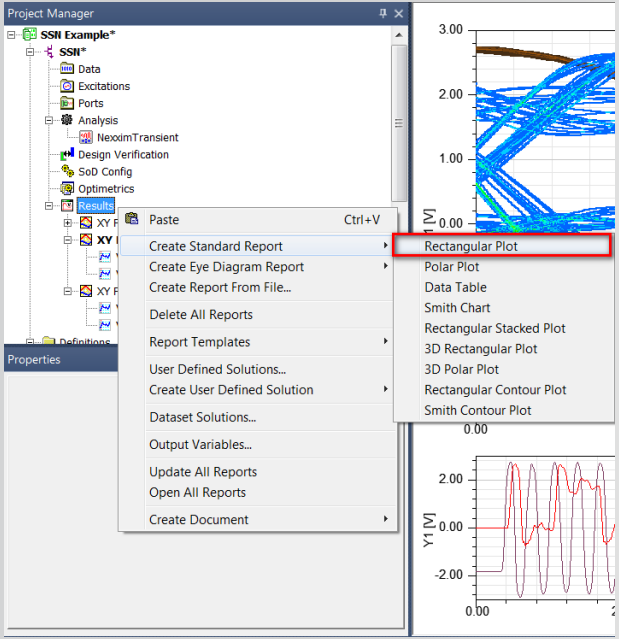
Compare Eye from Data and Strobe

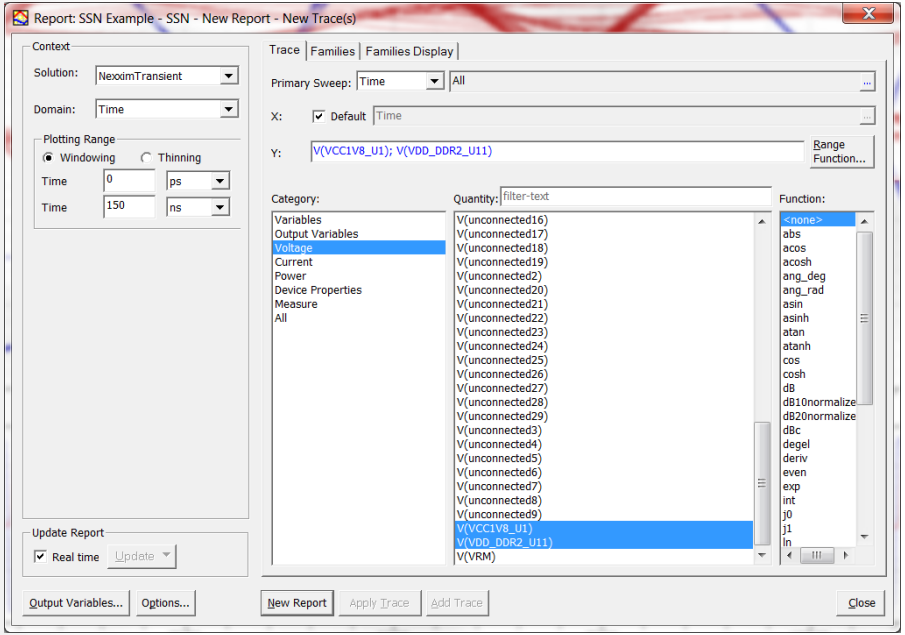
- Note that the strobe edge appears in the middle of the data eye, indicating that we will be clocking data correctly. A more detailed analysis of this plot would be possible to determine setup and hold margins.
- Change the **Colormap** of the second plot by clicking on the waveform and changing the **Colormap Type** to **Ramp** , this will allow for better distinction between the two wave forms.



Power Noise Report

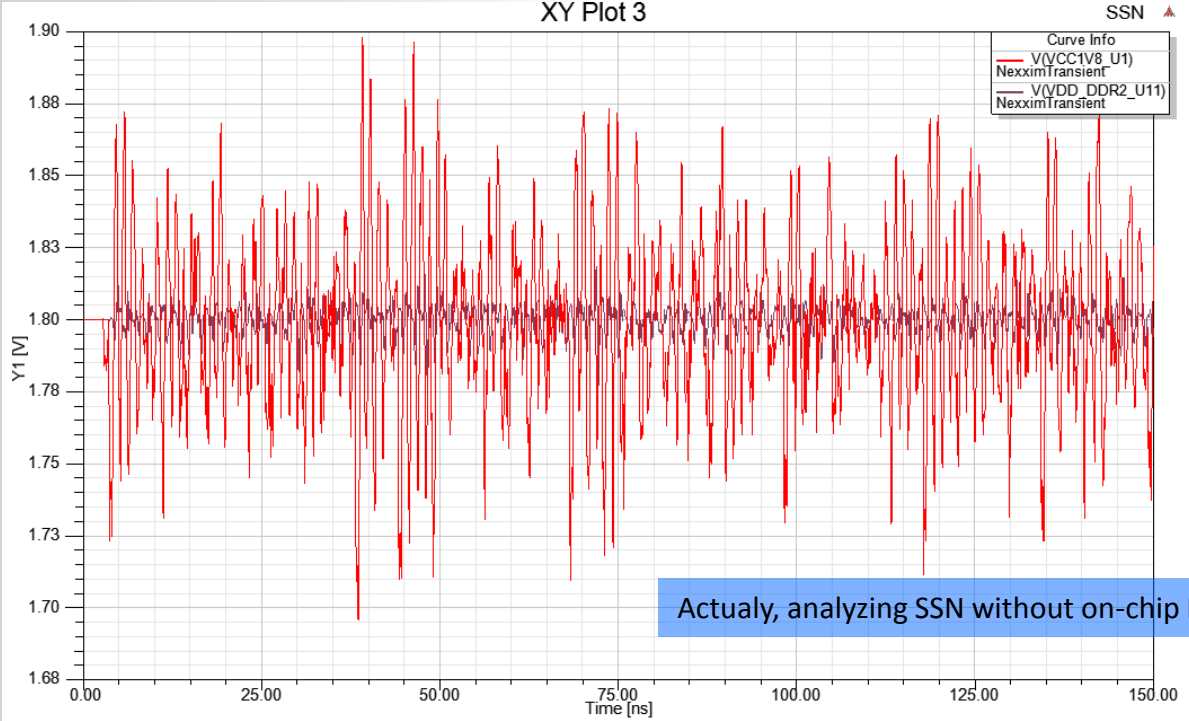
- **Create Power Noise Report**
  - Right-click on **Results** in the **Project Manager** under ***SSN Example > SSN*** and select ***Create Standard Report > Rectangular Plot***. In the New Report dialog box, select Voltage under **Category** and **V(VCC18V_U1)** and **V(VDD_DDR2_U11)** under **Quantity**. Click **New Report** to create the plot and **Close** to close the dialog.





View Power Noise Plot

- This plot shows the noise that appears at the power inputs of the active devices **U1** and **U11** where the drivers and receivers are drawing current as they switch.



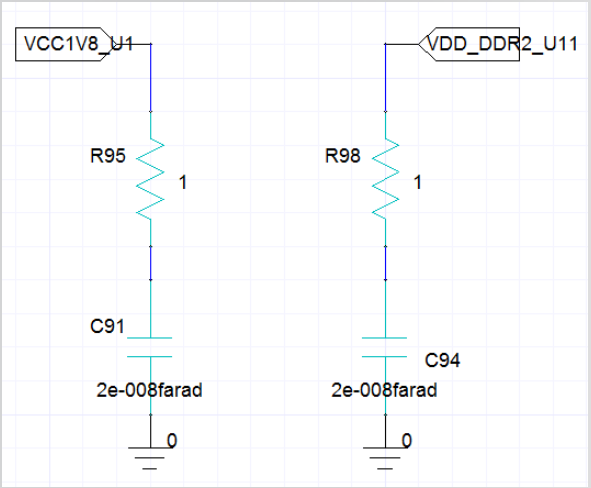
Challenge

#1. For 667Mbps write operation, use “DQ_FULL_ODT50_800” for all input buffers at U11(DDR2 Memory). this can be manipulated by model selector GUI in symbol. Note that you will have to change both **model1** and **model2** for the differential strobe input

And capture the voltage waveform of “D0” at U11 from 0nsec to 25nsec.

Challenge Cont’

#2. For #1, Add 20nF capacitor and 1 Ohm resistor at the both power of U1 and U11 as below schematic. (these mean two simple on-chip PDNs for each ICs.) in this case, how much is the maximum SSN from U1? Capture the screen shot from your report.



Stacked Plot