1. General description of the project:

The purpose of this project is to design one prototype satellite which will be part of a much larger network of such devices, placed temporarily on earth's orbit, for close monitoring of the permafrost (in and around the Arctic and Antarctic regions).

The schematic of the proposed project is indicated in ***Annex_1.***

The system description is as following:

In order to perform its main function, that of sequential photography, this device is using an ultra-high resolution, 71 Megapixels CMOS image sensor. This sensor will acquire 3 frames/second, every 6 hours, in order to completely capture one full seasonal climate cycle. The device is made up from the following components:

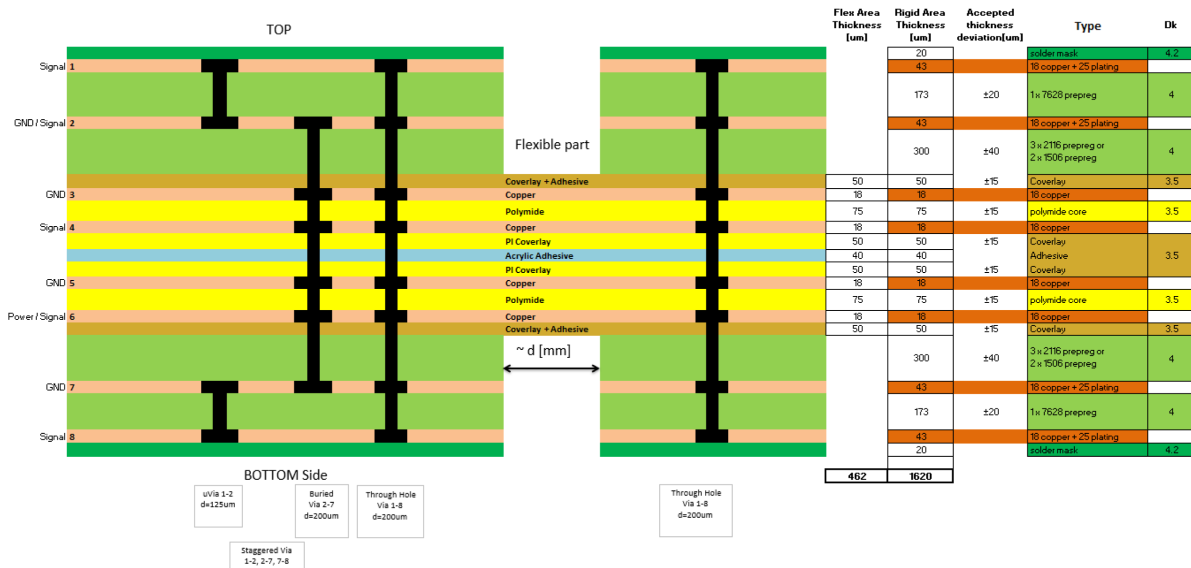
- The 71 megapixel CMOS image sensor. This component will be used at it's technological limit, to aquire 3 frames per second, in order to filter the noise per photo as much as possible (images will be processed locally and only one will be stored).
- In order to properly manage all the information which is fed via the image sensor, the chosen processing unit will be a **system-on-module (SoM)** IMX6-CPU has the following specifications:

  -528MHz NXP i.MX 6UL/6ULL ARM Cortex-A7 Processors
  - 512MB DDR3 SDRAM
  - 256MB Nand Flash (4GB eMMC Flash is optional)
  - Ready-to-Run Linux 4.1.15

- One **RadioFrequency(RF)** module used for high frequency communications. The satellite constellation will be comprised of 20 satellites which will be linked all together.
- One **Power Management IC(PMIC)**, will handle all the necessary energetic distribution needs.
- Due to recyclability reasons, easy handling and fast access, the satellite was designed to permit access to its internal data storage device (***eMMC***) from someone/something directly in outer space (most probably with ISS) for data management. The link to the data lines will be handled via an adapter tool connecting directly to one cluster of test points.

2. General requirements:

GEN-001	The design order is mandatory: libraries, schematic design, transfer procedure, layout design and postprocessing activities.
GEN-002	All dimensions shall be considered in mm.



Flex Area Thickness [um]	Rigid Area Thickness [um]	Accepted thickness deviation[um]	Type	Dk
	20		solder mask	4.2
	43		18 copper + 25 plating	
	173	±20	1x 7628 prepreg	4
	43		18 copper + 25 plating	
	300	±40	3 x 2116 prepreg or 2 x 1506 prepreg	4
50	50	±15	Coverlay	3.5
18	18		18 copper	
75	75	±15	polymide core	3.5
18	18		18 copper	
50	50	±15	Coverlay	3.5
40	40		Adhesive	
50	50	±15	Coverlay	
18	18		18 copper	
75	75	±15	polymide core	3.5
18	18		18 copper	
50	50	±15	Coverlay	3.5
	300	±40	3 x 2116 prepreg or 2 x 1506 prepreg	4
	43		18 copper + 25 plating	
	173	±20	1x 7628 prepreg	4
	43		18 copper + 25 plating	
	20		solder mask	4.2
462	**1620**			

Figure 1. Proposed stack-up definition for the thermal monitoring system.

Due to the complexity of this monitoring unit, and the geometry of the housing, the unit must be designed using one ***rigid-flex PCB***. It contains ***5 rigid sides*** named intuitively **A, B, C, D** and **E**. Each one of these sides has its specific constraints and placement requirements. See ***Annex_2*** and ***Annex_3***.

3. Schematic design specifications:

SCH-001	The schematic project will be created using any CAD system accepted in the contest (and respects all the minimum requirements published on the TIE official website).
SCH-002	The required components will be created in a new library named **TIE2019**.
SCH-003	The schematic must be drawn in a clear manner, e.g.: all references and values must have proper size and orientation, un-necessary crossings shall be avoided, no overlap of texts, graphical elements and electrical objects is allowed.
SCH-004	The schematic must be electrically correct, clean and readable. All reference designators must ***strictly*** follow ***Annex_1***. The main purpose is to generate a correct netlist for PCB design, but it must also provide a clear representation of functionality.
SCH-005	Test pads must be placed on the following nets (2 test pad per net): ***+V_SMPS_1V8, +V_SMPS_3V3, +V_LDO_RF_3V3, +V_IN*** and ***GND.*** ***Testpoints will be placed also on the high speed lines connecting the eMMC to the iMX-6 system on module (eMMC_CMD, eMMC_RST, eMMC_CLK, eMMC_DS, eMMC_DATA0..7).***
SCH-006	Following completion of the schematic, a ***Bill of Material (BOM)*** must be generated in following formats: **.xlsx .pdf .txt .csv**.
SCH-007	The same page size shall be used as the one received in ***Annex_1***.

4. Layout design specifications:

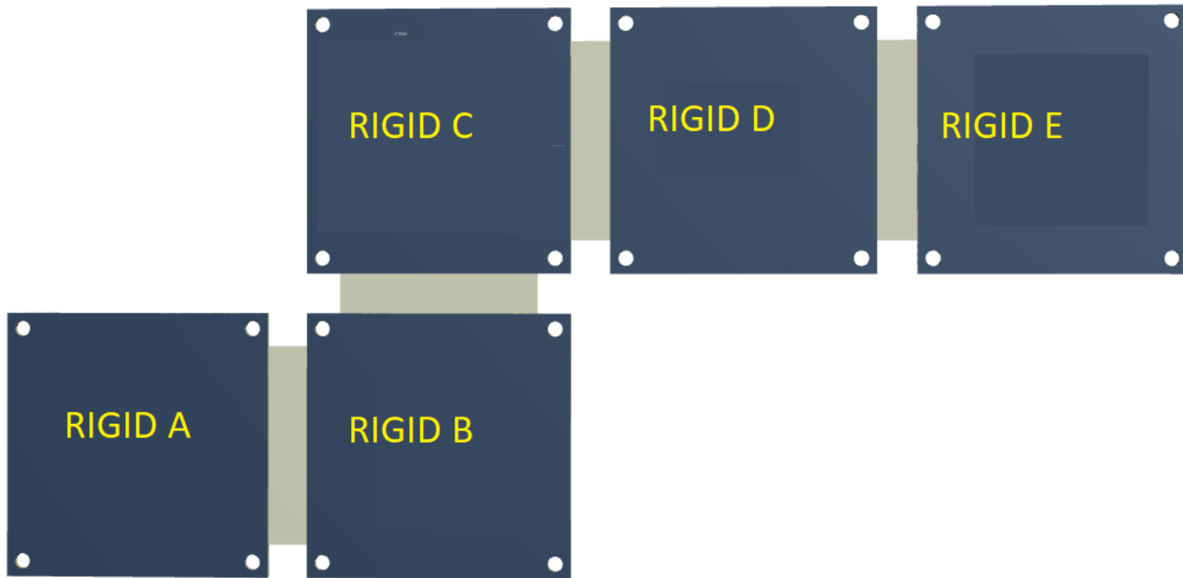
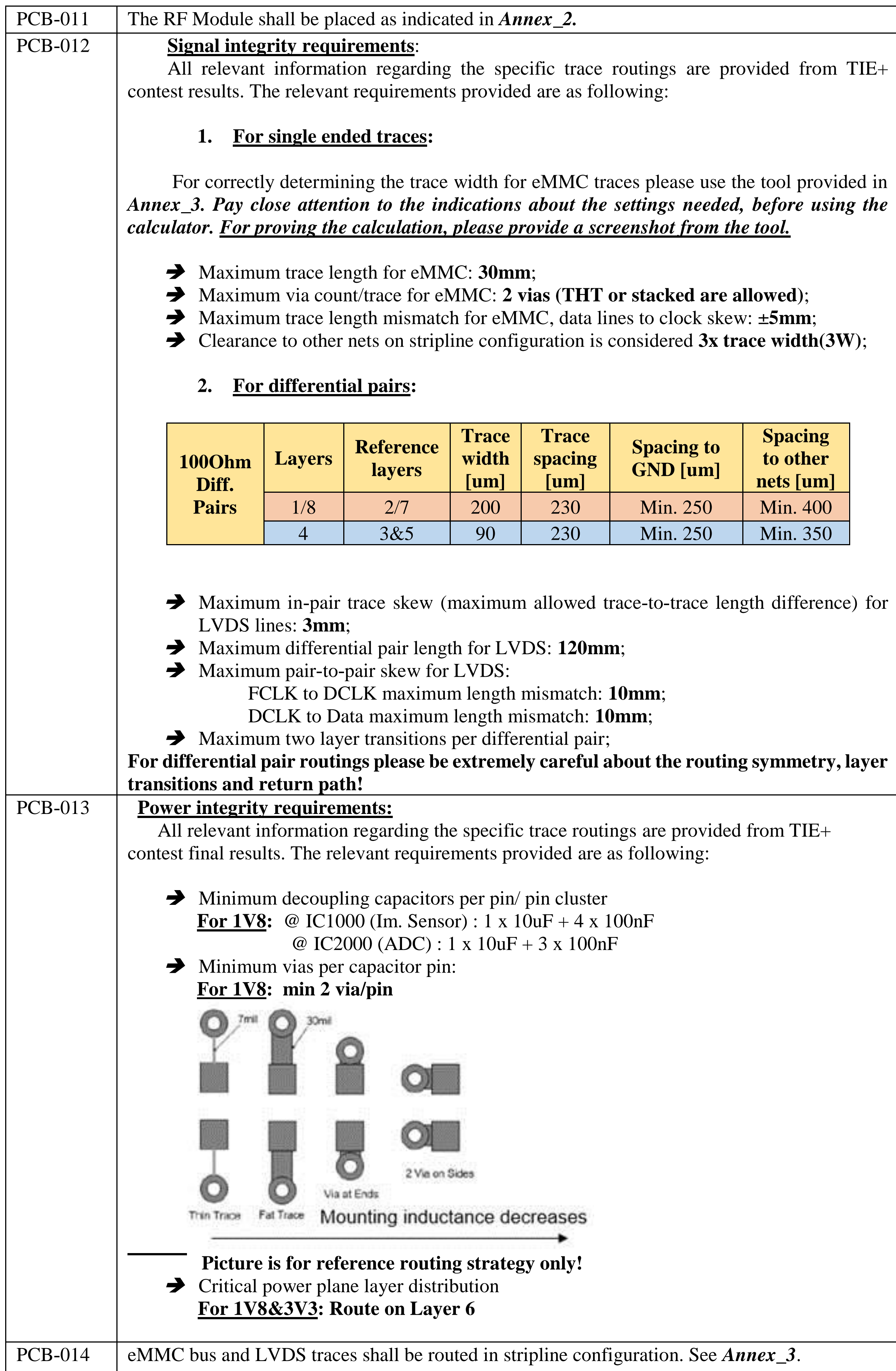


Figure 2. 2D view of the PCB and specific area naming.

PCB-001	The PCB layout design will take into consideration the proposed stack-up from ***Figure 1***. Each participant should define in their individual CAD software ***only the rigid stack-up.*** Minimum trace width is ***0.070mm*** and minimum clearance is ***0.100mm***.
PCB-002	Signal routing will be done as stated in the stack-up definition table/file provided. ***Please pay attention to the indications regarding the power plane distribution routing, signal distribution layers and the routing in the flexible areas.*** See ***Annex_3***.
PCB-003	Component descriptions, including standard footprints are indicated in the provided schematic and all the designers should have almost all of them prepared before the contest. One single component must be created as specified in the provided datasheet and saved in the ***TIE2019 library alongside all the components. For clarifications see Annex_5.***
PCB-004	All VIAs will have the following properties: • **THT VIA** (usage for rigid and flexible areas): **200µm** hole diameter, **350µm** solder mask opening and **400µm** copper pad; • **Blind/Buried VIAS (only rigid):** • **Layer 1 => Layer 2 – Blind(micro) via 125um hole size, pad size 325um, no solder mask opening;** • **Layer 2 => Layer 7 - Buried via 200um hole size, pad size 500um;** • **Layer 7 => Layer 8 – Blind(micro) via 125um hole size, pad size 325um, no solder mask opening;**
PCB-005	In order to have the desired functionalities, the components must be precisely placed, as indicated in the mechanical documentation. See ***Annex_2.***
PCB-006	The PCB origin shall be placed in the middle of the ***tooling hole No1***. See ***Annex_2.***
PCB-007	Knowing the mechanical information given in ***Annex_2***, please define the routing/placement restrictions on the specific mechanical/restriction layers accordingly (layer assignation is described in the ***Annex_2***).
PCB-008	Minimum distance between two adjacent components is ***400µm*** (component outline to component outline), and pad to pad ***250µm***.
PCB-009	On flexible areas, due to manufacturing requirements the routing will be done with ***rounded traces***. Also, if layer transitions are needed (via usage is mandatory) it is absolutely a must to use ***teardrops*** in order to prevent trace-to-via detachments.
PCB-010	The Camera Sensor (1IMG219) shall be placed as indicated in ***Annex_2.***



ID	Requirement
PCB-011	The RF Module shall be placed as indicated in ***Annex_2.***

PCB-012

Signal integrity requirements:

All relevant information regarding the specific trace routings are provided from TIE+ contest results. The relevant requirements provided are as following:

1. **For single ended traces:**

For correctly determining the trace width for eMMC traces please use the tool provided in ***Annex_3. Pay close attention to the indications about the settings needed, before using the calculator. For proving the calculation, please provide a screenshot from the tool.***

- ➔ Maximum trace length for eMMC: **30mm**;
- ➔ Maximum via count/trace for eMMC: **2 vias (THT or stacked are allowed)**;
- ➔ Maximum trace length mismatch for eMMC, data lines to clock skew: **±5mm**;
- ➔ Clearance to other nets on stripline configuration is considered **3x trace width(3W)**;

2. **For differential pairs:**

100Ohm Diff. Pairs	**Layers**	**Reference layers**	**Trace width [um]**	**Trace spacing [um]**	**Spacing to GND [um]**	**Spacing to other nets [um]**
	1/8	2/7	200	230	Min. 250	Min. 400
	4	3&5	90	230	Min. 250	Min. 350

- ➔ Maximum in-pair trace skew (maximum allowed trace-to-trace length difference) for LVDS lines: **3mm**;
- ➔ Maximum differential pair length for LVDS: **120mm**;
- ➔ Maximum pair-to-pair skew for LVDS:
  - FCLK to DCLK maximum length mismatch: **10mm**;
  - DCLK to Data maximum length mismatch: **10mm**;
- ➔ Maximum two layer transitions per differential pair;

For differential pair routings please be extremely careful about the routing symmetry, layer transitions and return path!

PCB-013

Power integrity requirements:

All relevant information regarding the specific trace routings are provided from TIE+ contest final results. The relevant requirements provided are as following:

- ➔ Minimum decoupling capacitors per pin/ pin cluster
  For 1V8: @ IC1000 (Im. Sensor) : 1 x 10uF + 4 x 100nF
  @ IC2000 (ADC) : 1 x 10uF + 3 x 100nF
- ➔ Minimum vias per capacitor pin:
  For 1V8: min 2 via/pin

Picture is for reference routing strategy only!

- ➔ Critical power plane layer distribution
  For 1V8&3V3: Route on Layer 6

ID	Requirement
PCB-014	eMMC bus and LVDS traces shall be routed in stripline configuration. See ***Annex_3***.

PCB-015	Minimize the current loop area for the DC-DC converter and keep the switching nodes (**SMPS1..4_SW**) as short as possible.
PCB-016	Use a minimum 3 vias per power rail to output capacitor pad for +V_SMPS_1V8 net and minimum 2 vias per output capacitor pad for +V_SMPS_3V3 net.
PCB-017	The following signals **SMPS1_FDBK, SMPS2_FDBK, SMPS3_FDBK, SMPS4_FDBK,** are sensitive load measuring signals. Please route these traces as close as possible to the power pins (**IC1000&IC2000**) clusters or decoupling capacitor areas, in order to dynamically adjust the energy distribution system.

5. Thermal considerations:

THERM-001	A thermal feedback will be provided to the power supply (PMIC) via **TH1000**(thermistor) to achieve supplementary protection for the controller. In case of overtemperature the supply rail to the processor will be cut. Make sure that the placement of this component is correct.
THERM-002	Since the system will run in space the only cooling mechanism is done using conduction and radiation. In order to remove the heat generated by electronics, one face of the cubical housing will act as a heatsink. Design a planar heatsink having the required radiative surface to dissipate a heat flux of **3W**. The emissivity of the surface is **0.7** and the mean temperature is **110 degC**. What is the thermal resistance of the heatsink? See ***Annex_4.1***. ***The results must be noted on the documentation layer.***
THERM-003	PMIC component has significant power dissipation value. Design the PCB level cooling method (Copper plane, thermal vias cluster and soldermask opening) to extract the heat from component taking into consideration that conduction heat path should have no more than **34°C/W** thermal resistance. See ***Annex_4.2***.

6. Test specifications:

TST-001	Test pads must be ***0.5mm (0.575mm solder mask opening)*** in diameter and they must all be accessible for the needles of an In-Circuit Test system (ICT).
TST-002	Test points added for accessing ***eMMC*** data/clock lines must be placed on ***rigid area C***, bottom side.
TST-003	Global fiducial markers, having circular shape ***1mm*** copper pad and solder mask opening of ***3mm***, must be introduced in a proper number, according to IPC recommendations.

7. Fabrication specifications:

FAB-001	In order to complete the manufacturing documentation, define one „documentation” layer, which will contain minimum the overall length and width of the PCB. On the same layer, clearly mark the rigid and flexible areas.
FAB-002	The necessary fabrication files (in extended Gerber format) must be provided.
FAB-003	Distinct drill file for holes must be provided.
FAB-004	Pick-and-place file for all SMT components must be generated.
FAB-005	A list of test point co-ordinates must be created, as a text file.

Total: ***300 points***