TIEplus 2019 Subject brief

TIEplus
Signal & Power Integrity
Simulation Challenge

› The diagram below describes a simplified architecture of a video monitoring system.
An **Image Sensor Board** is connected to a Main Board by a Flexible Printed Circuit cable.

System components:

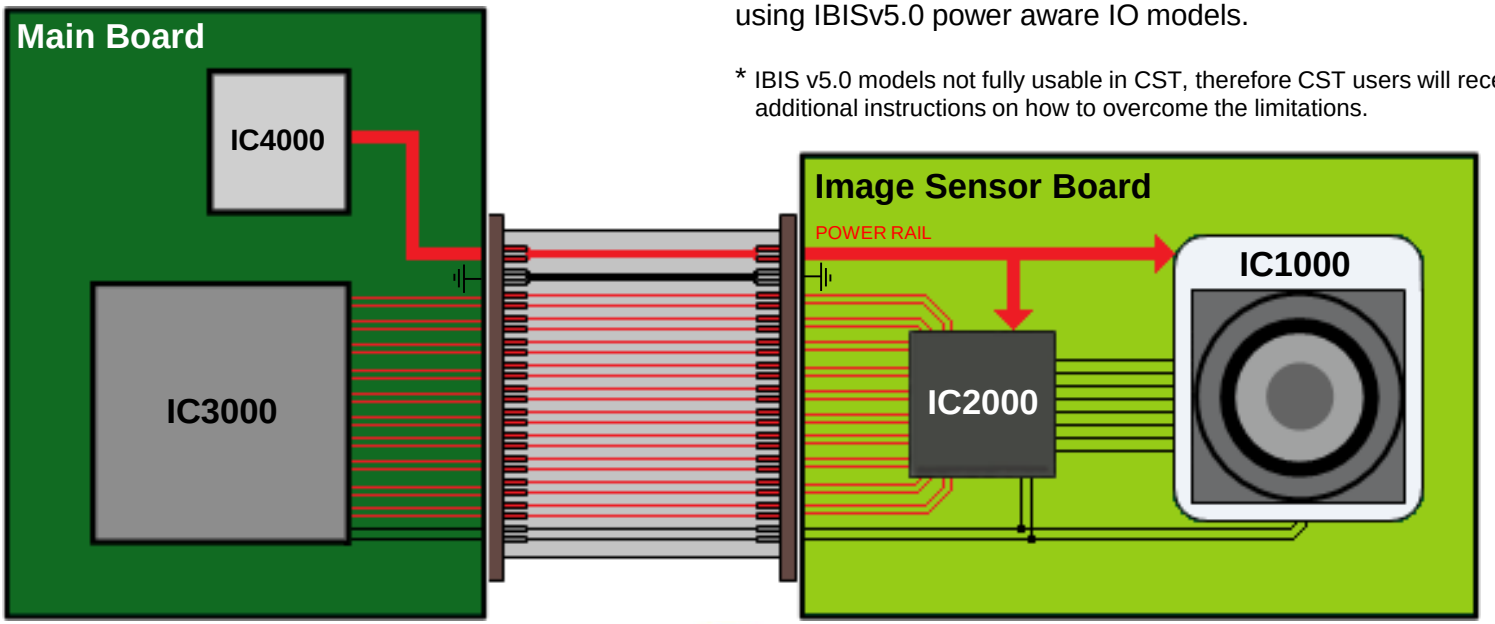
- IC1000 → Image sensor with Analog Outputs
- IC2000 → ADC with LVDS Outputs
- IC3000 → MCU with LVDS Inputs
- IC4000 → SMPS Module

› The objective is to **design** the **power distribution network**, (including capacitor selection and supply plane routing) as well as the **LVDS signal lines** for the Image Sensor Board.

› Solving the requirements will involve the complete workflow: pre-layout simulation, PCB design and post-layout simulation.

› To achieve this you must perform **SI/PI transient co-simulations** using IBISv5.0 power aware IO models.

* IBIS v5.0 models not fully usable in CST, therefore CST users will receive additional instructions on how to overcome the limitations.



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