

The diagram in slide 2 describes the simplified architecture for a FPGA graphic accelerator card connected to a server motherboard by a standard PCIe* edge connector (slot).

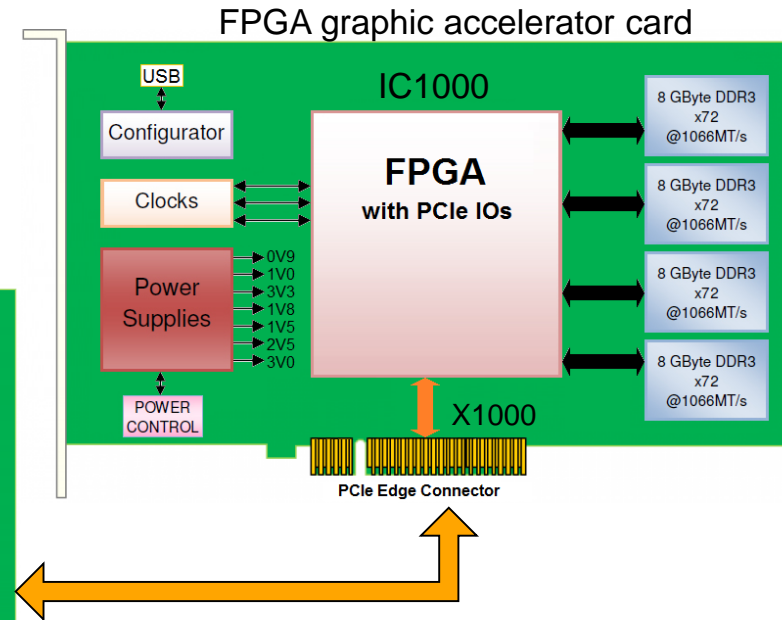
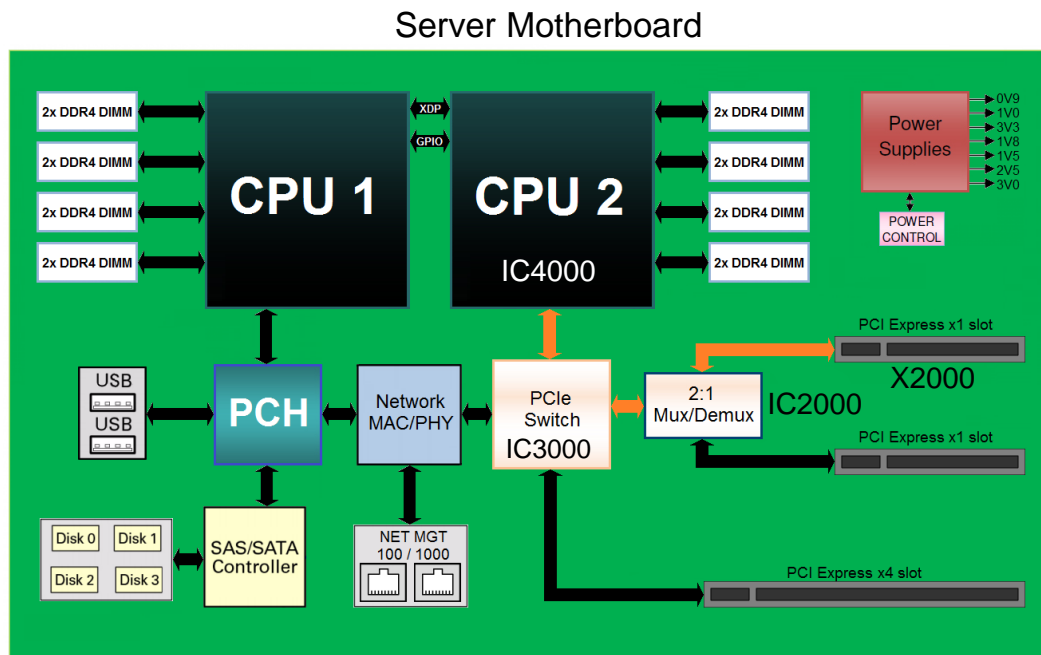
System components for the PCIe channel (marked in orange color):

- IC1000 → FPGA with PCIe I/O
- X1000 → board edge connector
- X2000 → socket connector for PCIe
- IC2000 → PCIe multiplexer IC
- IC3000 → PCIe switch IC
- IC4000 → CPU with PCIe I/O

The technical challenge is to design the a PCIe channel from IC1000 to IC4000 for 5GT/s and to evaluate basic compliance parameters based on the PCIsig specifications.

*PCIe (Peripheral Component Interconnect Express), officially abbreviated as PCIe or PCI-e is a high-speed serial computer expansion bus standard.

System Overview



Requirements



PRE-LAYOUT

- (A) Based on the provided stack-up definitions (pages 6, 7) define routing directives and strategy for FPGA graphic accelerator card and Server Motherboard PCBs. This implies defining routing layers, width, pair spacing and layer transitions.
- (B) Define a differential via design pattern to match the differential pair routing impedance for each PCB. The drill pairs for each PCB can be defined by you in order to meet impedance, skew and stub length requirements.
- (C) Evaluate intra-pair skew requirements and define length matching for each PCB.
- (D) Evaluate PCIe connector touchstone model (see page 8) and define the optimal pin choice PCIe routing.
- * Use any type of simulation (S-parameter, AC, Transient, Field Solver) to define the pre-layout guidelines.

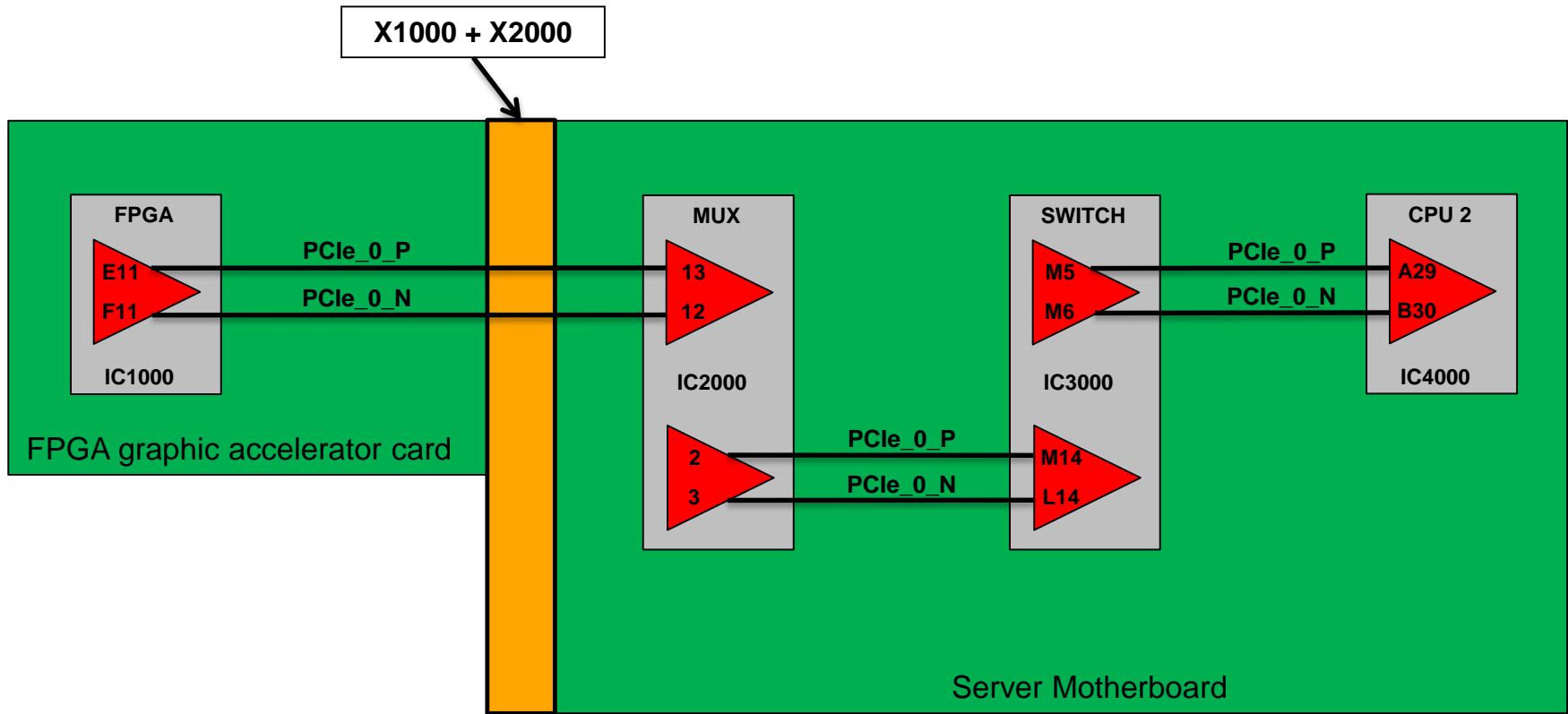
LAYOUT

- (E) Based on the results from the pre-layout analysis route the PCIe on both PCBs in a CAD environment. Board outlines and component placement are shown at page 10, while footprint guidelines are presented in separate documents.

POST-LAYOUT

- (F) Evaluate signal quality based on the eye diagram requirement at receiver IC4000 input.
- (G) Verify differential channel insertion loss compliance based on S-parameter mask at page 9.
- (H) Evaluate channel tolerance to random jitter.



























Block diagram



Part information\modeling summary

Part Name \ Reference	Description	Modeling information
IC1000	FPGA IC	Ibis file: <i>IC1000.ibs</i>
X1000	PCIe Edge Connector	Touchstone file: <i>X1000_X2000.s22p</i> considering both connectors
X2000	PCIe x4 Slot	
IC2000	PCIe Multiplexer IC	Touchstone file: <i>IC2000.s4p</i>
IC3000	PCIe Switch IC	Ibis file: <i>IC3000.ibs</i>
IC4000	CPU2 IC	Ibis file: <i>IC4000.ibs</i> Use <i>Receiver specification</i> from “PCI_Express_Base_Specification_Revision_3.0.pdf”

PCB Stack-up for Graphic Card

14 LAYER PCB										
	Layer #	Material Name	Material Type	Material Construction	Material Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)
							0.7	Solder Mask		
Top	1							 1	2.2	1.5
S1	2	FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7	4	3.4	 2	0.6	0.5
		FR-408	Core	1 x 3313 RC = 53.8%	3.7		4	 3	0.6	0.5
Ground	3							 3	0.6	0.5
		FR-408	Prepreg	2 x 106 RC = 63.3%	4	4	3	 4	0.6	0.5
V1	4							 4	0.6	0.5
		FR-408	Core	1 x 3313 RC = 53.8%	3.7		4	 5	0.6	0.5
S2	5							 5	0.6	0.5
		FR-408	Prepreg	1 X 3313 RC = 53.8%	3.7	4	3.4	 6	0.6	0.5
S3	6							 6	0.6	0.5
		FR-408	Core	1 x 3313 RC = 53.8%	3.7		4	 7	0.6	0.5
Ground	7							 7	0.6	0.5
		FR-408	Prepreg	2 x 106 RC = 63.3%	4	4	3	 8	0.6	0.5
V2	8							 8	0.6	0.5
		FR-408	Core	1 x 3313 RC = 53.8%	3.7		4	 9	0.6	0.5
S4	9							 9	0.6	0.5
		FR-408	Prepreg	1 X 3313 RC = 53.8%	3.7	4	3.4	 10	0.6	0.5
S5	10							 10	0.6	0.5
		FR-408	Core	1 x 3313 RC = 53.8%	3.7		4	 11	0.6	0.5
V4	11							 11	0.6	0.5
		FR-408	Prepreg	2 x 106 RC = 63.3%	4	4	3	 12	0.6	0.5
Ground	12							 12	0.6	0.5
		FR-408	Core	1 x 3313 RC = 53.8%	3.7		4	 13	0.6	0.5
S8	13							 13	0.6	0.5
		FR-408	Prepreg	1 x 3313 RC = 53.8%	3.7	4	3.4	 14	2.2	1.5
Bottom	14							 14	2.2	1.5
							0.7	Solder Mask		
							48.0	59.6	11.6	
							Material Thickness	Total Thickness	Copper Thickness	

Df Values

Solder mask – 0.028

3313 Core – 0.012

106 Core – 0.009

Signal routing layer

Microvias

L1-L2

L13-L14

L1-L3,

L12-L14

PCB Stack-up for Motherboard PCB

Layer #	Material Name	Material Type	Material Construction	Copper Type S = RTF, X = HVLP	Material Pressed Er (at ~2 GHz)	Material Unpressed Thickness (mils)	Material Pressed Thickness (mils)	Picture	Copper Thickness (mils)	Copper Thickness (oz)
1	Top				4.2		0.7	Solder Mask		
	FR-408HR	Prepreg	1 x 3313 RC = 53.8%		3.6	4	3.4	Prepreg	2.2	1.5
2	Ground			X						
	FR-408HR	Core	1 x 3313 RC = 53.8%	core	3.9		4	Core	0.6	0.5
3	Sig 1			X						
	FR-408HR	Prepreg	2 x 3313 RC = 53.8%		4.05	8	7.5	Prepreg	0.6	0.5
4	GND			X						
	FR-408HR	Core	1 x 3313 RC = 53.8%	core	3.9		4	Core	0.6	0.5
5	Sig 2			X						
	FR-408HR	Prepreg	2 x 3313 RC = 53.8%		4.05	8	7.5	Prepreg	0.6	0.5
6	GND			X						
	FR-408HR	Core	1 x 3313 RC = 53.8%	core	3.9		4	Core	0.6	0.5
7	Sig 3			X						
	FR-408HR	Prepreg	2 x 3313 RC = 53.8%		4.05	8	7.5	Prepreg	0.6	0.5
8	GND			S						
	FR-408HR	Core	3 x 1652 RC = 50%	core	4.37		18	Core	0.6	0.5
9	GND			S						
	FR-408HR	Prepreg	2 x 3313 RC = 53.8%		4.05	8	7.5	Prepreg	0.6	0.5
10	Sig 4			S						
	FR-408HR	Core	1 x 3313 RC = 53.8%	core	3.9		4	Core	0.6	0.5
11	GND			S						
	FR-408HR	Prepreg	2 x 3313 RC = 53.8%		4.05	8	7.5	Prepreg	0.6	0.5
12	Sig 5			S						
	FR-408HR	Core	1 x 3313 RC = 53.8%	core	3.9		4	Core	0.6	0.5
13	GND			S						
	FR-408HR	Prepreg	2 x 3313 RC = 53.8%		4.05	8	7.5	Prepreg	0.6	0.5
14	Sig 6			S						
	FR-408HR	Core	1 x 3313 RC = 53.8%	core	3.9		4	Core	0.6	0.5
15	Ground			S						
	FR-408HR	Prepreg	1 x 3313 RC = 53.8%		3.6	4	3.4	Prepreg	0.6	0.5
16	BOTTOM									
					4.2		0.7	Solder Mask		
							95.2	108.0	12.8	
							Material Thickness	Total Thickness	Copper Thickness	

Df Values

Solder mask – 0.025
3313 Prepreg – 0.010
3x1625 Core – 0.012

Signal routing layer

Microvias

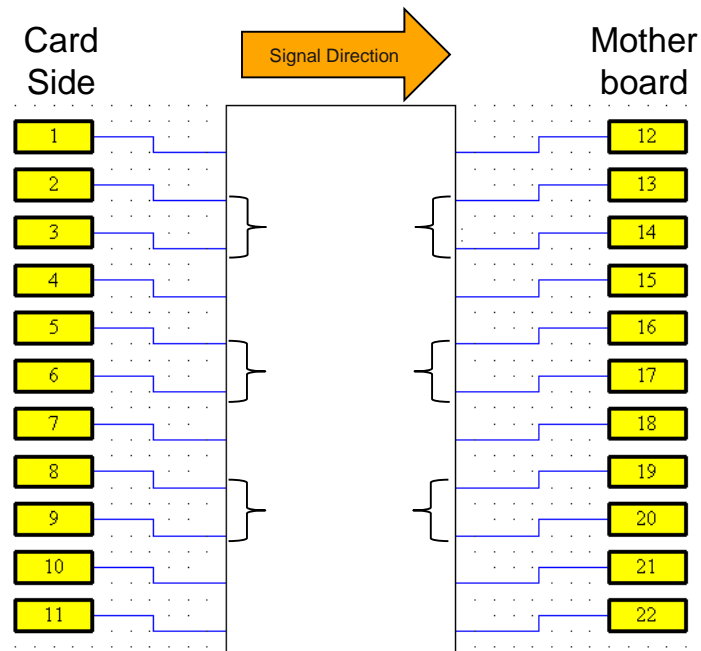
L1-L2
L15-L16
L1-L3,
L14-L16

PCIe Edge Connector

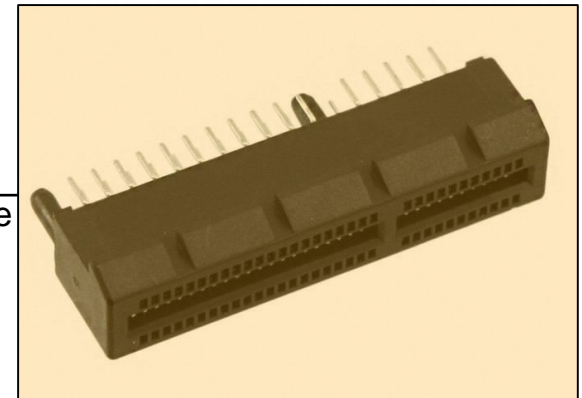
Amphenol FCI PCIe Gen 3 Board edge connector (36-position, 1.57 mm PCB thickness)

PCIe_conn.s22p – Touchstone model

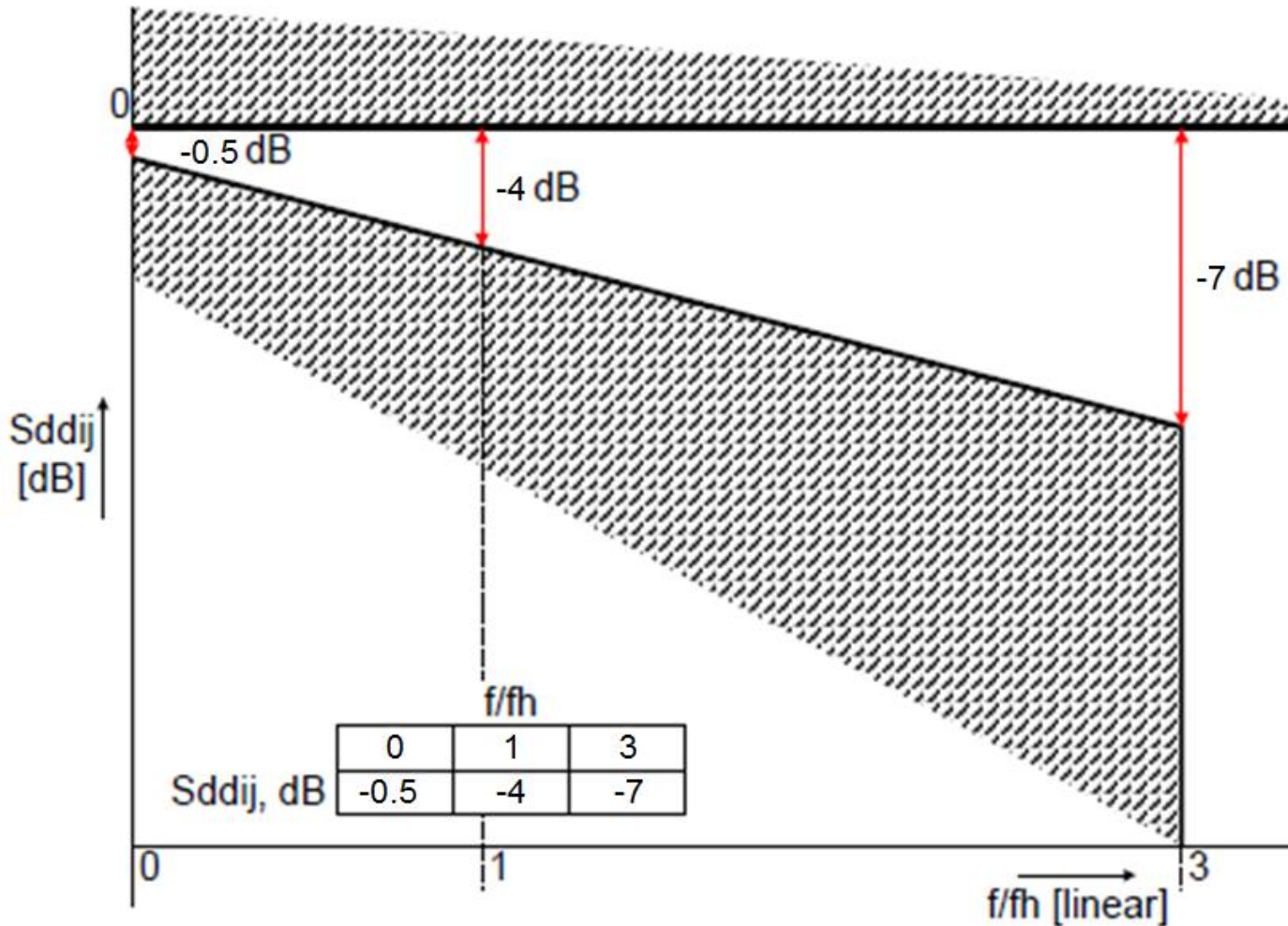
PCIe_conn_drawing.pdf – mechanical drawing and footprint



PCIe differential
Transmission side



Differential channel insertion loss



' f_h ' is the fundamental frequency for data transmission and is equal to $1/(2 \cdot UI)$

Mechanical drawings

