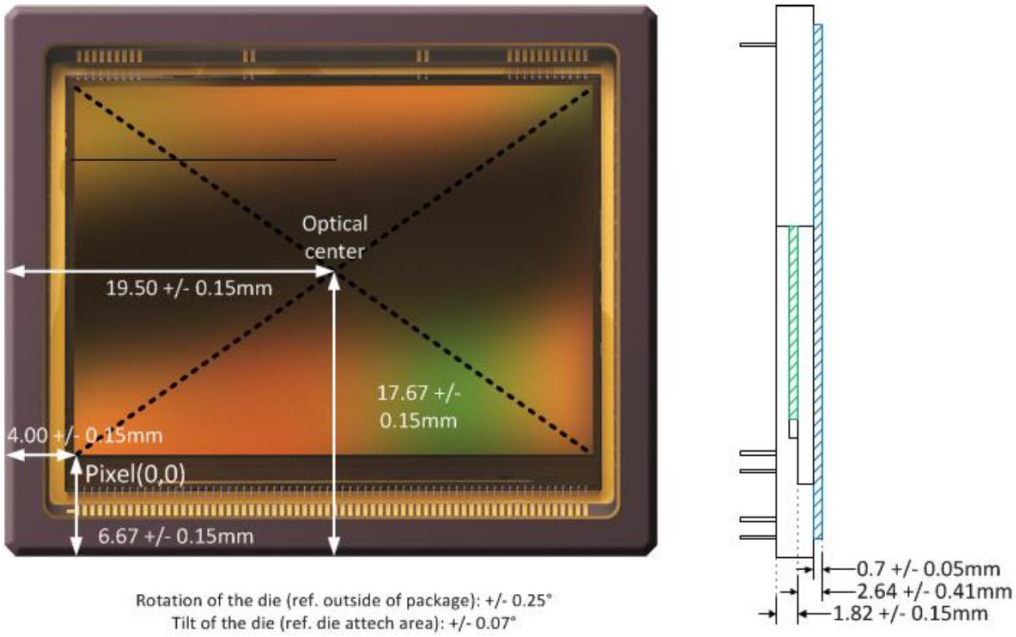


Figure 1 Image Sensor assembly

ELECTRICAL CHARACTERISTICS

(VDD3V3 = 3.3V, VDD1V8 = 1.8V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	Units
POWER REQUIREMENTS						
VDD1V8 Supply Voltage	(1) V_{VDD1V8}		1.75	1.80	1.90	V
VDD1V8 Peak Supply Current	I_{VDD1V8}			140		mA
VDD1V8 Idle Supply Current	I_{VDD1V8}			40		mA

(1) VDD1V8 may include AC noise above the specified limits for frequencies higher than 30MHz

For high-channel count applications, a high-speed serial interface between the data converter and MCU is preferred over a parallel interface because it simplifies the design and provides a denser and more cost-effective solution. A functional diagram of the octal 12-bit, 30Msps ADC is shown in Figure 18. The high-speed interface to the MCU consists of 10 LVDS pairs (20 pins): 8 high-speed serial outputs (1 for each channel), 1 serial LVDS output clock (LCLK), and 1 frame alignment clock (ADCLK).

The ADC clock input (CLK) or sample clock is multiplied by 6 to derive the serial LVDS output clock (LCLK). Serial data on each 12-bit channel is clocked on both the rising and falling edges of CLKOUT. The rising edge of the frame alignment clock (FRAME) corresponds to the first bit of the 12-bit serial data stream on each of the eight channels

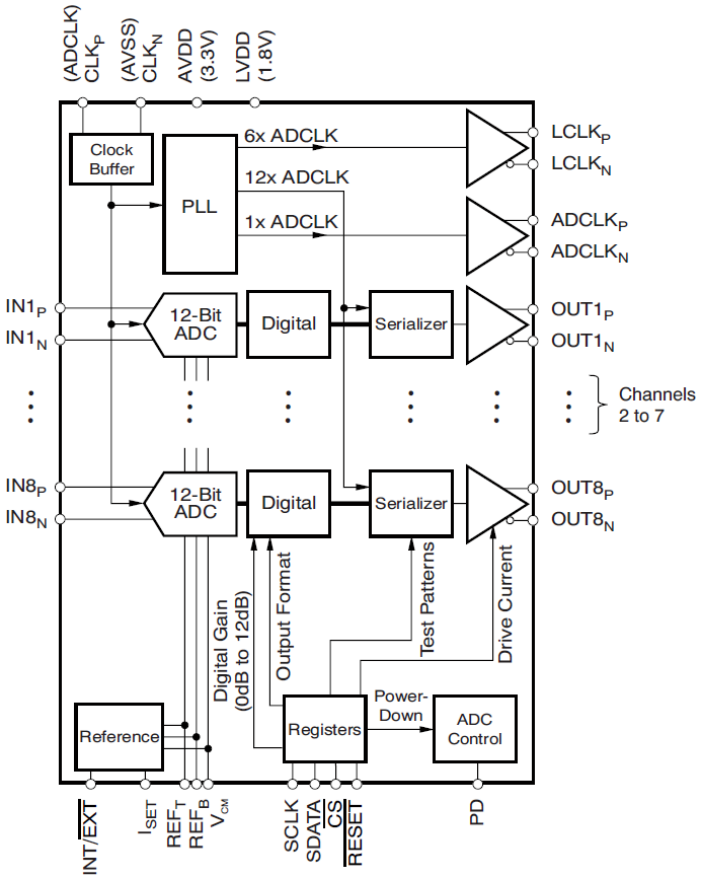


Figure 2 Simplified ADC Block Diagram

Implementing an octal 12-bit, 30Msps ADC with parallel CMOS outputs would require 97 pins for the highspeed digital interface to the MCU (approximately 5 times that of the serial LVDS interface). The significantly higher pin-count for a parallel interface implementation would require significantly more MCU I/O resources to capture the data. Larger packages for both MCU and ADC would also be required, which increase the routing complexity and number of printed circuit board layers needed for the design.

ABSOLUTE MAXIMUM RATINGS

Analog Supply AVDD to GND ..... -0.3V to +3.8V
Digital Supply LVDD to GND ..... -0.3V to +2.1V

OUT_P, OUT_N, $ADCLK_P$, $ADCLK_N$
$LCLK_P$, $LCLK_N$, to GND ..... -0.3V to the lower of (LVDD + 0.3V) and +2.1V

Junction Temperature ..... +150°C

Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AVDD = 3.3V, LVDD = 1.8V, f_{CLK} = 30MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	Units
LVDS DIGITAL OUTPUTS (OUT_P/OUT_N; $LCLK_P$/$LCLK_N$; $ADCLK_P$/$ADCLK_N$)						
Differential Output Voltage	$\|V_{OD}\|$	External RLOAD = 100 Ω	250		450	mV
Output Offset Voltage	V_{OS}	External RLOAD = 100 Ω	1.125		1.375	V
TIMING CHARACTERISTICS (Figures 4 and 5)						
Input Sampling Frequency	F_{SAMPLE}			30		MHz
Input Sampling Period	t_{SAMPLE}			33		ns
Data Valid to LCLK Rise/Fall	t_{OD}		$t_{SAMPLE}/24$ - 0.10	$t_{SAMPLE}/24$	$t_{SAMPLE}/24$ + 0.10	ns
LCLK Output High Time Width	t_{CH}			$t_{SAMPLE}/12$		ns
LCLK Output Low Time Width	t_{CL}			$t_{SAMPLE}/12$		ns
ADCLK Rise to LCLK Rise	t_{DF}		$t_{SAMPLE}/24$ - 0.10	$t_{SAMPLE}/24$	$t_{SAMPLE}/24$ + 0.10	ns
POWER REQUIREMENTS						
Analog Supply Voltage	V_{AVDD}		3.1	3.3	3.5	V
Digital Output Supply Voltage	V_{LVDD}		1.7	1.8	1.9	V

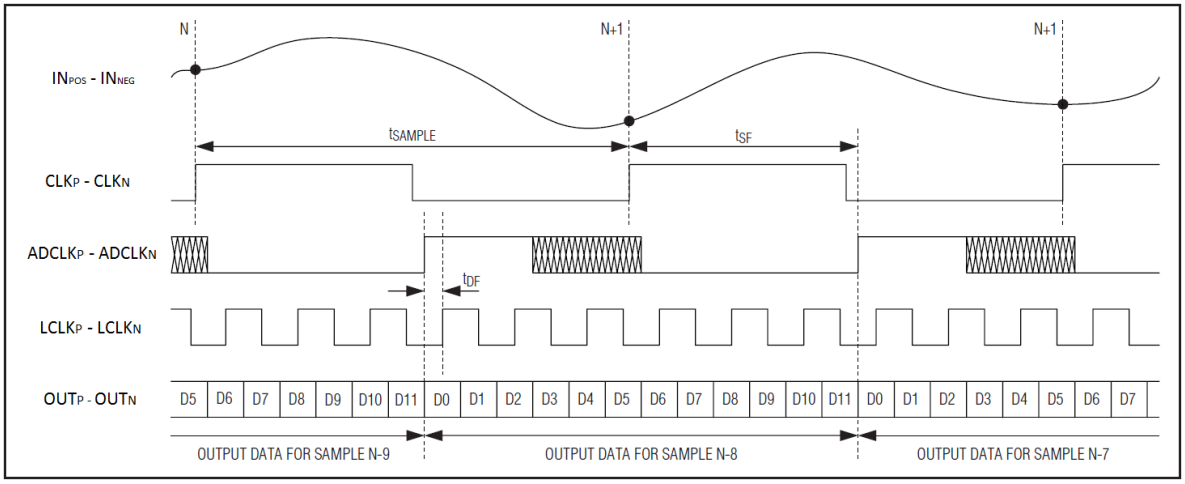


Figure 3 Conversion Timing Diagram

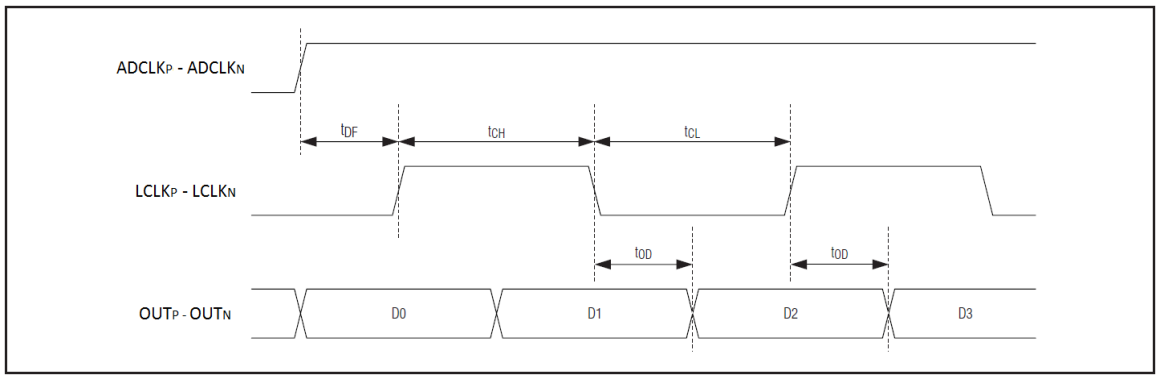


Figure 4 Detailed Output Timing Diagram

PIN DESCRIPTIONS – QFN64

PIN NAME	DESCRIPTION	PIN NUMBER	# OF PINS
AVDD	Analog power supply, 1.8V	49, 50, 57, 60	4
AVSS	Analog ground	3, 6, 9, 37, 40, 43, 46, 65(TAB)	7 + TAB
CLK_P	Positive differential clock input	58	1
CLK_N	Negative differential clock input Tie CLK_N to 0V for a single-ended clock	59	1
IN 1 $_P$	P Negative differential input signal, channel 1	1	1
IN 1 $_N$	N Negative differential input signal, channel 1	2	1
IN 2 $_P$	P Negative differential input signal, channel 2	4	1
IN 2 $_N$	N Negative differential input signal, channel 2	5	1
IN 3 $_P$	P Negative differential input signal, channel 3	7	1
IN 3 $_N$	N Negative differential input signal, channel 3	8	1
IN 4 $_P$	P Negative differential input signal, channel 4	10	1
IN 4 $_N$	N Negative differential input signal, channel 4	11	1
IN 5 $_P$	P Negative differential input signal, channel 5	38	1
IN 5 $_N$	N Negative differential input signal, channel 5	39	1
IN 6 $_P$	P Negative differential input signal, channel 6	41	1
IN 6 $_N$	N Negative differential input signal, channel 6	42	1
IN 7 $_P$	P Negative differential input signal, channel 7	44	1
IN 7 $_N$	N Negative differential input signal, channel 7	45	1
IN 8 $_P$	P Negative differential input signal, channel 8	47	1
IN 8 $_N$	N Negative differential input signal, channel 8	48	1
LVDD	Digital and I/O power supply, 1.8V	35	1
LVSS	Digital ground	12, 14, 36	3
$LCLK_P$	LVDS bit clock (6X)—positive output	25	1
$LCLK_N$	LVDS bit clock (6X)—negative output	26	1
$ADCLK_P$	LVDS frame clock (1X)—positive output	23	1
$ADCLK_N$	LVDS frame clock (1X)—negative output	24	1
OUT 1 $_P$	LVDS channel 1—positive output	15	1
OUT 1 $_N$	LVDS channel 1—negative output	16	1
OUT 2 $_P$	LVDS channel 2—positive output	17	1
OUT 2 $_N$	LVDS channel 2—negative output	18	1
OUT 3 $_P$	LVDS channel 3—positive output	19	1
OUT 3 $_N$	LVDS channel 3—negative output	20	1
OUT 4 $_P$	LVDS channel 4—positive output	21	1
OUT 4 $_N$	LVDS channel 4—negative output	22	1
OUT 5 $_P$	LVDS channel 5—positive output	27	1
OUT 5 $_N$	LVDS channel 5—negative output	28	1
OUT 6 $_P$	LVDS channel 6—positive output	29	1
OUT 6 $_N$	LVDS channel 6—negative output	30	1
OUT 7 $_P$	LVDS channel 7—positive output	31	1
OUT 7 $_N$	LVDS channel 7—negative output	32	1
OUT 8 $_P$	LVDS channel 8—positive output	33	1
OUT 8 $_N$	LVDS channel 8—negative output	34	1
PD	Power-down input	13	1
I_{SET}	Bias pin—56.2kΩ to ground 51 1	51	1
TP	Test pin, do not use	52	1
V_{CM}	Common-mode output pin, 1.5V output	53	1
REF $_B$	Negative reference input/output	54	1
REF $_T$	Positive reference input/output	55	1
INT/ #EXT	Internal/external reference mode select input	56	1
#CS	CS Serial enable chip select—active low digital input	61	1
SDATA	Serial data input	62	1
SCLK	Serial clock input	63	1
#RESET	Active low RESET input	64	1

PROCESSING MODULE

Measuring only 37mm by 39mm, the **Processing Module** is an system-on-module (SoM) covered with shield and powered by a processor based on the ARM Cortex-A7 architecture. The module carries out peripheral signals and IOs through **1.0mm pitch 140-pin stamp hole expansion interface**.

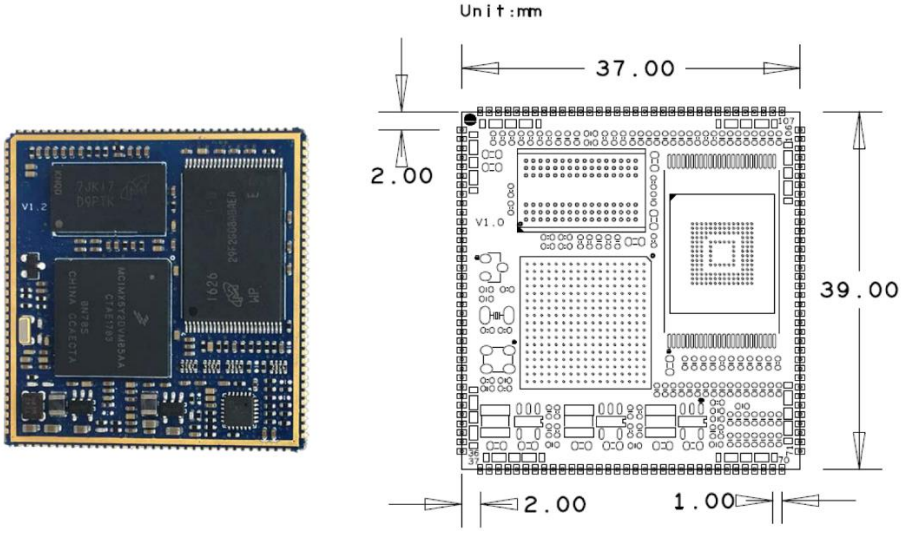


Figure 5 PROCESSING MODULE (140 pins)

The processor presents a Serial LVDS interface which reduces the number of interface lines, resulting in a compact package that allows for high system integration density.

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" for details.

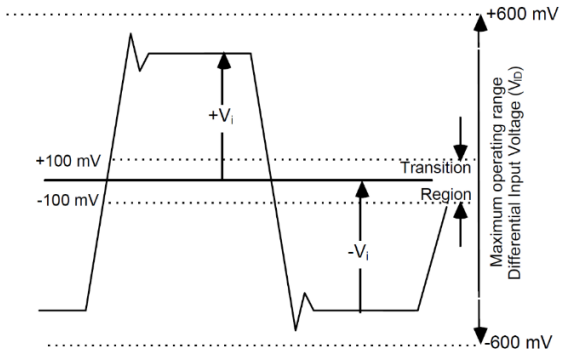


Figure 6 LVDS Receiver Input Measurement

ELECTRICAL CHARACTERISTICS

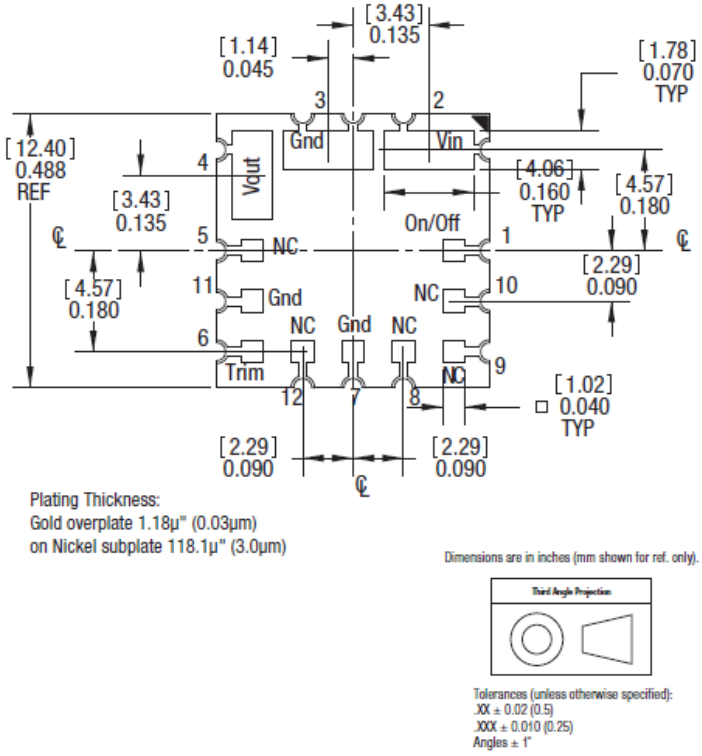
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	Units
LVDS INPUTS ($LVDS_P$/$LVDS_N$)						
Input Voltage High	V_i	Internal R_{TERM} = 100 Ω enabled	100		600	mV
Input Voltage Low	$-V_i$	Internal R_{TERM} = 100 Ω enabled	-600		100	mV
Input Common mode voltage	V_{ICM}	Internal R_{TERM} = 100 Ω enabled	0.300	1.200	1.425	V
Differential Internal resistance	R_{TERM}			100		Ω
INPUT TIMING CHARACTERISTICS						
Frame CLK Period	t_{FRAME}		20		50	ns
Pixel CLK Period	t_{PIXEL}			$t_{FRAME}/6$		ns
Frame CLK to Pixel CLK Skew	$t_{FP-SKEW}$		$t_{FRAME}/24$ - 0.20		$t_{FRAME}/24$ + 0.20	ns
Pixel CLK to Data Valid Skew	$t_{PD-SKEW}$		$t_{FRAME}/24$ - 0.20		$t_{FRAME}/24$ + 0.20	ns

Overshoot and undershoot conditions (transitions of single-ended signals above VDDSoM and below GND) must be held below 0.3V. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

POWER SUPPLY

Figure 7 POWER SUPPLY MODULE

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units
DC output voltage accuracy includes voltage references, DC load and line regulation, process and temperature	PWM mode	-1		2	%
Output Voltage Ripple	VOUT = 1.8 V		4		mV_{PP}



INPUT/OUTPUT CONNECTIONS	
Solder Pad	**Function**
1	On/Off Control *
2	Vin
3	Ground
4	Vout
5	No Connection **
6	Trim
7	Ground
8	No Connection**
9	No Connection **
10	No Connection**
11	Ground
12	No Connection**

* The Remote On/Off can be provided with either positive (P suffix) or negative (N suffix) logic.

** No Connection pins should not be connected to anything and should be left floating.

Figure 8 POWER SUPPLY MODULE Mechanical Outline