# Board Stack-up

The PCB stack-up is an 8 layer HDI based on the following configuration (final thickness values after pressing):

| LAYER CONSTRUCTION | LAYER TYPE | THICKNESS [µm] | $D_k$ |
|---|---|---|---|
| TOP LAYER | SIGNAL | 41 | |
| PREPREG 1x1080 | | 80 | 3.9 |
| INTERNAL LAYER TOP-1 | GND | 30 | |
| PREPREG 1x1080 | | 79 | 3.9 |
| INTERNAL LAYER TOP-2 | SIGNAL | 33 | |
| CORE 2x1506 | | 305 | 4.3 |
| INTERNAL LAYER TOP-3 | POWER | 15 | |
| PREPREG 2x7628 | | 387 | 4.4 |
| INTERNAL LAYER BOTTOM-3 | POWER | 15 | |
| CORE 2x1506 | | 305 | 4.3 |
| INTERNAL LAYER BOTTOM-2 | SIGNAL | 33 | |
| PREPREG 1x1080 | | 79 | 3.9 |
| INTERNAL LAYER BOTTOM-1 | GND | 30 | |
| PREPREG 1x1080 | | 80 | 3.9 |
| BOTTOM LAYER | SIGNAL | 41 | |

Soldermask properties:

- thickness =22µm
- $D_k$ = 4.6

Routing restrictions:

- Minimum trace width: 100µm
- Minimum spacing: 100µm

VIA configuration:

- MICROVIAS:
  ·ø 125 µm FROM TOP LAYER TO INTERNAL LAYER TOP-1
  ·ø 125 µm FROM TOP LAYER TO INTERNAL LAYER TOP-2
  ·ø 125 µm FROM INTERNAL LAYER BOTTOM-2 TO BOTTOM LAYER
  ·ø 125 µm FROM INTERNAL LAYER BOTTOM-1 TO BOTTOM LAYER
- BURIED VIAS:
  ·ø 250 µm FROM INTERNAL LAYER TOP-2 TO INTERNAL LAYER BOTTOM-2
- TH VIAS:
  ·ø 350 µm FROM TOP LAYER TO BOTTOM LAYER
- STACKED VIA COMBINATIONS (MICROVIA+BURIED)
  - TOP LAYER TO INTERNAL LAYER TOP-2 + INTERNAL LAYER TOP-2 TO INTERNAL LAYER BOTTOM-2 + INTERNAL LAYER BOTTOM-2 TO BOTTOM LAYER
  - TOP LAYER TO INTERNAL LAYER TOP-2 + INTERNAL LAYER TOP-2 TO INTERNAL LAYER BOTTOM-2
  - INTERNAL LAYER TOP-2 TO INTERNAL LAYER BOTTOM-2 + INTERNAL LAYER BOTTOM-2 TO BOTTOM LAYER
- VIA IN PAD IS allowed for IC1000 fan-out
- VIA plating thickness is 25 µm