TIE+ Subject
General circuit description

Figure 1 presents the block diagram for a SoC based graphical processing system. Figure 2 presents the connectivity diagram for the embedded x32 DDR3 point-to-point interface.

System description:

- IC1000 represents the GPU processing unit IC in a BGA625 package
- IC2000 and IC3000 are the two 1Gb DDR3 memory ICs in a FBGA96 package
- The data transfer rate is 1066MT/s; DDR3 clock frequency is 533MHz
- The DDR3 module is supplied by a 1.5V rail generated by the SMPS module based on IC5000
- VREF supply line design is not required

The following documents are provided:

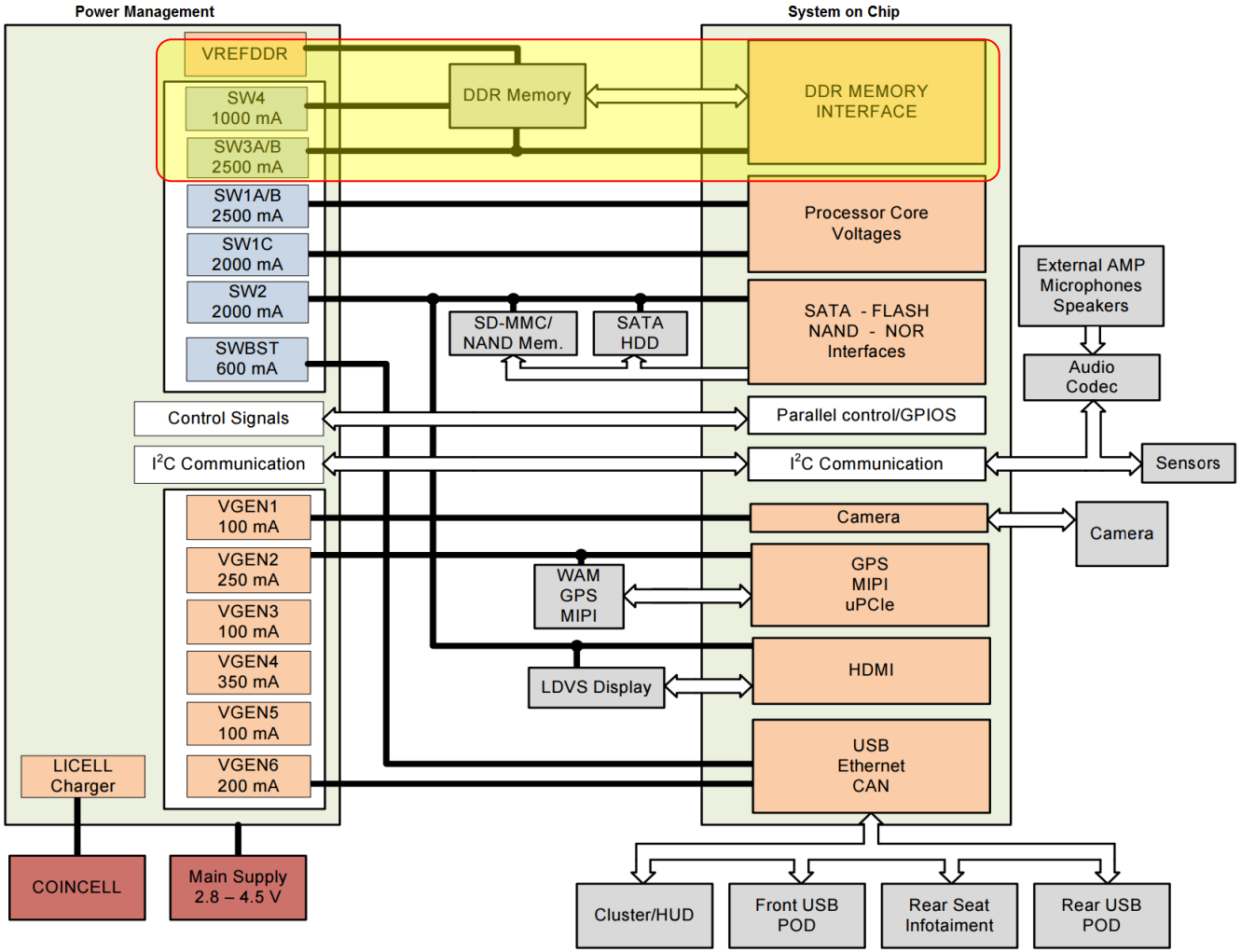
1. Stack-up.pdf – PCB stack-up definition with material properties and routing constraints
2. DDR3_Datasheet – technical data for DDR3 memory IC
3. SoC_Datasheet - technical data for GPU SoC
4. Schematic.pdf – the DDR3 interface schematic

The board definition and component placement are defined in on page 5.
The VRM (SMPS) modeling information is provided on page 6.

TIE+ Subject
Generic System Diagram

TIEplus
Signal & Power Integrity
Simulation Challenge

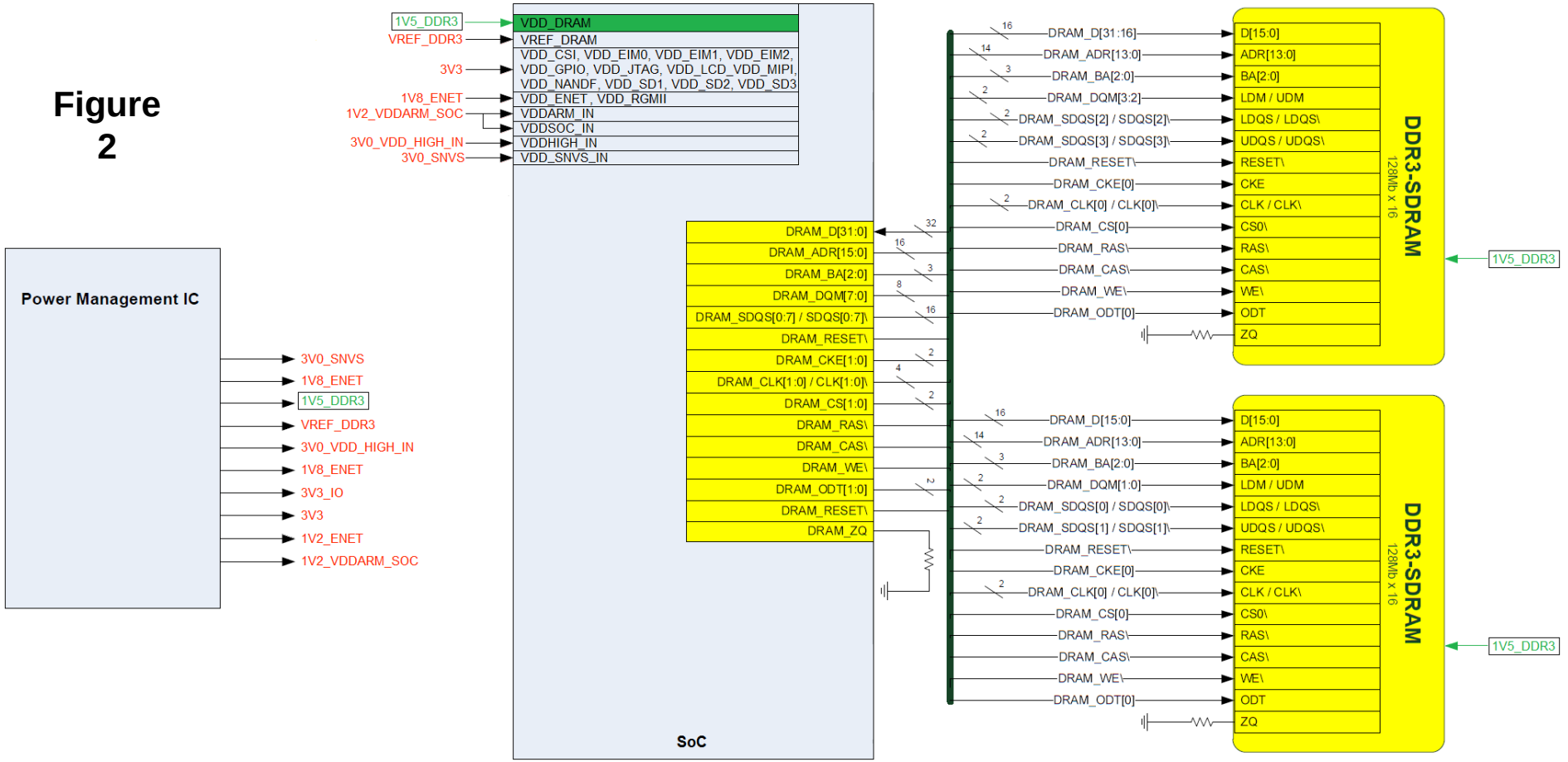
Figure 1



TIE+ Subject
DDR3 Interface Diagram

TIEplus Signal & Power Integrity Simulation Challenge

Figure 2



TIE+ Subject
Requirements

TIEplus
Signal & Power Integrity
Simulation Challenge

Based on the previous system description it is required to design and verify the power integrity solution for 1.5V DDR3 supply rail in order to meet the ripple noise requirements under maximum transient load conditions.

PRE-LAYOUT

(A) Evaluate noise budget and define DC drop and AC design targets

(B) Define plane geometry constraints based on the DC drop target

(C) Evaluate capacitor mounting inductance and plane spread inductance

(D) Establish the guidelines for power plane routing (minimum width, length)

(E) Define the decoupling capacitor network based on the AC design target

*Use capacitor models from Murata MLCC lineup (www.murata.com)
*Only capacitors with 0402, 0603 and 0805 case type must be used for decoupling

LAYOUT

(F) Based on the defined results from (D) and (E), route the power rails for 1V5 and GND (including capacitor network) in a CAD environment

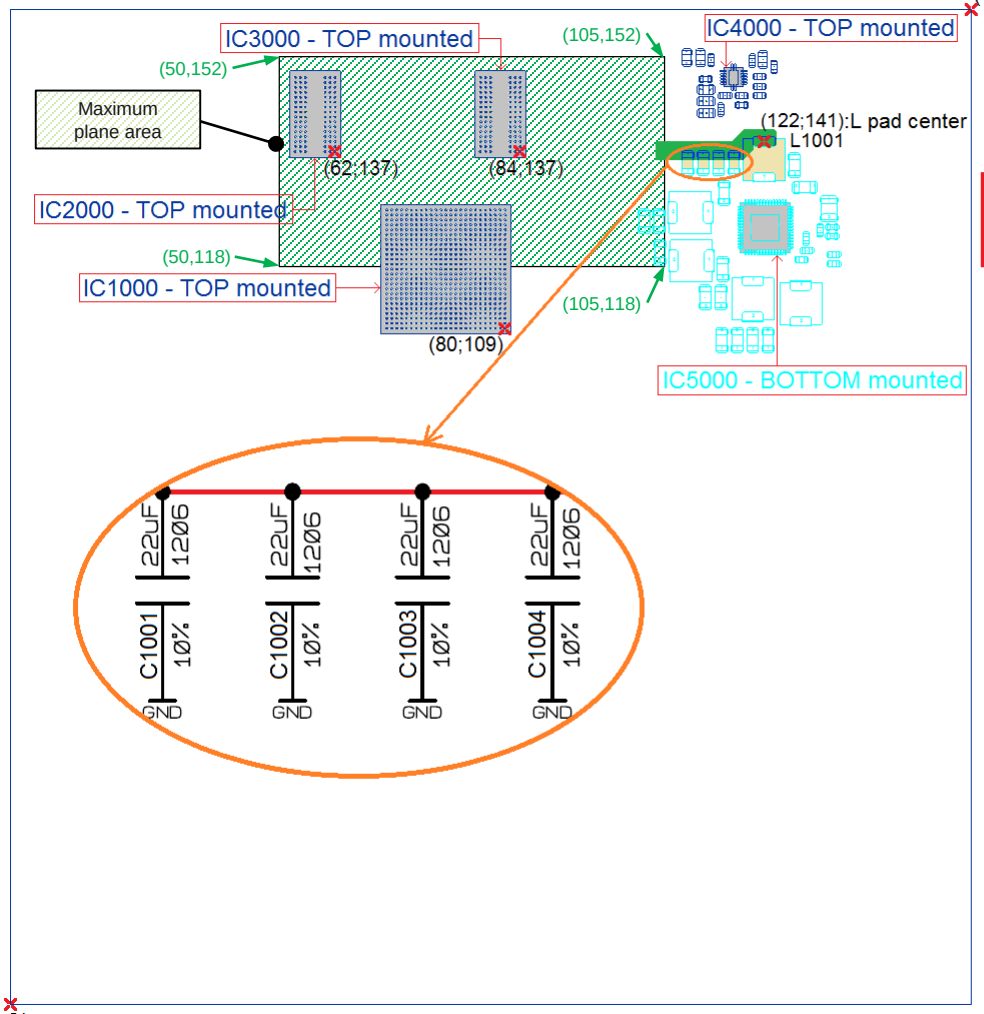
POST-LAYOUT

(G) Make an IR Drop Analysis on the 1V5 supply rail and verify compliance to the DC Drop target (point A)

(H) Make a post-layout analysis in the frequency domain for the 1V5 supply rail (and corresponding return path) and analyze impedance vs. frequency plot compliance to the target impedance (point A)

(I) Optimize the PDN design using a minimum number of decoupling capacitors

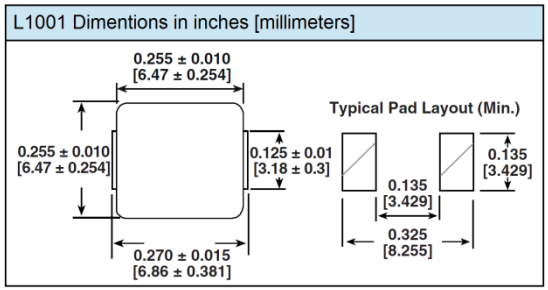
TIE+ Subject
Mechanical Drawing



(156;162)

- Top components
- Bottom components
- Bottom Layer
- Coordinates (in mm)

Coordinates for IC1000, IC2000 and IC3000 are given for ball A1 of each IC



Notes:

- Only the following components are mandatory for layout design: IC1000, IC2000, IC3000, L1001, C1001, C1002, C1003, C1004
- 1V5_DDR3 plane routing is allowed only on INTERNAL LAYER TOP-3 and INTERNAL LAYER BOTTOM-3 (refer to stack-up.pdf)
- GND plane routing is allowed only on INTERNAL LAYER TOP-1 and INTERNAL LAYER BOTTOM-1
- 1V5_DDR3 and GND islands (not full planes) are allowed on TOP LAYER and BOTTOM LAYER near decoupling capacitors
- 1V5_DDR3 and GND maximum plane dimensions are defined by the hatched area marked “Maximum plane area” (coordinates marked in green)
- All coordinates are specified as (x,y) in millimeters

Component list:

L1001: IHLP-2525CZ-A1 (Vishay)

C1001, C1002, C1003, C1004: GRM31CR70J226KE19K (Murata)

TIE+ Subject
VRM (SMPS) Characteristics

Output Voltage: 1.5 [V] (net ***1V5_DDR***)

Output Switching Ripple: 13 [mV]

Set point accuracy: +/-1 %

VRM Modeling: