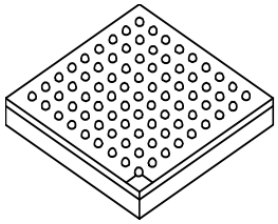
Automotive and Infotainment Application Processor



Package Information
Plastic Package
BGA Case 2240 21 x 21 mm, 0.8 mm pitch

1. Introduction

The automotive and infotainment processors represent the latest achievement in integrated multimedia-focused products offering high-performance processing with a high degree of functional integration. These processors are designed considering the needs of the growing automotive infotainment, telematics, HMI, and display-based cluster markets.

The system features an advanced implementation of ARM Cortex core, includes 2D and 3D graphics processors, 1080p video processing, and integrated power management.
It provides a 32-bit DDR3/LVDDR3-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

The processor is specifically useful for applications, such as:

- Entry-Level Automotive navigation and entertainment
- Graphics rendering for HMI
- High-performance speech processing with large databases
- Audio playback
- Video processing and display

1. Introduction 1
1.1. Features 1
2. Architectural Overview 2
2.1. Block Diagram 2
3. Modules List 2
4. Electrical Characteristics 3
4.1. Chip-Level Conditions 3
4.1.1 Absolute Maximum Ratings 3
4.1.2 Operating Range 3
4.1.3 Supply Currents 3
4.2. I/O DC Parameters 4
4.2.1 DDR Mode I/O DC Parameters 4
4.3. I/O AC Parameters 5
4.3.1 DDR Mode I/O AC Parameters 5
4.4. Output Buffer Impedance Parameters 6
4.4.1 DDR I/O Output Buffer Parameters 6
4.5. System Modules Timing 7
4.5.1 DDR3 Timing Parameters 7
5. Package Information and Contact Assignments 9
5.1. 21x21 mm Package Information 9
5.1.1 Case 2240, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix 9
5.1.2 21 x 21 mm Signal Assignments, Power Rails, and I/O 10
5.1.3 21 x 21 mm Ball Map 13

1.1 Features

External memory interfaces: The processor support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.

— 16/32-bit LP-DDR2, 16/32-bit DDR3-1066, and LV-DDR3-1066

— 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size.

— 16-bit NOR Flash.

— 16-bit PSRAM, Cellular RAM

2.Architectural Overview

Figure 1 shows the functional modules in the processor system

2.1 System block diagram

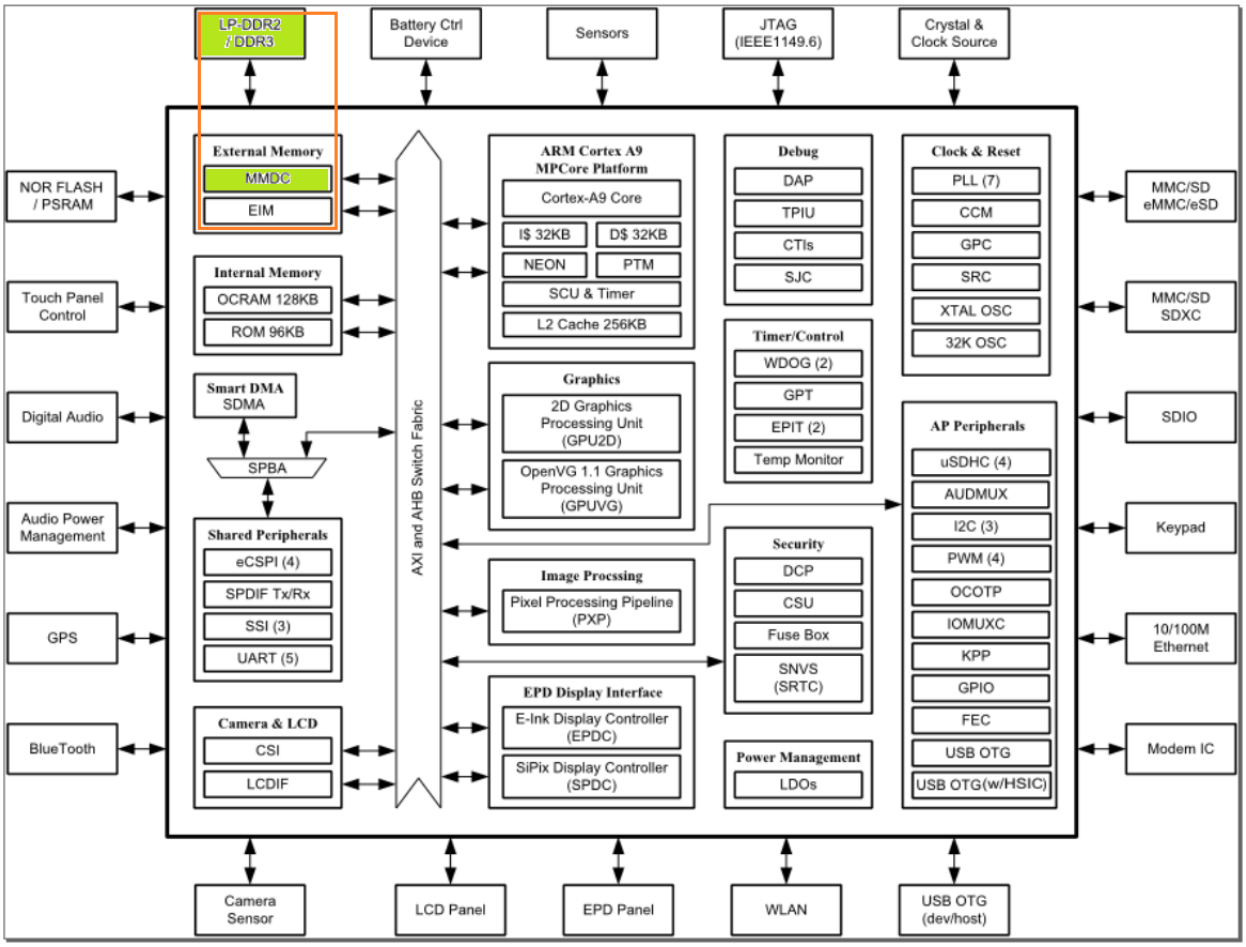


Figure 1 System Block Diagram

3.Module List

The processor contains a variety of digital and analog modules described in Table 2

Table 1 Module List

Block Mnemonic	Block Name	Subsystem	Brief Description
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32-bit DDR3-1066 (LV) or LPDDR2-1066 • Supports up to 4 GByte DDR memory space
⋮			

4. Electrical Characteristics

This section provides the device and module-level electrical characteristics.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 3 for a quick reference to the individual tables and sections.

4.1.1 Absolute Maximum Ratings

Stresses beyond those listed under Table 2 may affect reliability or cause permanent damage to the device. These are stress ratings only.

Table 2 Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Supply Voltage DDR IO	Supply denoted as IO supply	-0.2	1.975	V
⋮				

4.1.2 Operating Range

Table 3 provides the operating ranges of the processors.

Table 3 Operating Ranges

Parameter Description	Symbol	Min	Typ	Max	Unit	Comment
DDR IO supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2 / DDR3U
DDR IO supply	NVCC_DRAM	1.425	1.5	1.575	V	DDR3
DDR IO supply	NVCC_DRAM	1.283	1.35	1.45	V	DDR3-L
⋮						

4.1.3 Supply Currents

Table 4 represents the maximal momentary current transients on power lines, and should be used for power supply selection. Maximal currents are higher by far than the average power consumption of typical use cases.

Table 4 Supply Currents

Parameter Description	Conditions	Max Current	Unit
NVCC_DRAM steady		176	mA
NVCC_DRAM peak dynamic	Bandwidth requirement: DC-50MHz	460	mA
⋮			

4.2 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- Double Data Rate IO (DDR) for LPDDR2 and DDR3 modes
- General Purpose IO (GPIO)…
- LVDS I/O…

The term 'OVDD' in this section refers to the associated supply rail of an input or output.

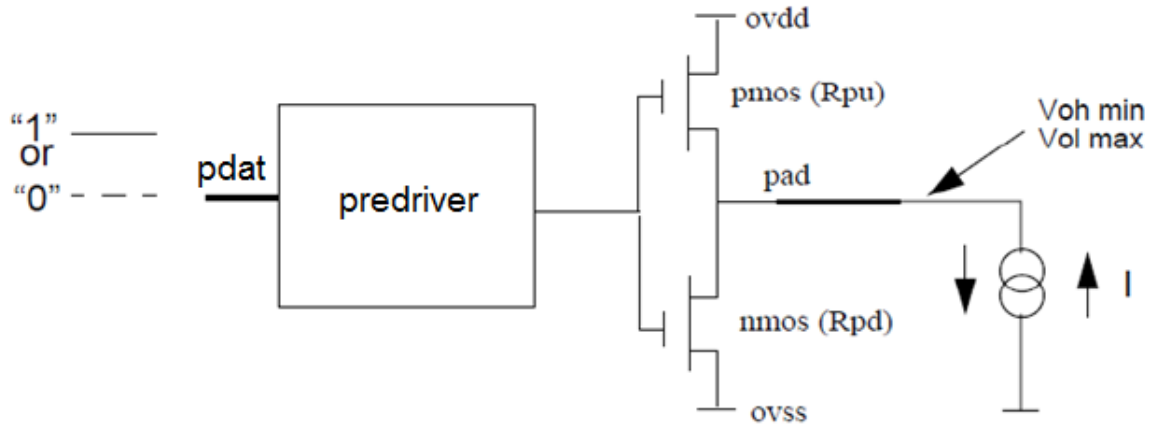


Figure 2 Voh and Vol for I/O Cells

4.2.1 DDR3 Mode I/O DC Parameters

The DDR3 interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.
The parameters in Table 5 are guaranteed per the operating ranges in Table 3.

Table 5 DDR3 I/O DC Electrical Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	-	0.8 x OVDD[1]	-	-	V
Low-level output voltage	Vol	-	-	-	0.2 x OVDD	V
DC input Logic High	Vih(dc)	-	Vref[2] + 0.1	-	OVDD	V
DC input Logic Low	Vil(dc)	-	OVSS	-	Vref - 0.1	V
Differential input Logic High	Vih(diff)	-	0.2	-	See Note[3]	V
Differential input Logic Low	Vil(diff)	-	See Note[3]			V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49 x OVDD	Vref	0.51 x OVDD	V
Pull-up/Pull-down impedance mismatch	MMpupd	-	-10	-	+10	%
240 Ω unit calibration resolution	Rres	-	-	-	10+	Ω

Note[1]: OVDD— I/O power supply (1.425 V-1.575 V for DDR3)
Note[2]: Vref— DDR3 external reference voltage
Note[3]: The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.3 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- Double Data Rate IO (DDR) for LPDDR2 and DDR3 modes
- General Purpose IO (GPIO)…
- LVDS I/O…

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 3 and Figure 4

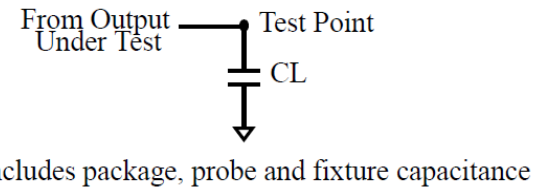


Figure 3 Load Circuit for Output

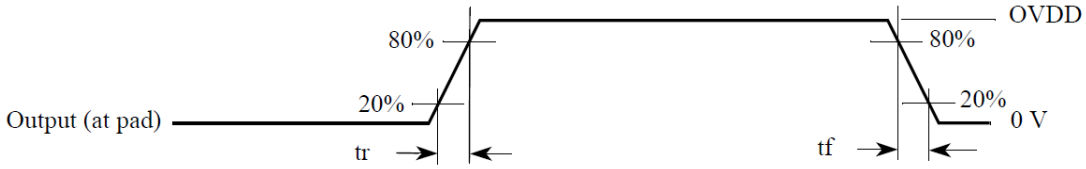


Figure 4 Output Transition Time Waveform

4.3.1 DDR3 Mode I/O AC Parameters

The DDR3 interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008. Table 6 shows the AC parameters for DDR I/O operating in DDR3 mode.

Table 6 DDR I/O DDR3 Mode AC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AC input Logic High	Vih(ac)	-	Vref + 0.175	-	OVDD	V
AC input Logic Low	Vil(ac)	-	OVSS	-	Vref - 0.175	V
AC differential input voltage [1]	Vid(ac)		0.35	-	-	V
Input AC differential cross point voltage [2]	Vix(ac)	Relative to Vref	Vref - 0.15	-	Vref + 0.15	V
Over/undershoot peak	Vpeak	-	-	-	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	533 MHz	-	-	0.5	Vns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Drive impedance = 34 Ω	2.5	-	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 533 MHz	-	-	0.1	ns

Note[1]: Vid(ac) specifies the input differential voltage | Vtr-Vcp | required for switching, where Vtr is the "true" input signal and Vcp is the "complementary" input signal.
The Minimum value is equal to Vih(ac) - Vil(ac).

Note[2]: The typical value of Vix(ac) is expected to be about 0.5 x OVDD and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.4 Output Buffer Impedance Parameters

This section includes the I/O impedance parameters of the following I/O types:

- Double Data Rate IO (DDR) for LPDDR2 and DDR3 modes
- General Purpose IO (GPIO)…
- LVDS I/O…

4.4.1 DDR I/O Output Buffer Parameters

The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 7 shows DDR I/O output buffer impedance.

Table 7 DDR3 I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical (NVCC_DRM = 1.5 V)	Unit
Output Driver Impedance	Rdrv	Drive Strength (DSE) = 000 001 010 011 100 101 110 111	 Hi-Z 240 120 80 60 48 40 34	Ω

The power consumption for the NVCC_DRAM supply is affected by various factors, including the following:

- Amount of activity of the DDR interface
- On-die termination (ODT)—Enabled/disabled, termination value, which is used for the DDR controller and DDR memories
- Board termination for DDR control and address bus
- Configuration of the DDR pads (such as, drive strength)
- Board layout
- Load of the DDR memory devices

4.5 System Modules Timing

This section contains the timing and electrical parameters for the each of the modules in the processors.

4.5.1 DDR3 Timing Parameters

Figure 5 shows the basic timing parameters. The timing parameters for this diagram appear in Table 8.

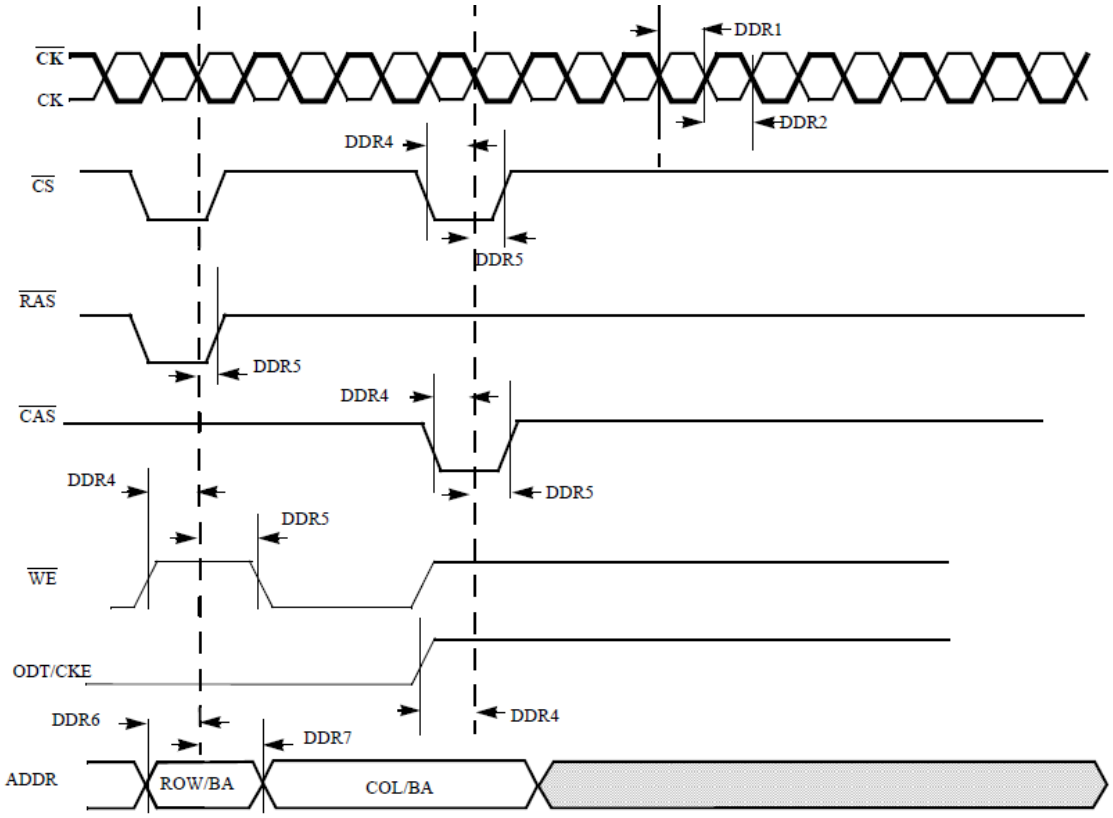


Figure 5 DDR3 Command and Address Timing Parameters

Table 8 DDR3 Timing Parameter Table

ID	Parameter	Symbol	CL = 532 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	t_{CH}	0.47	0.53	t_{CK}
DDR2	CK clock low-level width	t_{CL}	0.47	0.53	t_{CK}
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}	500	-	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}	400	-	ps
DDR6	Address output setup time	t_{IS}	500	-	ps
DDR7	Address output hold time	t_{IH}	400	-	ps

Figure 6 shows the write timing parameters. The timing parameters for this diagram appear in Table 9.

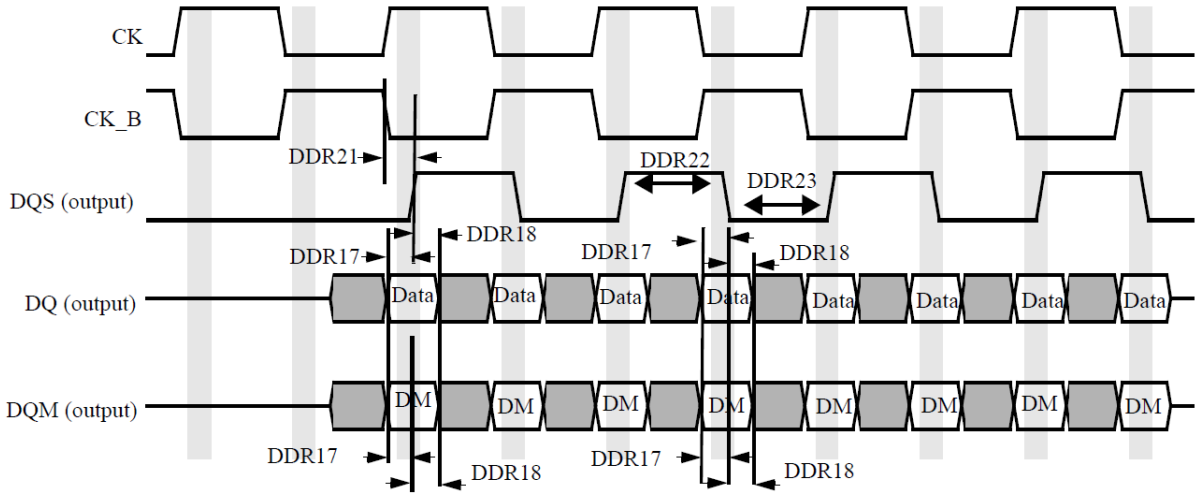


Figure 6 DDR3 Write Cycle

Table 9 DDR3 Write Cycle

ID	Parameter	Symbol	CL = 532 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	t_{DS}	240	-	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	t_{DH}	240	-	ps
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.25	+0.25	t_{CK}
DDR22	DQS high level width	t_{DQSH}	0.45	0.55	t_{CK}
DDR23	DQS low level width	t_{DQSL}	0.45	0.55	t_{CK}

All measurements are in reference to Vref level.

Figure 7 shows the write timing parameters. The timing parameters for this diagram appear in Table 10.

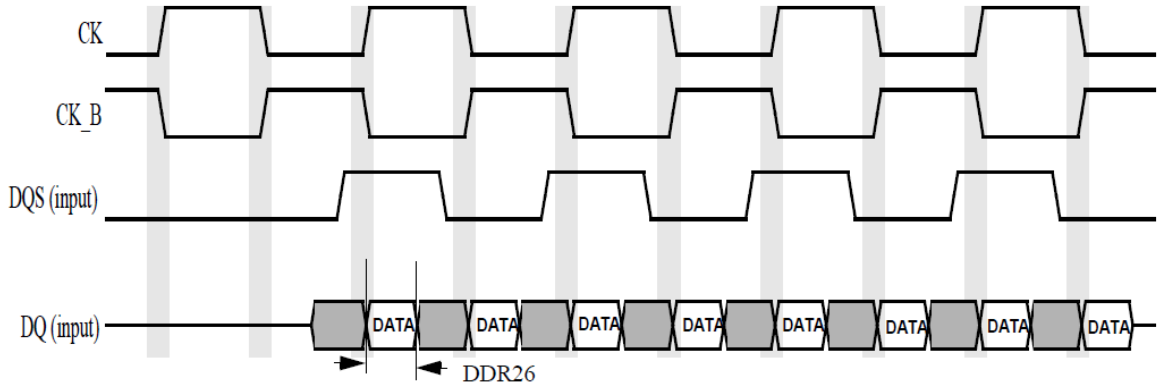


Figure 7 DDR3 Read Cycle

Table 10 DDR3 Read Cycle

ID	Parameter	Symbol	CL = 532 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	-	450	-	ps

All measurements are in reference to Vref level.

5. Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing

5.1 21 x 21 mm Package Information (BGA625)

5.1.1 Case 2240, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix

Figure 8 shows the top, bottom, and side views of the 21x21 mm BGA package. (All dimensions in mm)

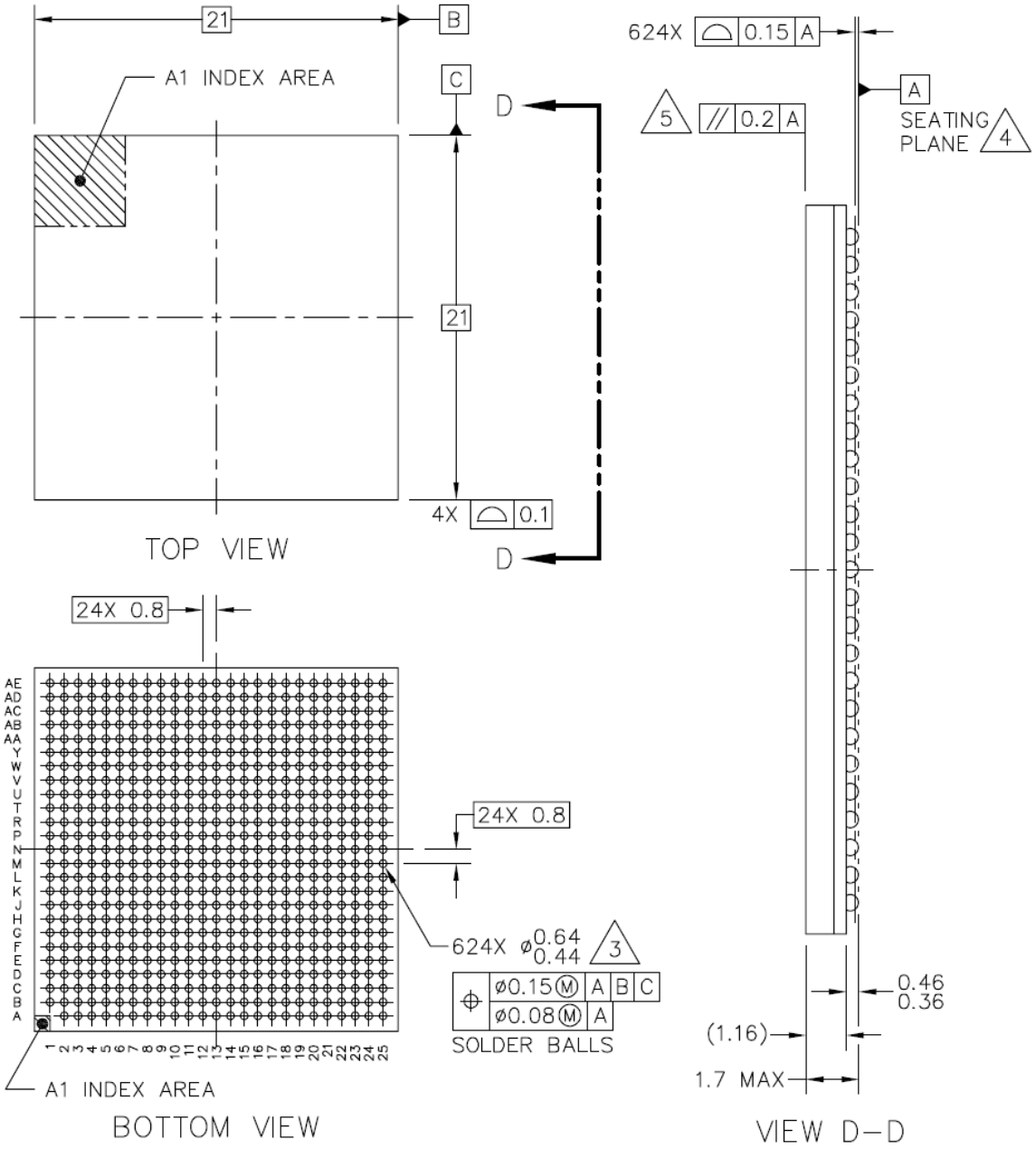


Figure 8 PBGA, Low Profile, Fine Pitch, 624 I/O, 21x21 PKG, 0.8 mm Pitch

5.1.2 21 x 21 mm Signal Assignments, Power Rails, and I/O

Table 11 Supplies Contact Assignments

Supply Rail Name	Ball(s) Position(s)	Remark
GND	A4, A8, A13, A25, B4, C1, C4, C6, C10, D3, D6, D8, E5, E6, E7, F5, F6, F7, F8, G3, G10, G19, H8, H12, H15, H18, J2, J8, J12, J15, J18, K8, K10, K12, K15, K18, L2, L5, L8, L10, L12, L15, L18, M8, M10, M12, M15, M18, N8, N10, N15, N18, P8, P10, P12, P15, P18, R8, R12, R15, R17, T8, T11, T12, T15, T17, T19, U8, U11, U12, U15, U17, U19, V8, V19, W3, W7, W8, W9, W10, W11, W12, W13, W15, W16, W17, W18, W19, Y5, Y24, AA7, AA10, AA13, AA16, AA19, AA22, AB3, AB24, AD4, AD7, AD10, AD13, AD16, AD19, AD22, AE1, AE25	
NVCC_DRAM	R18, T18, U18, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18	Supply of DDR interface

Table 12 Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]		
				Default Function	Input/ Output	Value
DRAM_A0	AC14	NVCC_DRAM	DDR	mmdc.DRAM_A0	Output	Low
DRAM_A1	AB14	NVCC_DRAM	DDR	mmdc.DRAM_A1	Output	Low
DRAM_A2	AA14	NVCC_DRAM	DDR	mmdc.DRAM_A2	Output	Low
DRAM_A3	Y14	NVCC_DRAM	DDR	mmdc.DRAM_A3	Output	Low
DRAM_A4	W14	NVCC_DRAM	DDR	mmdc.DRAM_A4	Output	Low
DRAM_A5	AE13	NVCC_DRAM	DDR	mmdc.DRAM_A5	Output	Low
DRAM_A6	AC13	NVCC_DRAM	DDR	mmdc.DRAM_A6	Output	Low
DRAM_A7	Y13	NVCC_DRAM	DDR	mmdc.DRAM_A7	Output	Low
DRAM_A8	AB13	NVCC_DRAM	DDR	mmdc.DRAM_A8	Output	Low
DRAM_A9	AE12	NVCC_DRAM	DDR	mmdc.DRAM_A9	Output	Low
DRAM_A10	AA15	NVCC_DRAM	DDR	mmdc.DRAM_A10	Output	Low
DRAM_A11	AC12	NVCC_DRAM	DDR	mmdc.DRAM_A11	Output	Low
DRAM_A12	AD12	NVCC_DRAM	DDR	mmdc.DRAM_A12	Output	Low
DRAM_A13	AC17	NVCC_DRAM	DDR	mmdc.DRAM_A13	Output	Low
DRAM_A14	AA12	NVCC_DRAM	DDR	mmdc.DRAM_A14	Output	Low
DRAM_A15	Y12	NVCC_DRAM	DDR	mmdc.DRAM_A15	Output	Low
DRAM_CAS	AE16	NVCC_DRAM	DDR	mmdc.DRAM_CAS	Output	Low
DRAM_RAS	AB15	NVCC_DRAM	DDR	mmdc.DRAM_RAS	Output	Low
DRAM_SDBA0	AC15	NVCC_DRAM	DDR	mmdc.DRAM_SDBA[0]	Output	Low
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	mmdc.DRAM_SDBA[1]	Output	Low
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	mmdc.DRAM_SDBA[2]	Output	Low
DRAM_SDODT0	AC16	NVCC_DRAM	DDR	mmdc.DRAM_ODT[0]	Output	Low
DRAM_SDODT1	AB17	NVCC_DRAM	DDR	mmdc.DRAM_ODT[1]	Output	Low
DRAM_SDWE	AB16	NVCC_DRAM	DDR	mmdc.DRAM_SDWE	Output	Low
DRAM_CS0	Y16	NVCC_DRAM	DDR	mmdc.DRAM_CS[0]	Output	Low
DRAM_CS1	AD17	NVCC_DRAM	DDR	mmdc.DRAM_CS[1]	Output	Low
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	mmdc.DRAM_SDCKE[0]	Output	Low
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	mmdc.DRAM_SDCKE[1]	Output	Low
DRAM_RESET	Y6	NVCC_DRAM	DDR	mmdc.DRAM_RESET	Output	Low

DRAM_D0	AD2	NVCC_DRAM	DDR	mmdc.DRAM_D[0]	Input	100 kΩ pull-up
DRAM_D1	AE2	NVCC_DRAM	DDR	mmdc.DRAM_D[1]	Input	100 kΩ pull-up
DRAM_D2	AC4	NVCC_DRAM	DDR	mmdc.DRAM_D[2]	Input	100 kΩ pull-up
DRAM_D3	AA5	NVCC_DRAM	DDR	mmdc.DRAM_D[3]	Input	100 kΩ pull-up
DRAM_D4	AC1	NVCC_DRAM	DDR	mmdc.DRAM_D[4]	Input	100 kΩ pull-up
DRAM_D5	AD1	NVCC_DRAM	DDR	mmdc.DRAM_D[5]	Input	100 kΩ pull-up
DRAM_D6	AB4	NVCC_DRAM	DDR	mmdc.DRAM_D[6]	Input	100 kΩ pull-up
DRAM_D7	AE4	NVCC_DRAM	DDR	mmdc.DRAM_D[7]	Input	100 kΩ pull-up
DRAM_D8	AD5	NVCC_DRAM	DDR	mmdc.DRAM_D[8]	Input	100 kΩ pull-up
DRAM_D9	AE5	NVCC_DRAM	DDR	mmdc.DRAM_D[9]	Input	100 kΩ pull-up
DRAM_D10	AA6	NVCC_DRAM	DDR	mmdc.DRAM_D[10]	Input	100 kΩ pull-up
DRAM_D11	AE7	NVCC_DRAM	DDR	mmdc.DRAM_D[11]	Input	100 kΩ pull-up
DRAM_D12	AB5	NVCC_DRAM	DDR	mmdc.DRAM_D[12]	Input	100 kΩ pull-up
DRAM_D13	AC5	NVCC_DRAM	DDR	mmdc.DRAM_D[13]	Input	100 kΩ pull-up
DRAM_D14	AB6	NVCC_DRAM	DDR	mmdc.DRAM_D[14]	Input	100 kΩ pull-up
DRAM_D15	AC7	NVCC_DRAM	DDR	mmdc.DRAM_D[15]	Input	100 kΩ pull-up
DRAM_D16	AB7	NVCC_DRAM	DDR	mmdc.DRAM_D[16]	Input	100 kΩ pull-up
DRAM_D17	AA8	NVCC_DRAM	DDR	mmdc.DRAM_D[17]	Input	100 kΩ pull-up
DRAM_D18	AB9	NVCC_DRAM	DDR	mmdc.DRAM_D[18]	Input	100 kΩ pull-up
DRAM_D19	Y9	NVCC_DRAM	DDR	mmdc.DRAM_D[19]	Input	100 kΩ pull-up
DRAM_D20	Y7	NVCC_DRAM	DDR	mmdc.DRAM_D[20]	Input	100 kΩ pull-up
DRAM_D21	Y8	NVCC_DRAM	DDR	mmdc.DRAM_D[21]	Input	100 kΩ pull-up
DRAM_D22	AC8	NVCC_DRAM	DDR	mmdc.DRAM_D[22]	Input	100 kΩ pull-up
DRAM_D23	AA9	NVCC_DRAM	DDR	mmdc.DRAM_D[23]	Input	100 kΩ pull-up
DRAM_D24	AE9	NVCC_DRAM	DDR	mmdc.DRAM_D[24]	Input	100 kΩ pull-up
DRAM_D25	Y10	NVCC_DRAM	DDR	mmdc.DRAM_D[25]	Input	100 kΩ pull-up
DRAM_D26	AE11	NVCC_DRAM	DDR	mmdc.DRAM_D[26]	Input	100 kΩ pull-up
DRAM_D27	AB11	NVCC_DRAM	DDR	mmdc.DRAM_D[27]	Input	100 kΩ pull-up
DRAM_D28	AC9	NVCC_DRAM	DDR	mmdc.DRAM_D[28]	Input	100 kΩ pull-up
DRAM_D29	AD9	NVCC_DRAM	DDR	mmdc.DRAM_D[29]	Input	100 kΩ pull-up
DRAM_D30	AD11	NVCC_DRAM	DDR	mmdc.DRAM_D[30]	Input	100 kΩ pull-up
DRAM_D31	AC11	NVCC_DRAM	DDR	mmdc.DRAM_D[31]	Input	100 kΩ pull-up
DRAM_D32	AA17	NVCC_DRAM	DDR	mmdc.DRAM_D[32]	Input	100 kΩ pull-up
DRAM_D33	AA18	NVCC_DRAM	DDR	mmdc.DRAM_D[33]	Input	100 kΩ pull-up
DRAM_D34	AC18	NVCC_DRAM	DDR	mmdc.DRAM_D[34]	Input	100 kΩ pull-up
DRAM_D35	AE19	NVCC_DRAM	DDR	mmdc.DRAM_D[35]	Input	100 kΩ pull-up
DRAM_D36	Y17	NVCC_DRAM	DDR	mmdc.DRAM_D[36]	Input	100 kΩ pull-up
DRAM_D37	Y18	NVCC_DRAM	DDR	mmdc.DRAM_D[37]	Input	100 kΩ pull-up
DRAM_D38	AB19	NVCC_DRAM	DDR	mmdc.DRAM_D[38]	Input	100 kΩ pull-up
DRAM_D39	AC19	NVCC_DRAM	DDR	mmdc.DRAM_D[39]	Input	100 kΩ pull-up
DRAM_D40	Y19	NVCC_DRAM	DDR	mmdc.DRAM_D[40]	Input	100 kΩ pull-up
DRAM_D41	AB20	NVCC_DRAM	DDR	mmdc.DRAM_D[41]	Input	100 kΩ pull-up
DRAM_D42	AB21	NVCC_DRAM	DDR	mmdc.DRAM_D[42]	Input	100 kΩ pull-up
DRAM_D43	AD21	NVCC_DRAM	DDR	mmdc.DRAM_D[43]	Input	100 kΩ pull-up
DRAM_D44	Y20	NVCC_DRAM	DDR	mmdc.DRAM_D[44]	Input	100 kΩ pull-up
DRAM_D45	AA20	NVCC_DRAM	DDR	mmdc.DRAM_D[45]	Input	100 kΩ pull-up
DRAM_D46	AE21	NVCC_DRAM	DDR	mmdc.DRAM_D[46]	Input	100 kΩ pull-up

DRAM_D47	AC21	NVCC_DRAM	DDR	mmdc.DRAM_D[47]	Input	100 kΩ pull-up
DRAM_D48	AC22	NVCC_DRAM	DDR	mmdc.DRAM_D[48]	Input	100 kΩ pull-up
DRAM_D49	AE22	NVCC_DRAM	DDR	mmdc.DRAM_D[49]	Input	100 kΩ pull-up
DRAM_D50	AE24	NVCC_DRAM	DDR	mmdc.DRAM_D[50]	Input	100 kΩ pull-up
DRAM_D51	AC24	NVCC_DRAM	DDR	mmdc.DRAM_D[51]	Input	100 kΩ pull-up
DRAM_D52	AB22	NVCC_DRAM	DDR	mmdc.DRAM_D[52]	Input	100 kΩ pull-up
DRAM_D53	AC23	NVCC_DRAM	DDR	mmdc.DRAM_D[53]	Input	100 kΩ pull-up
DRAM_D54	AD25	NVCC_DRAM	DDR	mmdc.DRAM_D[54]	Input	100 kΩ pull-up
DRAM_D55	AC25	NVCC_DRAM	DDR	mmdc.DRAM_D[55]	Input	100 kΩ pull-up
DRAM_D56	AB25	NVCC_DRAM	DDR	mmdc.DRAM_D[56]	Input	100 kΩ pull-up
DRAM_D57	AA21	NVCC_DRAM	DDR	mmdc.DRAM_D[57]	Input	100 kΩ pull-up
DRAM_D58	Y25	NVCC_DRAM	DDR	mmdc.DRAM_D[58]	Input	100 kΩ pull-up
DRAM_D59	Y22	NVCC_DRAM	DDR	mmdc.DRAM_D[59]	Input	100 kΩ pull-up
DRAM_D60	AB23	NVCC_DRAM	DDR	mmdc.DRAM_D[60]	Input	100 kΩ pull-up
DRAM_D61	AA23	NVCC_DRAM	DDR	mmdc.DRAM_D[61]	Input	100 kΩ pull-up
DRAM_D62	Y23	NVCC_DRAM	DDR	mmdc.DRAM_D[62]	Input	100 kΩ pull-up
DRAM_D63	W25	NVCC_DRAM	DDR	mmdc.DRAM_D[63]	Input	100 kΩ pull-up
DRAM_DQM0	AC3	NVCC_DRAM	DDR	mmdc.DRAM_DQM[0]	Output	Low
DRAM_DQM1	AC6	NVCC_DRAM	DDR	mmdc.DRAM_DQM[1]	Output	Low
DRAM_DQM2	AB8	NVCC_DRAM	DDR	mmdc.DRAM_DQM[2]	Output	Low
DRAM_DQM3	AE10	NVCC_DRAM	DDR	mmdc.DRAM_DQM[3]	Output	Low
DRAM_DQM4	AB18	NVCC_DRAM	DDR	mmdc.DRAM_DQM[4]	Output	Low
DRAM_DQM5	AC20	NVCC_DRAM	DDR	mmdc.DRAM_DQM[5]	Output	Low
DRAM_DQM6	AD24	NVCC_DRAM	DDR	mmdc.DRAM_DQM[6]	Output	Low
DRAM_DQM7	Y21	NVCC_DRAM	DDR	mmdc.DRAM_DQM[7]	Output	Low
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDR CLK	mmdc.DRAM_SDCLK0	Output	Low
DRAM_SDCLK_0_B	AE15					
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDR CLK	mmdc.DRAM_SDCLK1	Output	Low
DRAM_SDCLK_1_B	AE14					
DRAM_SDDQS_0	AE3	NVCC_DRAM	DDR CLK	mmdc.DRAM_SDDQS[0]	Output	Hi-Z
DRAM_SDDQS_0_B	AD3					
DRAM_SDDQS_1	AD6	NVCC_DRAM	DDR CLK	mmdc.DRAM_SDDQS[1]	Output	Hi-Z
DRAM_SDDQS_1_B	AE6					
DRAM_SDDQS_2	AD8	NVCC_DRAM	DDR CLK	mmdc.DRAM_SDDQS[2]	Output	Hi-Z
DRAM_SDDQS_2_B	AE8					
DRAM_SDDQS_3	AC10	NVCC_DRAM	DDR CLK	mmdc.DRAM_SDDQS[3]	Output	Hi-Z
DRAM_SDDQS_3_B	AB10					
DRAM_SDDQS_4	AD18	NVCC_DRAM	DDR CLK	mmdc.DRAM_SDDQS[4]	Output	Hi-Z
DRAM_SDDQS_4_B	AE18					
DRAM_SDDQS_5	AD20	NVCC_DRAM	DDR CLK	mmdc.DRAM_SDDQS[5]	Output	Hi-Z
DRAM_SDDQS_5_B	AE20					
DRAM_SDDQS_6	AD23	NVCC_DRAM	DDR CLK	mmdc.DRAM_SDDQS[6]	Output	Hi-Z
DRAM_SDDQS_6_B	AE23					
DRAM_SDDQS_7	AA25	NVCC_DRAM	DDR CLK	mmdc.DRAM_SDDQS[7]	Output	Hi-Z
DRAM_SDDQS_7_B	AA24					

Note[1]: The state immediately after reset and before ROM firmware or software has executed.

5.1.3 21 x 21 mm Ball Map

G	F	E	D	C	B	A	
DSI_D0P	NC	NC	CSI_D1M	GND	PCIE_RXM	NC	1
DSI_D0M	NC	NC	CSI_D1P	JTAG_TRSTB	PCIE_RXP	PCIE_REXT	2
GND	CSI_CLK0P	CSI_D0P	GND	JTAG_TMS	PCIE_TXP	PCIE_TXM	3
DSI_REXT	CSI_CLK0M	CSI_D0M	CSI_REXT	GND	GND	GND	4
JTAG_TDI	GND	GND	CLK2_P	CLK2_N	VDD_FA	FA_ANA	5
JTAG_TDO	GND	GND	GND	GND	USB_OTG_DN	USB_OTG_DP	6
PCIE_VPH	GND	GND	CLK1_P	CLK1_N	XTALO	XTALI	7
PCIE_VPTX	GND	NVCC_PLL_OUT	GND	GPANAIO	USB_OTG_CHD_B	GND	8
VDD_SNVS_CAP	VDDUSB_CAP	USB_OTG_VBUS	RTC_XTALI	RTC_XTALO	MLB_SP	MLB_SN	9
GND	USB_H1_DN	USB_H1_DP	USB_H1_VBUS	GND	MLB_DN	MLB_DP	10
VDD_SNVS_IN	PMIC_STBY_REQ	TAMPER	PMIC_ON_REQ	POR_B	MLB_CP	MLB_CN	11
NC	BOOT_MODE1	TEST_MODE	ONOFF	BOOT_MODE0	NC	NC	12
NC	SD3_DAT7	SD3_DAT6	SD3_DAT4	SD3_DAT5	SD3_CMD	GND	13
NVCC_SD3	SD3_DAT1	SD3_DAT0	SD3_CLK	NC	NC	NC	14
NVCC_NANDF	NANDF_CS0	NANDF_WP_B	SD3_RST	NANDF_CLE	SD3_DAT3	SD3_DAT2	15
NVCC_SD1	NANDF_D2	SD4_CLK	NANDF_CS3	NANDF_CS1	NANDF_RB0	NANDF_ALE	16
NVCC_SD2	SD4_DAT2	NANDF_D6	NANDF_D3	NANDF_D1	SD4_CMD	NANDF_CS2	17
NVCC_RGMII	SD1_DAT3	SD4_DAT4	SD4_DAT0	NANDF_D7	NANDF_D5	NANDF_D0	18
GND	SD2_CMD	SD1_DAT2	SD4_DAT7	SD4_DAT5	SD4_DAT1	NANDF_D4	19
EIM_D20	RGMII_TD1	SD2_DAT1	SD1_CLK	SD1_DAT1	SD4_DAT6	SD4_DAT3	20
EIM_D19	EIM_D17	RGMII_TD2	RGMII_TXC	SD2_CLK	SD1_CMD	SD1_DAT0	21
EIM_D25	EIM_D24	EIM_EB2	RGMII_RX_CTL	RGMII_TD0	SD2_DAT3	SD2_DAT0	22
EIM_D28	EIM_EB3	EIM_D22	RGMII_RD3	RGMII_TX_CTL	RGMII_RD1	SD2_DAT2	23
EIM_A17	EIM_A22	EIM_D26	EIM_D18	RGMII_RD0	RGMII_RD2	RGMII_TD3	24
EIM_A19	EIM_A24	EIM_D27	EIM_D23	EIM_D16	RGMII_RXC	GND	25
G	F	E	D	C	B	A	

Figure 9 Ball Map

R	P	N	M	L	K	J	H	
GPIO_17	CSI0_PIXCLK	CSI0_DAT4	CSI0_DAT10	CSI0_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P	1
GPIO_16	CSI0_DAT5	CSI0_VSYNC	CSI0_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M	2
GPIO_7	CSI0_DATA_EN	CSI0_DAT7	CSI0_DAT11	CSI0_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M	3
GPIO_5	CSI0_MCLK	CSI0_DAT6	CSI0_DAT14	CSI0_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P	4
GPIO_8	GPIO_19	CSI0_DAT9	CSI0_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK	5
GPIO_4	GPIO_18	CSI0_DAT8	CSI0_DAT18	CSI0_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD	6
GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP	7
GND	GND	GND	GND	GND	GND	GND	GND	8
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN	9
VDDSOC_CAP	GND	GND	GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP	10
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	11
GND	GND	NC	GND	GND	GND	GND	GND	12
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	13
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	14
GND	GND	GND	GND	GND	GND	GND	GND	15
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	16
GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	17
NVCC_DRAM	GND	GND	GND	GND	GND	GND	GND	18
NVCC_ENET	NVCC_LCD	DI0_DISP_CLK	NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25	19
DISP0_DAT13	DISP0_DAT4	DI0_PIN3	EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21	20
DISP0_DAT10	DISP0_DAT3	DI0_PIN15	EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31	21
DISP0_DAT8	DISP0_DAT1	EIM_BCLK	EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20	22
DISP0_DAT6	DISP0_DAT2	EIM_DA14	EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21	23
DISP0_DAT7	DISP0_DAT0	EIM_DA15	EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0	24
DISP0_DAT5	DI0_PIN4	DI0_PIN2	EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16	25
R	P	N	M	L	K	J	H	

Figure 10 Ball Map (continued)

AC	AB	AA	Y	W	V	U	T	
DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P	LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	1
DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N	LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	2
DRAM_DQM0	GND	LVDS1_TX3_N	LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	3
DRAM_D2	DRAM_D6	LVDS1_TX3_P	LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	4
DRAM_D13	DRAM_D12	DRAM_D3	GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	5
DRAM_DQM1	DRAM_D14	DRAM_D10	DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	6
DRAM_D15	DRAM_D16	GND	DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	7
DRAM_D22	DRAM_DQM2	DRAM_D17	DRAM_D21	GND	GND	GND	GND	8
DRAM_D28	DRAM_D18	DRAM_D23	DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN	9
DRAM_SDQS3	DRAM_SDQS3_B	GND	DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	10
DRAM_D31	DRAM_D27	DRAM_SDCKE1	DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	11
DRAM_A11	DRAM_SDBA2	DRAM_A14	DRAM_A15	GND	NVCC_DRAM	GND	GND	12
DRAM_A6	DRAM_A8	GND	DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	13
DRAM_A0	DRAM_A1	DRAM_A2	DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	14
DRAM_SDBA0	DRAM_RAS	DRAM_A10	DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	15
DRAM_SDODT0	DRAM_SDWE	GND	DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	16
DRAM_A13	DRAM_SDODT1	DRAM_D32	DRAM_D36	GND	NVCC_DRAM	GND	GND	17
DRAM_D34	DRAM_DQM4	DRAM_D33	DRAM_D37	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	18
DRAM_D39	DRAM_D38	GND	DRAM_D40	GND	GND	GND	GND	19
DRAM_DQM5	DRAM_D41	DRAM_D45	DRAM_D44	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	20
DRAM_D47	DRAM_D42	DRAM_D57	DRAM_DQM7	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	21
DRAM_D48	DRAM_D52	GND	DRAM_D59	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	22
DRAM_D53	DRAM_D60	DRAM_D61	DRAM_D62	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	23
DRAM_D51	GND	DRAM_SDQS7_B	GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12	24
DRAM_D55	DRAM_D56	DRAM_SDQS7	DRAM_D58	DRAM_D63	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9	25
AC	AB	AA	Y	W	V	U	T	

Figure 11 Ball Map (continued)

	AE	AD
1	GND	DRAM_D5
2	DRAM_D1	DRAM_D0
3	DRAM_SDQS0	DRAM_SDQS0_B
4	DRAM_D7	GND
5	DRAM_D9	DRAM_D8
6	DRAM_SDQS1_B	DRAM_SDQS1
7	DRAM_D11	GND
8	DRAM_SDQS2_B	DRAM_SDQS2
9	DRAM_D24	DRAM_D29
10	DRAM_DQM3	GND
11	DRAM_D26	DRAM_D30
12	DRAM_A9	DRAM_A12
13	DRAM_A5	GND
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0
16	DRAM_CAS	GND
17	ZQPAD	DRAM_CS1
18	DRAM_SDQS4_B	DRAM_SDQS4
19	DRAM_D35	GND
20	DRAM_SDQS5_B	DRAM_SDQS5
21	DRAM_D46	DRAM_D43
22	DRAM_D49	GND
23	DRAM_SDQS6_B	DRAM_SDQS6
24	DRAM_D50	DRAM_DQM6
25	GND	DRAM_D54
	AE	AD

Figure 12 Ball Map (continued)