1 General description of the project

The project goal is to design and generate layout and fabrication files for the PCB of an IOT (Internet-of-Things) system.

The IOT system, presented in figure 1, consists of:

1. A microcontroller (IC1) for acquiring data from sensors, management of the TCP/IP stack and hosting an application software;
2. An Ethernet interface circuit (IC8) for Internet connection through a RJ45 connector;
3. Four thermocouple measurement circuits (MAX6675) with serial interface;
4. A power supply;
5. Connectors (for power supply, I/O signals).

The IOT system, powered from a single 12V supply, can acquire 12 analog input signals, 4 thermocouple measurements and one isolated discrete input. The application software hosted by the microcontroller can process these signals and can make them available to worldwide access through the Ethernet connection.

The PCB of the system must be 120 x 80 mm in order to fit in a plastic enclosure. All I/O connectors must be placed as specified in figure 2. The PCB must also provide 4 holes as specified below. All components must be placed on the top side.

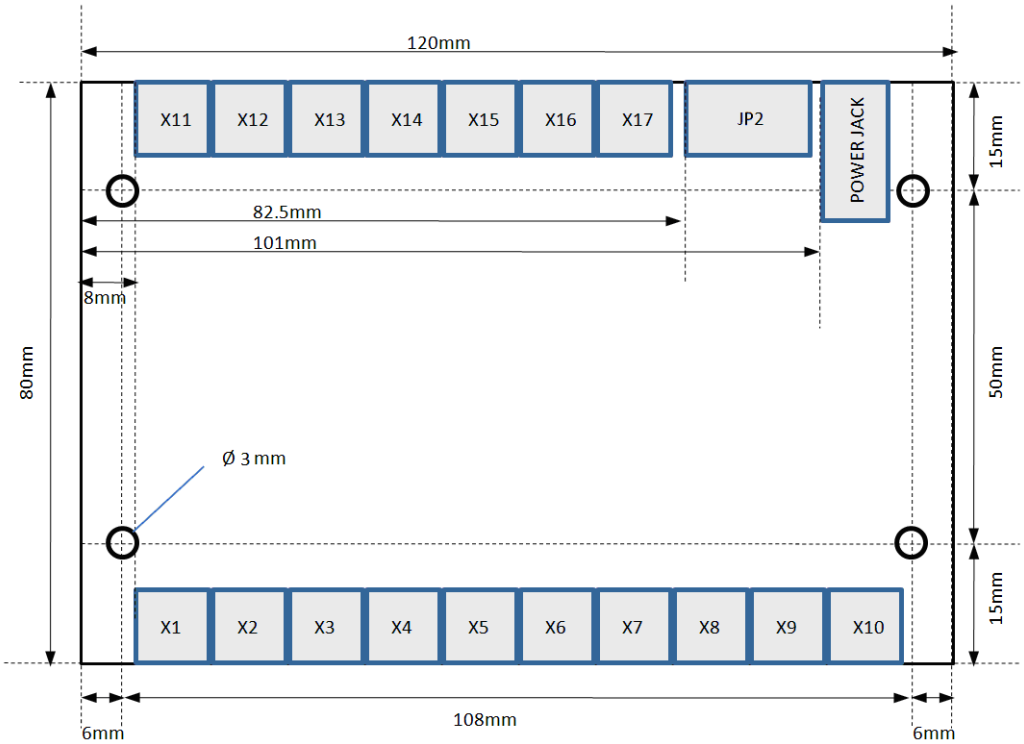

Figure 2. Top view of the IOT system PCB.

2 General requirements

GEN-001	The design order is mandatory: libraries, schematic design, transfer procedure, layout design and post-processing activities.
GEN-002	All dimensions must be considered in metric system.

3 Schematic design specifications (80 points)

SCH-001	The schematic project will be created using any CAD system accepted in the contest.
SCH-002	The components IC1, IC2 and IC8 will be created in a new library named with the last name (surname/family name) of the contestant.
SCH-003	The schematic must be drawn in a clear manner, e.g.: all references and values must have proper size and orientation, all references must be in accordance with table 1, un-necessary crossings must be avoided.

Notes: the schematic diagram must be electrically correct, clean and readable. The main purpose is to generate a correct netlist for PCB design, but it must also provide a clear representation of the functionality.

4 Mechanical design specifications (10 points)

MEC-001	The PCB geometry is specified in figure 2. Accepted tolerance is ±0.1 mm.
MEC-002	The PCB must have 4 non-plated holes (3 mm diameter) for PCB fixing screws and must accommodate all 4 screws in order to be fixed firmly. A clearance of 2 mm must be provided around holes.

5 Layout design specifications (145 points)

General rules: Critical signal traces must be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals, including noise carried on power and ground planes. Keeping the traces as short as possible can also reduce capacitive loading. Since the transmission line environment extends onto the printed circuit board, special attention must be paid to layout and routing of the differential signal pairs.

PCB-001	Components' footprints and layout guidelines are specified in the attached datasheets.
PCB-002	The layout design must take into consideration the next stack up: · Layer 1 – signal; · Layer 2 – ground plane; · Layer 3 – power plane; · Layer 4 – signal. Minimum trace width is 0.150 mm and minimum clearance is 0.150 mm.
PCB-003	Vias must be of 0.3mm drill diameter (except where otherwise stated), with a minimum annular ring of 0.15 mm. Only through hole vias are allowed.
PCB-004	Placement must follow the instructions given in figure 2.
PCB-005	All ICs must have a silkscreen marking for their reference pin (pin 1).
PCB-006	Minimum distance between 2 adjacent components is 0.5 mm, excepting connectors.
PCB-007	Minimum distance between components (including test pads) and outline of the PCB is 3 mm, excepting connectors.
PCB-008	A 10 mm x 10 mm copper area, covered by solder mask, must be placed on the PCB (for data matrix code).
PCB-009	IC3 must be provided with proper thermal pads/areas/clearance for cooling: 20 mm x 10 mm thermal area (both sides) and 0.3 mm drills for thermal vias on a 1.27 mm grid. (
PCB-010	Differential pair routing rules: · TPOUT+, TPOUT-, TPIN+, TPIN- must be routed as two differential pairs using 0.2mm width and 0.2mm spacing. The overall length of differential pairs must be less than 100 mm measured from the Ethernet device to the magnetics. The differential traces (within each pair) must be equal in total length to within 1.25 mm and as symmetrical as possible. · The two differential pairs are terminated with 49.9 Ω resistors, placed near the Ethernet controller. The C12 and C13 capacitors must be placed as close as possible (max. 3 mm) to the 49.9 ohm resistors, using a wide trace (0.5 mm width). No stubs are allowed on any differential net.

PCB-011	Differential pair clearance rules: · Do not route a pair of differential traces closer than 2.5 mm to another differential pair; · Do not route any other signal traces parallel to the differential traces and closer than 2.5 mm to the differential traces; · The reference plane for the differential pairs must be continuous (do not route differential pairs over splits in the associated reference plane as it may cause discontinuity in impedances).
PCB-012	Crystal routing rules: · Do not route traces and vias under crystals; · Traces between crystal and corresponding load capacitors must be as short as possible (max. 2.5 mm); · A local ground plane must be provided for each crystal circuitry.
PCB-013	Power and ground planes rules: · A dedicated area on the ground layer must be defined under JP2 connector, connected to the Shield pins of the connector (max. 0.3 mm clearance to the ground plane); · The Shield pins must not use thermal-relief.
PCB-014	Traces between decoupling capacitors and IC pins must be as short (max. 2.5 mm) and as wide as the width of the corresponding IC pad. Vias to the decoupling capacitors must be at least 0.6 mm in drill diameter.
PCB-015	The width of the high current traces for IC3 must be sized for a maximum current of 1.5 A ($\Delta T = 10°C$ and 35µm copper thickness).

6 Test specifications (9 points)

TST-001	Test pads (having 1mm copper diameter) must be placed on the bottom layer of the PCB for the following signals: SDI, SDO, SCK, GND. Test pads must be placed on a 2 mm grid.
TST-002	Global fiducial markers, having circular shape, must be introduced in a proper number, according to IPC7351 standard.
TST-003	Local fiducial markers must be placed for component IC1, according to IPC7351.

7 Fabrication specifications (6 points)

FAB-001	The fabrication files for all electrical layers must be created.
FAB-002	Distinct files for non-plated and plated holes must be provided.
FAB-003	A list of testpoint coordinates must be created, as a text file.

Total: 250 points

Crt. No.	Part	Value	Package	Description
1	C1, C2, C6, C12, C13, C24-C27	100nF	0603	CAPACITOR
2	C3, C4, C5, C7, C8, C10, C16, C18	10uF	1206	CAPACITOR
3	C9, C19	150pF	0805	CAPACITOR
4	C11, C17	2uF	see cap_pol datasheet	POLARIZED CAPACITOR
5	C14, C15, C22, C23	22pF	0805	CAPACITOR
6	C20, C21	18pF	0805	CAPACITOR
7	D1	1N5819	DO35	DIODE
8	D2	GF1	DO214BA	DIODE
9	IC8	ENC28J60-SO	SO28	Microchip 10Mbit Et
10	IC1	PIC24F32KA304	TQFP44	microcontroller
11	IC2	MC34063	DIP-8	DC/DC converter
12	IC3	REG1117	SOT223	800mA and 1A LDO
13	J1	POWER	see POWER_JACK_PTH datasheet	Power Jack
14	JP1	M20-9990245	see M20-9990245 datasheet	PIN HEADER
15	L1	1mH	0603	SMD Multilayer Inductor
16	L2, L3, L4, L5	10uH	0603	SMD Multilayer Inductor
17	L6, L8	330uH	see BS11 datasheet	INDUCTOR
18	L7, L9	200uH	0603	SMD Multilayer Inductor
19	IC9	PC817	DIP-4	SHARP OPTO COUPLER
20	Y1	40MHz	see CX2520DBxxxxxD0GEJ datasheet	CRYSTAL
21	Y2	80MHz	see CX2520DBxxxxxD0GEJ datasheet	CRYSTAL
22	Y3	25MHz	see CX2520DBxxxxxD0GEJ datasheet	CRYSTAL
23	R1	5K	1206	RESISTOR
24	R2, R6	200	1206	RESISTOR
25	R3	0R33	1206	RESISTOR
26	R4	16K	1206	RESISTOR
27	R5, R12, R13, R14, R40	10K	1206	RESISTOR
28	R7, R8, R9, R10	49R9	1206	RESISTOR
29	R11	2K	1206	RESISTOR
30	R15, R16, R17, R19, R21, R23, R27, R29, R31, R33, R35, R37	150	1206	RESISTOR
31	R39	1K	1206	RESISTOR
32	JP2	CJCBA8HF1Y0	see CJCBA8HF1Y0 datasheet	RJ45 connector
33	IC4 ... IC7	MAX6675	SO8	Thermocouple circuit
34	X1 ... X17	W237-102	see W237-102 datasheet	WAGO SCREW CLAMP

Table 1. BOM for IOT system.