

# Complementary MOSFET Half-Bridge (N- and P-Channel)

## PRODUCT SUMMARY

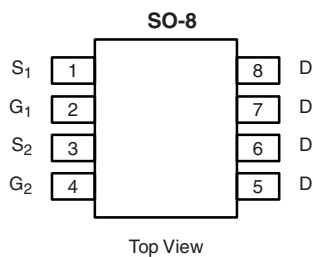
	$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
N-Channel	20	0.020 at $V_{GS} = 4.5$ V	9.1
		0.030 at $V_{GS} = 2.5$ V	7.5
P-Channel	- 20	0.060 at $V_{GS} = - 4.5$ V	- 5.3
		0.100 at $V_{GS} = - 2.5$ V	- 4.1

## FEATURES

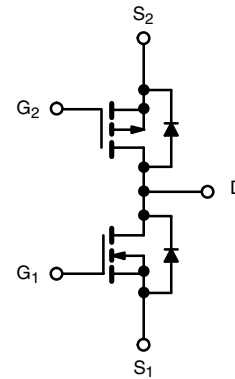
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



**Ordering Information:** Si4500BDY-T1-E3 (Lead (Pb)-free)  
Si4500BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)



## ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter		Symbol	N-Channel		P-Channel		Unit
			10 s	Steady State	10 s	Steady State	
Drain-Source Voltage		V <sub>DS</sub>	20		- 20		V
Gate-Source Voltage		V <sub>GS</sub>	± 12		± 12		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a,b</sup>	T <sub>A</sub> = 25 °C	I <sub>D</sub>	9.1	6.6	- 5.3	- 3.8	A
	T <sub>A</sub> = 70 °C		7.3	5.3	- 4.9	- 3.1	
Pulsed Drain Current		I <sub>DM</sub>	30		- 20		
Continuous Source Current (Diode Conduction) <sup>a,b</sup>		I <sub>S</sub>	2.1	1.1	- 2.1	- 1.1	
Maximum Power Dissipation <sup>a,b</sup>	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5	1.3	2.5	1.3	W
	T <sub>A</sub> = 70 °C		1.6	0.8	1.6	0.8	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150				°C

## THERMAL RESISTANCE RATINGS

Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ s	$R_{thJA}$	40	50	41	50	°C/W
	Steady State		75	95	75	95	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	20	22	23	26	

Notes:

a. Surface Mounted on FR4 board.

b.  $t \leq 10$  s.

SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions		Min.	Typ. <sup>a</sup>	Max.	Unit
Static							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	0.6		1.5	V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	P-Ch	- 0.6		- 1.5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V	N-Ch			± 100	nA
			P-Ch			± 100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	N-Ch			1	μA
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V	P-Ch			- 1	
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	N-Ch			5	
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	P-Ch			- 5	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	30			A
		V <sub>DS</sub> = - 5 V, V <sub>GS</sub> = - 4.5 V	P-Ch	- 20			
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9.1 A	N-Ch		0.016	0.020	Ω
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 5.3 A	P-Ch		0.048	0.060	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 3.3 A	N-Ch		0.024	0.030	
		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 1 A	P-Ch		0.082	0.100	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 9.1 A	N-Ch		29		S
		V <sub>DS</sub> = - 15 V, I <sub>D</sub> = - 5.3 A	P-Ch		11		
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.1 A, V <sub>GS</sub> = 0 V	N-Ch		0.8	1.2	V
		I <sub>S</sub> = - 2.1 A, V <sub>GS</sub> = 0 V	P-Ch		- 0.8	- 1.2	
Dynamic <sup>a</sup>							
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 9.1 A	N-Ch		11	17	nC
Gate-Source Charge	Q <sub>gs</sub>		P-Ch		6.0	9	
		Gate-Drain Charge	Q <sub>gd</sub>	P-Channel V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 5.3 A	N-Ch		
P-Ch					1.3		
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 6 Ω	N-Ch		35	50	ns
			P-Ch		20	30	
Rise Time	t <sub>r</sub>		N-Ch		50	80	
			P-Ch		35	60	
Turn-Off Delay Time	t <sub>d(off)</sub>	P-Channel V <sub>DD</sub> = - 10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ - 1 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 6 Ω	N-Ch		31	50	
			P-Ch		55	85	
Fall Time	t <sub>f</sub>		N-Ch		15	30	
			P-Ch		35	60	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.1 A, dI/dt = 100 A/μs	N-Ch		30	60	
		I <sub>F</sub> = - 2.1 A, dI/dt = 100 A/μs	P-Ch		25	50	

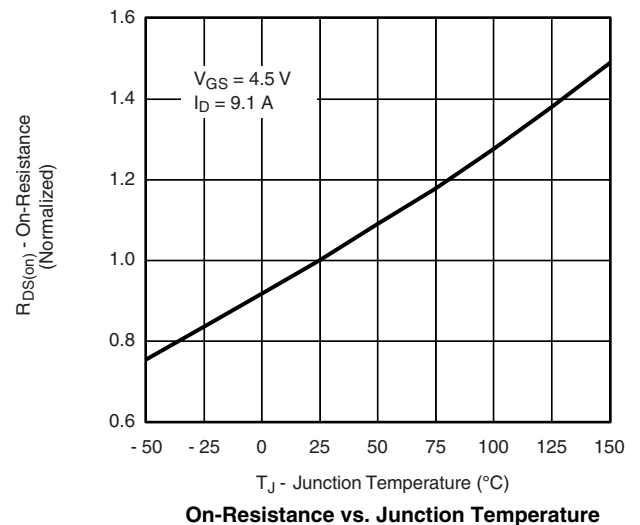
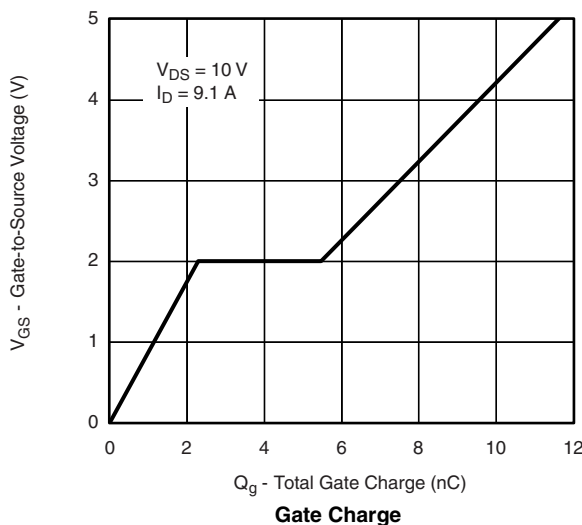
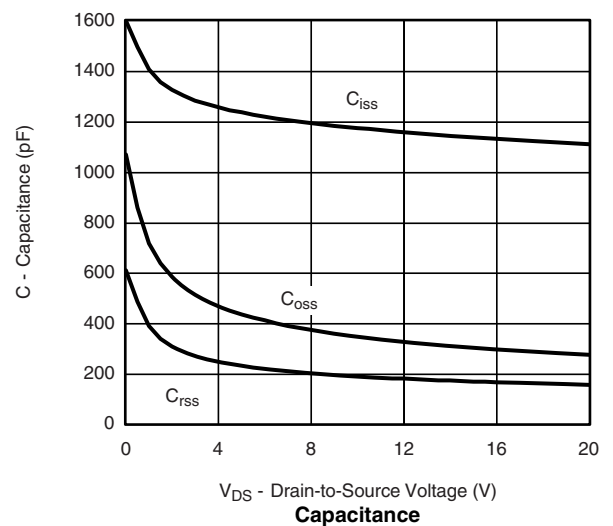
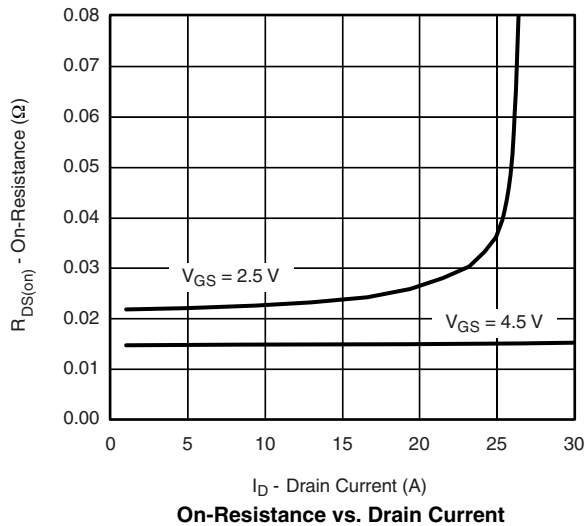
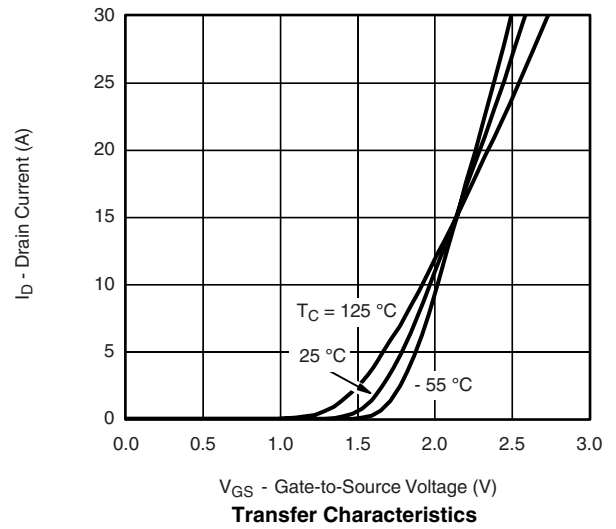
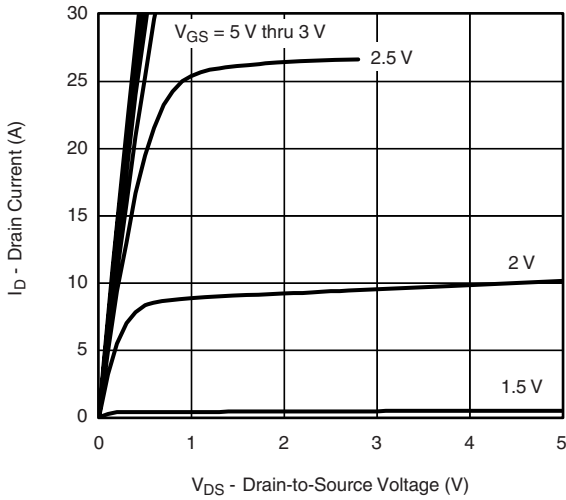
Notes:

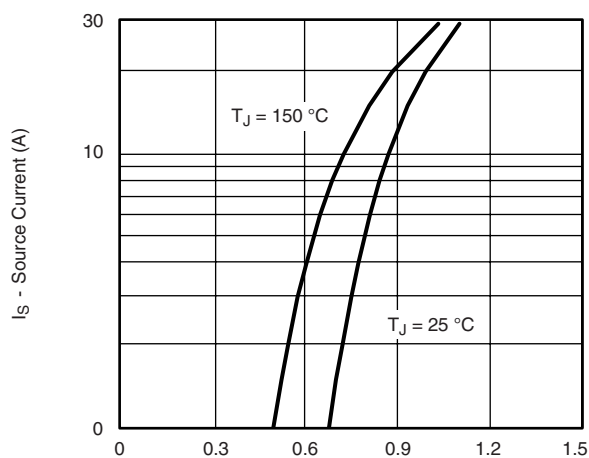
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

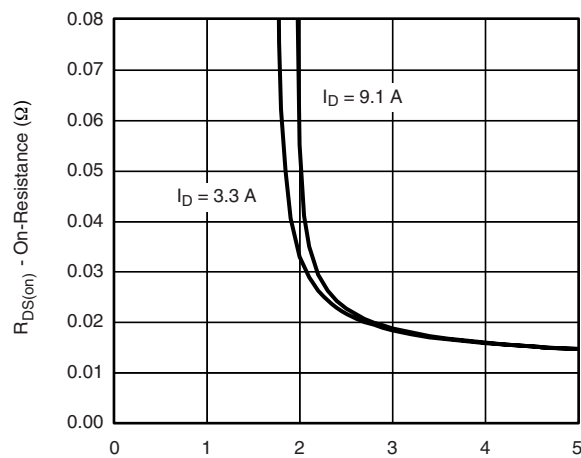
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

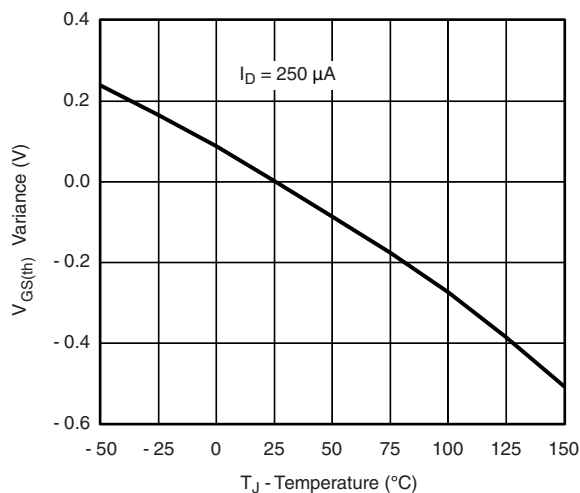


**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

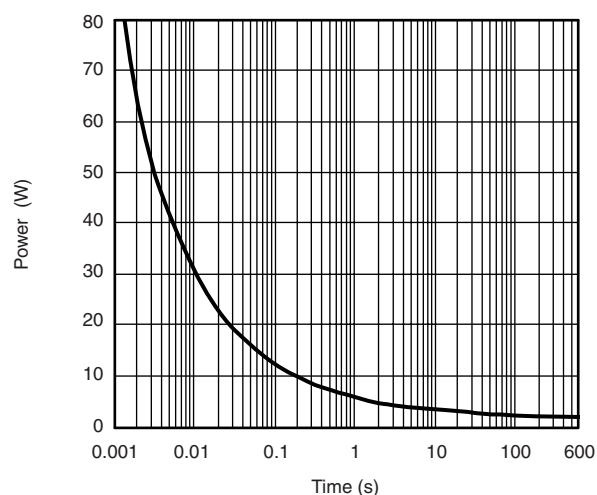
$V_{SD}$  - Source-to-Drain Voltage (V)  
Source-Drain Diode Forward Voltage



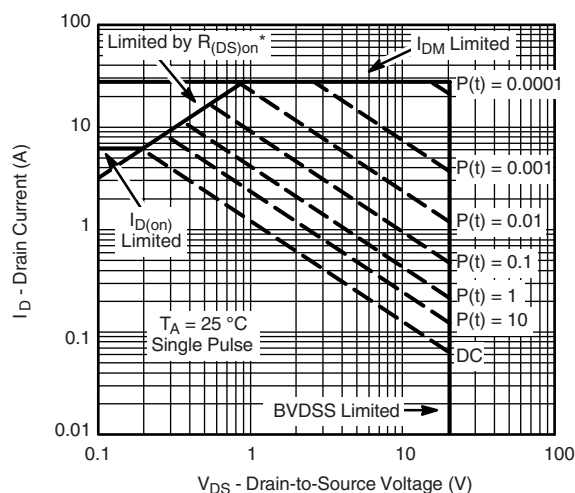
$V_{GS}$  - Gate-to-Source Voltage (V)  
On-Resistance vs. Gate-to-Source Voltage



$T_J$  - Temperature ( $^{\circ}\text{C}$ )  
Threshold Voltage



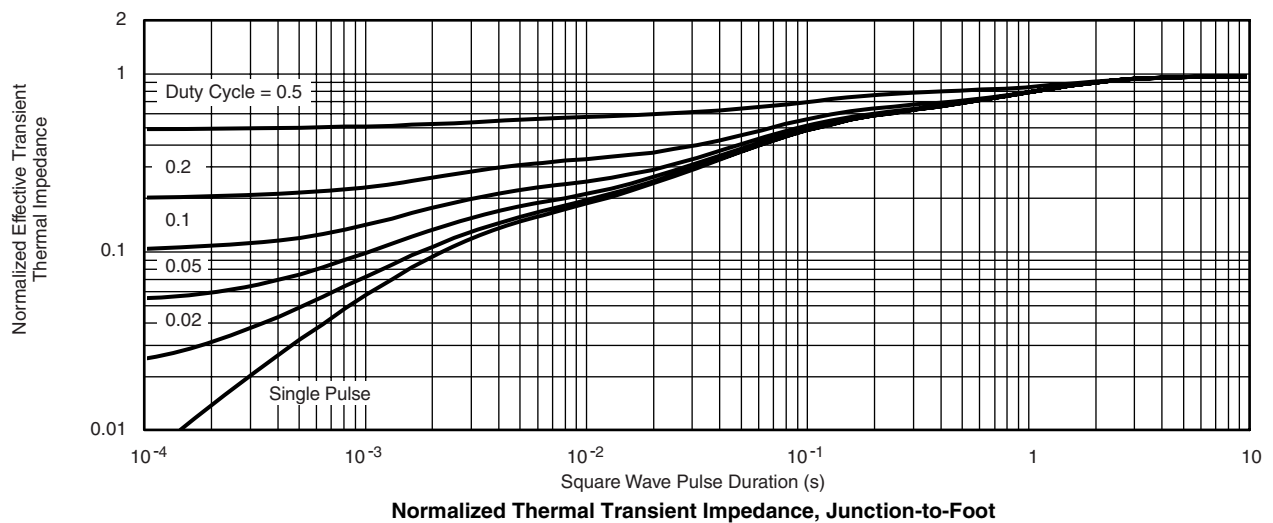
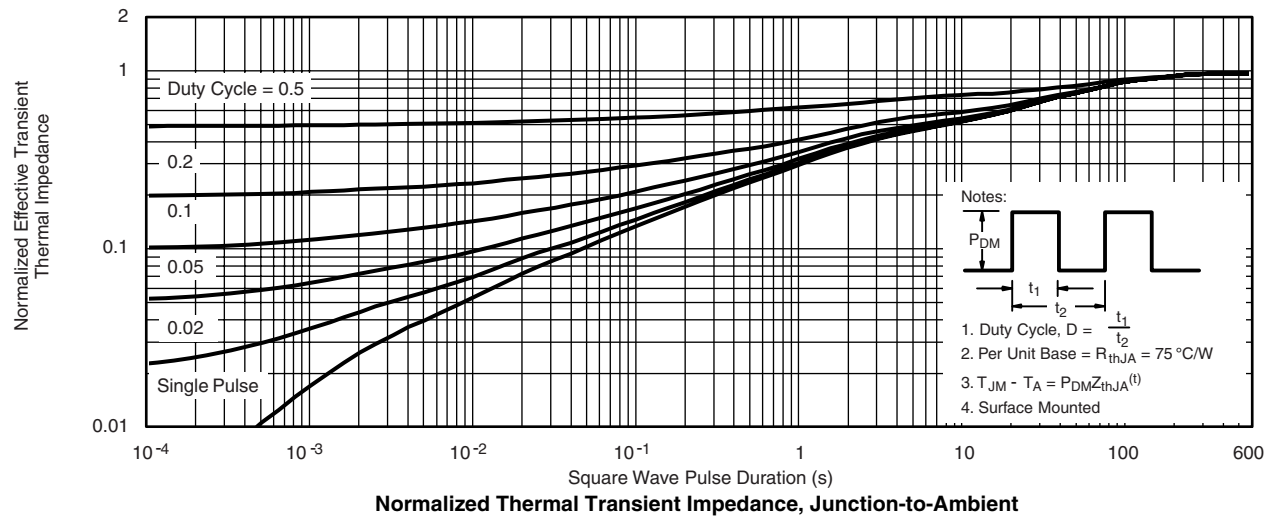
Single Pulse Power

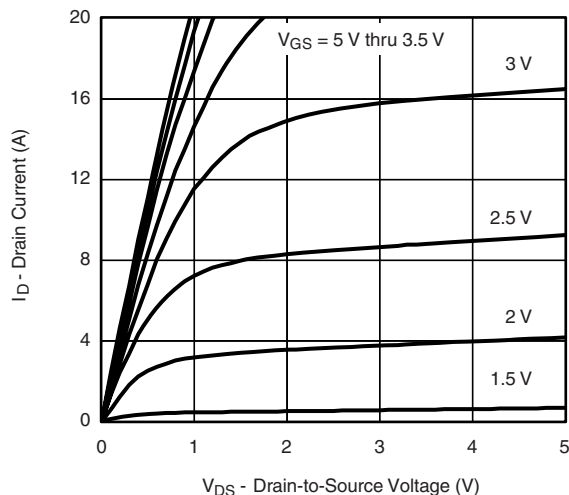
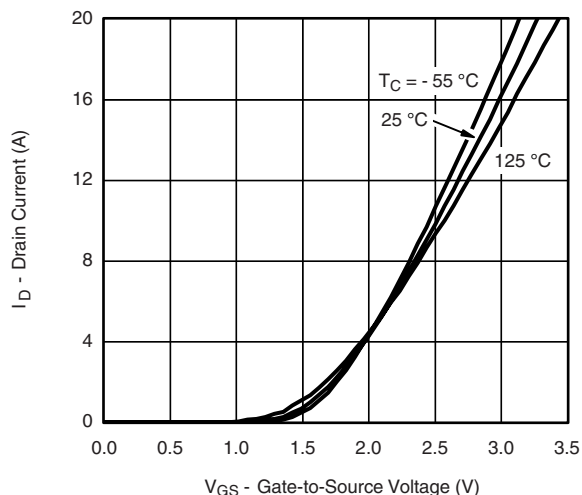
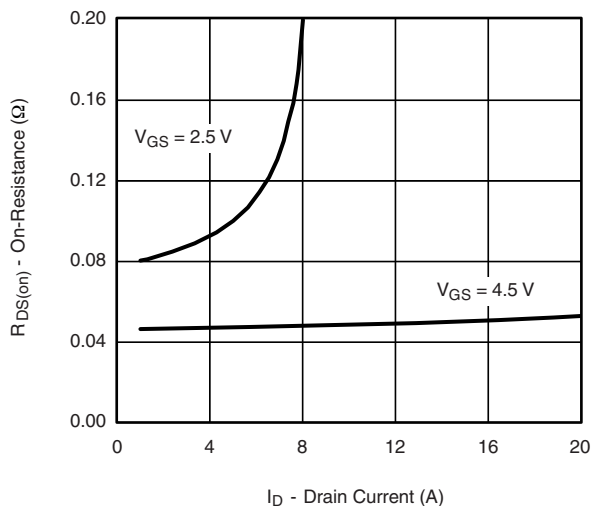
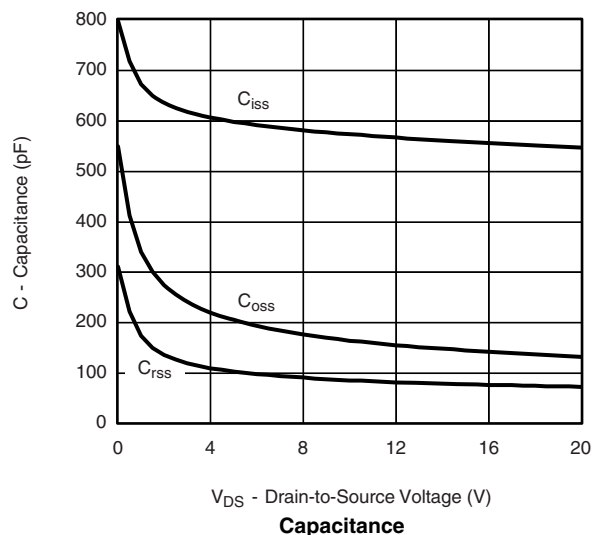
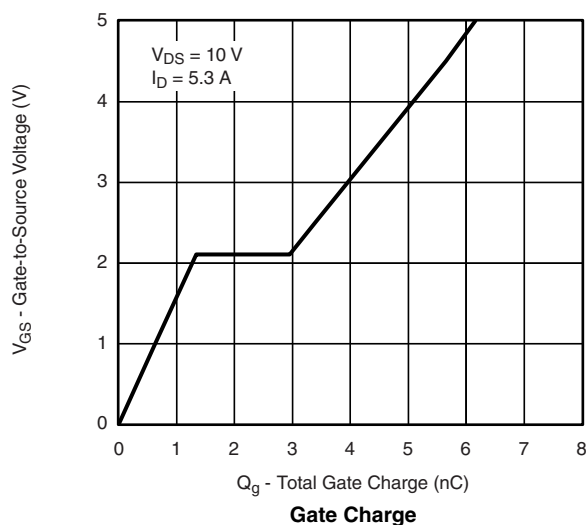
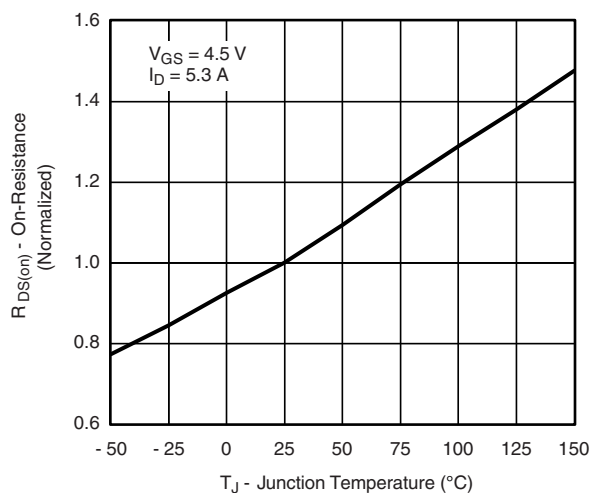


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

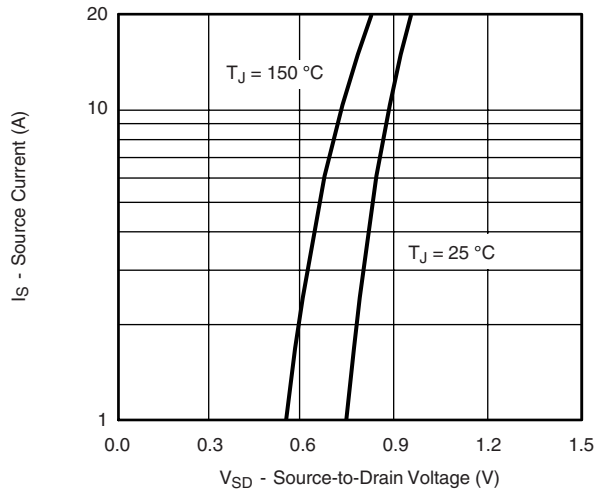
Safe Operating Area

**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

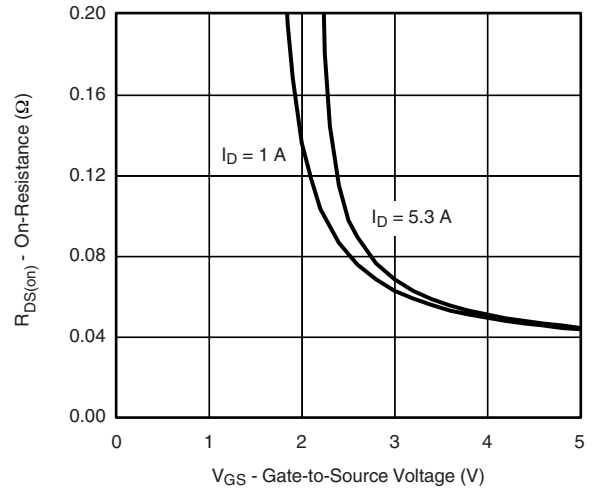


**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

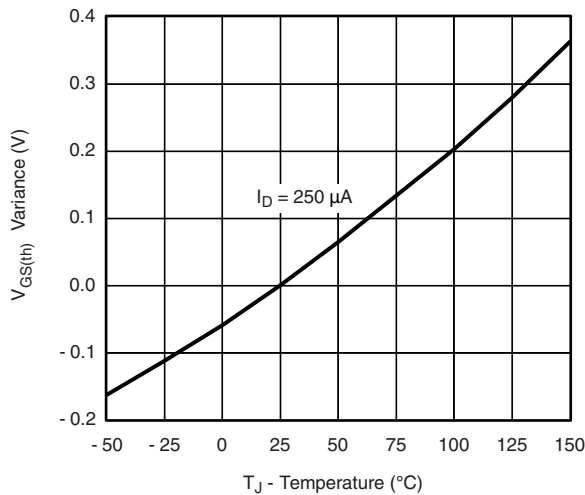
## P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



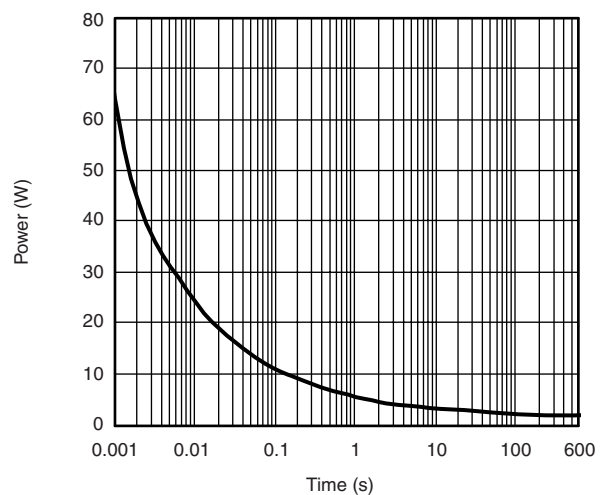
Source-Drain Diode Forward Voltage



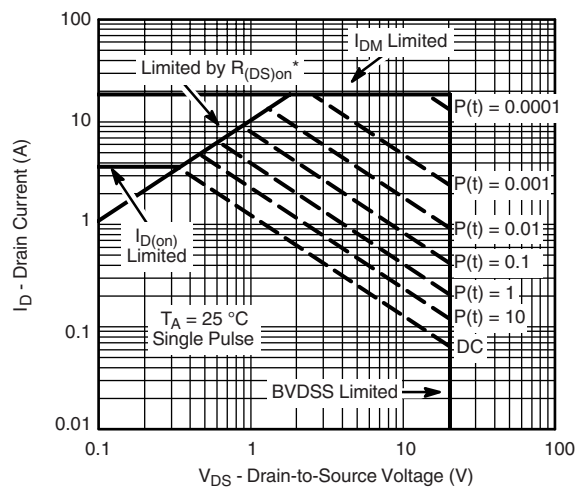
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

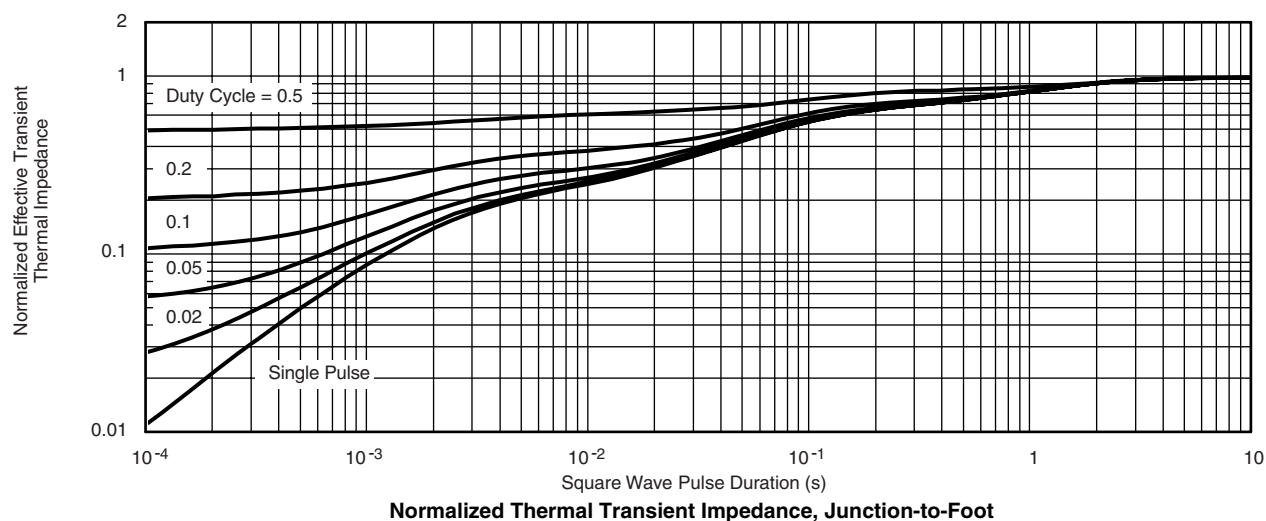
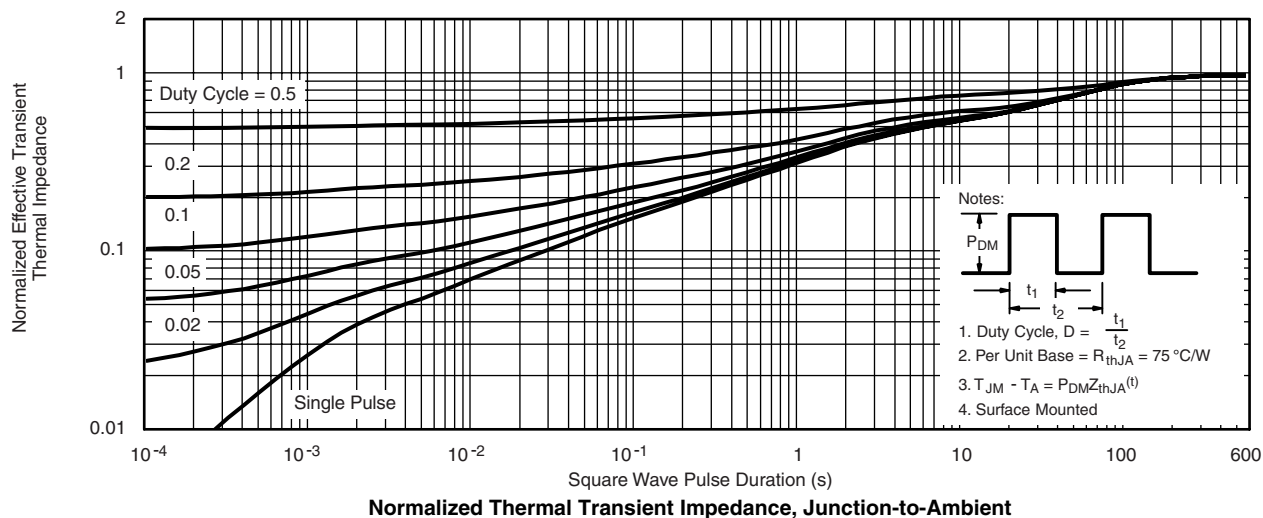


Single Pulse Power



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area

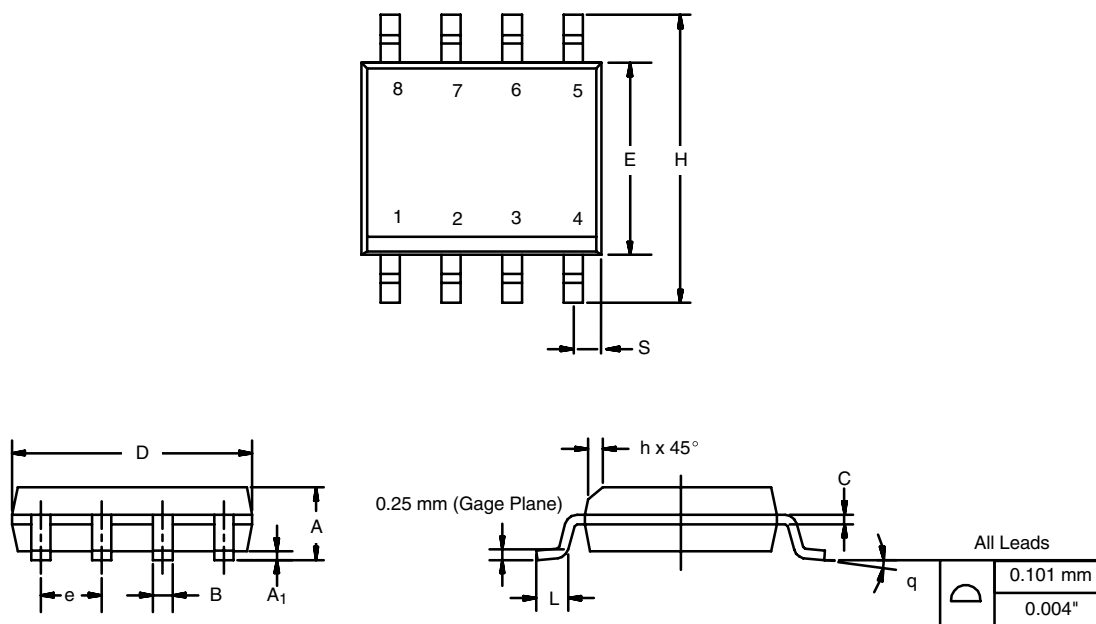
**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?72281](http://www.vishay.com/ppg?72281).



## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				



## Mounting LITTLE FOOT®, SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/ppg?72286>), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

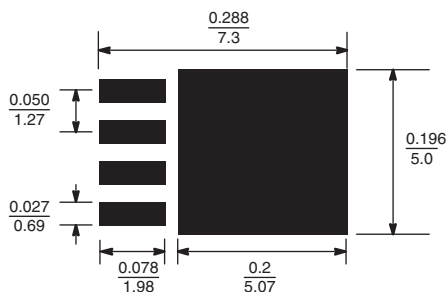


Figure 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

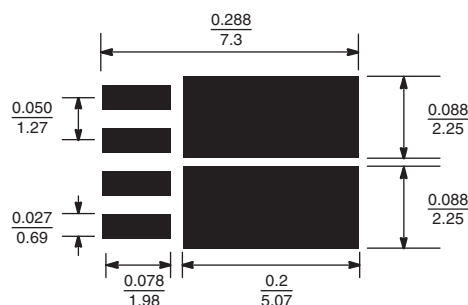


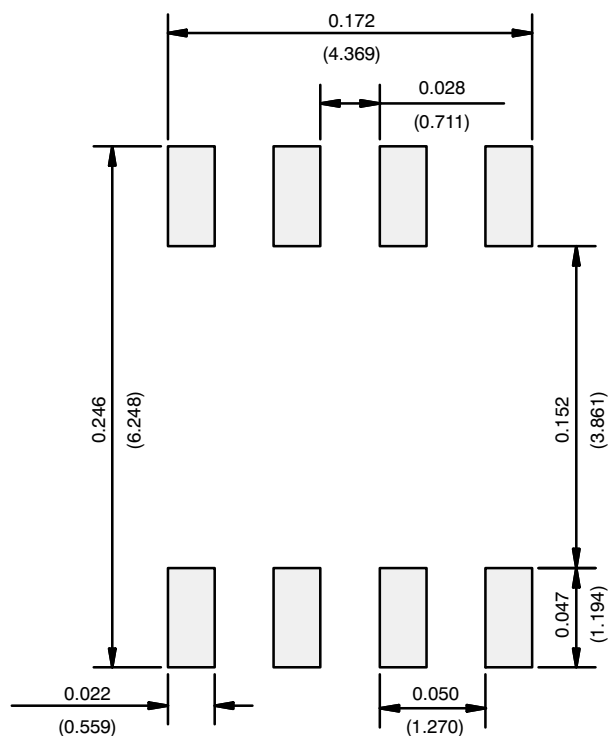
Figure 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**