Realize Your Product Promise®

ANSYS°

Slwave for Power Integrity Analysis

Workshop 2_2: PI Advisor

Opening or Importing a Project

Starting Slwave

- To launch SIwave, click the Microsoft Start Button > ALL Programs > ANSYS Electromagnetics > ANSYS Electromagnetics Suite 17.2.
- Select the ANSYS Slwave 2016 executable.
- ANSYS Electromagnetics
 ANSYS Electromagnetics Suite 16.2
 ANSYS Electromagnetics Suite 17.2
 ANSYS Corporate Website
 ANSYS Electronics Desktop 2016.2
 ANSYS EMIT 5.2
 ANSYS PEmag 2016.2
 ANSYS PExprt 2016.2
 ANSYS Savant 5.2
 ANSYS Simplorer 2016.2
 ANSYS Simplorer 2016.2
 Modify Integration with ANSYS 17.2
 Register with RSM

Open a Slwave Project

- Select the Open Project button
 - Browse for the file: Pl.siw,
 - Click the **Open** button





Slwave Workflow Wizard Dialogue

Opening the Workflow Wizard

• In the Common Functions menu, choose the **Slwave Workflow Wizard Dialogue**.



🔕 🛃 🔀 🗋 📂 🖌 🤊 🔍 🖛

3

ANSYS

Verify Stackup

	import import <td< th=""><th>Component Fil Stackup itackup 'adstacks Circuit Element</th><th>e Parameters</th><th>• Mo • Cli • Cli</th><th>dify Stac ck on the Ve - This is the s previous de ck Cancel to</th><th>kup and l erify Stackup stackup fron esign. close this w</th><th>Material button. h the origina vindow.</th><th>Properti</th><th>es /e would like to</th><th>use a st</th><th>ackup ge</th><th>nerated fi</th><th>rom a</th></td<>	Component Fil Stackup itackup 'adstacks Circuit Element	e Parameters	• Mo • Cli • Cli	dify Stac ck on the Ve - This is the s previous de ck Cancel to	kup and l erify Stackup stackup fron esign. close this w	Material button. h the origina vindow.	Properti	es /e would like to	use a st	ackup ge	nerated fi	rom a
	😤 Verify	Layer S	itack-up Editor										
•	**	Color	Name	Туре	Thickness (mm)	🏠 Material	Conductivity (S/m)	🆄 Dielectric Fill	Dielectric constant	Loss tangent	Translucency	Elevation (mm)	Roughne
	Accian S.n		UNNAMED_000	DIELECTRIC	0	EDB_AIR	0		1	0		2.03454	
	Assign 5 p		TOP	METAL	0.04826	EDB_COPPER	5.959E+07	EDB_TOP_FILL	4.5	0	60	1.98628	HJ: (
			UNNAMED_002	DIELECTRIC	0.06731	EDB_FR-4_3	0		3.86	0.024		1.91897	
1	Assign SPI		PWR	METAL	0.03302	EDB_COPPER_1	5.959E+07	EDB_PWR_FILL	4.5	0.035	60	1.88595	HJ: (
			UNNAMED_004	DIELECTRIC	1.27	EDB_FR-4_2	0		4.34	0.018		0.61595	
	Configure I		LYR_1	METAL	0.03048	EDB_COPPER_1	5.959E+07	EDB_FR-4_1	4.5	0.035	60	0.58547	HJ: (
			UNNAMED_006	DIELECTRIC	0.2032	EDB_FR-4_1	0		4.5	0.035		0.38227	
	Configure		LYR 2	METAL	0.03048	EDB COPPER 1	5.959E+07	EDB FR-4 1	4.5	0.035	60	0.35179	HJ:
			UNNAMED 008	DIELECTRIC	0.2032	EDB_FR-4_1	0		4.5	0.035		0.14859	
i ∕Always s	how this dialog after (GND	METAL	0.03302	EDB COPPER 1	5.959E+07	EDB FR-4 1	4.5	0.035	60	0.11557	HJ:
			UNNAMED 010	DIELECTRIC	0.06731	EDB FR-4	0		3.86	0.024		0.04826	
			BOTTOM	METAL	0.04826	EDB COPPER	5.959E+07	EDB BOTTOM FIL	LL 4.5	0	60	0	HJ: (
		•	UNNAMED 012	DIELECTRIC	0	EDB AIR	0		1	0		0	
		Add / D Add Ad	elete Layer(s) d Above Selected La ld Below Selected Layer Delete Selected Layer	yer Ed Co Na yer Ty 's Ma	it Selected Layer(s) lor me As Is pe DIELECTRIC terial As Is		Update Update Update Update	Dielectric Fill Translucency Thickness Roughness	As Is	mm [Update Update Update Update		
		Select all	DIELECTRIC -	layers App	ly	Edit Material Prop	perties	Units II	nm 🔻			ОК	

April 5, 2017

х

Elevation (mm) Roughness (mm)

HJ: 0 , HJ: 0

Cancel

4

© 2016 ANSYS, Inc.

Import Stackup

	Import Component File						
	Import Stackup						
	i Verify Stackup						
	Verify Padstacks						
	Verify Circuit Element Parameters						
D	Verify Power/Ground Net Classification.						
D	Sanitize Layout for Simulation						
	Assign S-parameter Capacitor Models						
	Assign SPICE Netlists						
	Configure DC IR Drop Analysis						
	Configure PI Analysis						

• Importing a Stackup from a Previous Design

- Click the Import Stackup button.
- Locate WS2_STACKUP.stk in the same directory as Pl.siw.
- Click **Open** to apply the stackup.

Open				x
😋 🕞 🗕 🕨 Computer	► Local Disk (C:) ► Training ► WS2	▼ 4	Search WS2	٩
Organize 🔻 New folder			:==	• 🔟 🔞
😰 ScanSnap Folder 🔺	Name	Date modified	Туре	Size
E Libraries	🚳 PI.siw	1/12/2015 1:29 PM	Ansoft SIwave file	2,518 KB
Documents	WS2_STACKUP.stk	1/13/2015 4:20 PM	STK File	12 KB
J Music				
📔 Pictures 🗧				
Subversion				
H Videos				
💻 Computer				
🚢 Local Disk (C:)				
👝 Local Disk (E:) 🚽				
File <u>n</u> ar	ne: WS2_STACKUP.stk	•	All Files (*.*)	•
			<u>O</u> pen	Cancel



Verify Stackup

×

•



6

Verify Imported Stackup

- Click on the Verify Stackup button once again.
 - Importing the stackup from the last step has modified the material for metal layers. Importing the stackup can modify any and all parameters in this window.
 - Verify that copper is assigned to all of the metal layers.
- Click **Cancel** to close this window.

	Color	Name	Туре		🏝 Material	Conductivity (S/m)	🏝 Dielectric Fill	Dielectric constant	Loss tangent	Translucency	Elevation (mils)	Roughness (mils)
ian S-narameter		UNNAMED_000	DIELECTRIC	0	EDB_AIR	0		1	0		80.1	
gir 5 parameter		TOP	METAL	1.9	copper	5.8E+07	EDB_TOP_FILL	4.5	0	60	78.2	HJ: 0 , HJ: 0
a CDICE Matlia		UNNAMED_002	DIELECTRIC	2.65	EDB_FR-4_3	0		3.86	0.024		75.55	
1 SPICE INEUIS		PWR	METAL	1.3	copper	5.8E+07	EDB_PWR_FILL	4.5	0.035	60	74.25	HJ: 0 , HJ: 0
		UNNAMED_004	DIELECTRIC	50	EDB_FR-4_2	0		4.34	0.018		24.25	
jure DC IR Dr		LYR_1	METAL	1.2	copper	5.8E+07	EDB_FR-4_1	4.5	0.035	60	23.05	HJ: 0 , HJ: 0
		UNNAMED_006	DIELECTRIC	8	EDB_FR-4_1	0		4.5	0.035		15.05	
ure PI Analys		LYR_2	METAL	1.2	copper	5.8E+07	EDB_FR-4_1	4.5	0.035	60	13.85	HJ: 0 , HJ: 0
after project impod		UNNAMED_008	DIELECTRIC	8	EDB_FR-4_1	0		4.5	0.035		5.85	
g arter project import		GND	METAL	1.3	copper	5.8E+07	EDB_FR-4_1	4.5	0.035	60	4.55	HJ: 0 , HJ: 0
		UNNAMED_010	DIELECTRIC	2.65	EDB_FR-4	0		3.86	0.024		1.9	
		BOTTOM	METAL	1.9	copper	5.8E+07	EDB_BOTTOM_FILL	4.5	0	60	0	HJ: 0 , HJ: 0
		UNNAMED_012	DIELECTRIC	0	EDB_AIR	0		1	0		0	
Add / Delete Layer(s) Edit Selected Layer(s) Add Above Selected Layer Color Add Below Selected Layer Name												
	Add Add	Above Selected La	yer	Color As Is Name As Is			date Dielectric	Fill As Is	<u>(</u>)	Up Up Up Up	date date	

April 5, 2017

Assign S-parameter Capacitor (and Inductor) Models

SIwave Work	flow Wizard
	Import Component File
	Import Stackup
\bigcirc	😸 Verify Stackup
0	Verify Padstacks
0	Verify Circuit Element Parameters
	Verify Power/Ground Net Classification
	Sanitize Layout for Simulation
	Assign S-parameter Capacitor Models
	Assign SPICE Netlists
	Configure DC IR Drop Analysis
	Configure PI Analysis
	ow this dialog after project import

Assigning Broadband Models to Capacitor Locations

- For this exercise, we will assume that the Padstacks, Circuit Elements, and Power/Ground Net Classification has been handled properly during import.
- Click on the Assign S-parameter Capacitor Models button.
- Click Auto Match By Value.
 - The auto-match function looks at the original capacitance value and the estimated size and attempts to choose a suitable part from Slwave's vendor library. The vendor library includes over 20,000 capacitor and inductor models directly from 12 of the major vendors.
- Click **OK** to commit changes.

Local Part Name	Туре	Value	Size Est.	Manufacturer	Series	Part Name	Matched Value	Matched S
602431-005	Capacitor	470.000000 pF	0603	Kemet	C0603C	C0603C471K5GAC	470.00000 pF	0603
602433-026	Capacitor	2.200000 uF	0603	TDK	C1608	C1608JB1C225K	2.200000 uF	0603
602433-038	Capacitor	4.700000 uF	0603	TDK	C1608	C1608JB1A475K	4.700000 uF	0603
602433-057	Capacitor	47.000000 nF	0603	Panasonic	S-para	ECJ1VB1E473K	47.000000 nF	0603
602433-075	Capacitor	10.000000 uF	0603	Kemet	C0603C	C0603C106K9PAC	10.000000 uF	0603
602433-081	Capacitor	22.000000 uF	0603	Samsung	1608	CL10A226MP8N	22.000000 uF	0603
644066-030	Capacitor	100.00000 uF	1410	Murata	GWM32	GWM32RJ10E10	100.00000 uF	1210
644066-115	Capacitor	47.000000 uF	1206	TDK	C3216	C3216JB0J476M	47.00000 uF	1206
A32422-019	Inductor	1.000000 nH	2816	Coilcraft	0402CS	0402CS-1N0	1.000000 nH	Other
A36094-025	Capacitor	10.00000 pF	0402	Panasonic	S-para	ECDG0E100C	10.000000 pF	0402
100005-040	<u> </u>	10.000000 5	0.400		A 00400	04007040000044	10.000000 5	0.000
Auto Match By Va	alue Model			Auto Match By N Clear Model Assi	lame gnment		Import Part Export Part	Matching Fil Matching Fil
Import S-parameter Model OK Cancel								

Release 2016.0

7

PI Simulation Ports





8

PI Simulation Ports

Single active device to simplify simulation results.





Configure PI Analysis

SIwave Work	flow Wizard	×						
	Import Component File							
	import Stackup							
	😸 Verify Stackup							
0	Verify Padstacks							
0								
•	Verify Power/Ground Net Classificatio	n						
	Sanitize Layout for Simulation							
	Assign S-parameter Capacitor Models.	PI Config						
	Assign SPICE Netlists	AGND_ BST_V						
	Configure DC IR Drop Analysis	BST_V						
	Configure PI Analysis	GND RMII_S						
∠Aways sho	w this dialog after project import	V1P05						

Table Driven Schematic

- Place a check mark next to net V3P3_S0.
 - This displays any active devices connected to this net.
 - Check and uncheck Hide RLC components to see passive devices.
- Assign a Port to U2A5 and U2M1.
 - This was chosen only for simplification. It is possible to create ports for any and all components.
 - The default reference impedance is 0.10hm to resolve very small impedances.
- Click Configure Simulation.

Assign S-parameter Capacitor Models.	PI Configuration	_								
Assign SPICE Netlists	AGND_VCC		Ref. Des.	Part Number	Positive Net	Reference Net	Port	Ref. Imp.		
Absign of rectification	BST_V1P0_S0		CR3M1	C52251-001	V3P3_S0	VCC_FLASH	None			
Confirmer DC IB Dave Analysis	BST_V1P5_S5		FB1M1	656554-032	V3P3_S0	V3P3_S0_A	None			
Configure DC IR Drop Analysis	BST_V3P3_S5		J4A2	G46739-001	V3P3_S0	GND	None			
	GND		Q1L1	C81974-001	V3P3_S0	V3P3_S0	None			
Configure PI Analysis	RMII_S0_PFB		Q1L2	C81974-001	V3P3_S0	V3P3_S0	None			
wave show this dialog after project import	V 1P05_S0_IVR		U1L1	D30400-001	V3P3_S0	GND	None			
2 ,	V1P0_S0		U1L2	D30400-001	V3P3_S0	GND	None			
	V 1P0_S3_IVR		U1L3	D30400-001	V3P3_S0	GND	None			
	V1P0_S5_IVR		U1L4	D30400-001	V3P3_S0	GND	None			
	V1P5_S0		U2A5	IPD031-201	V3P3_S0	GND	Port	0.1ohm		
	V1P5_S3		U2B1	G83474-001	V3P3_S0	GND	None			
	V1P5_S5		U2M1	G94441-001	V3P3_S0	GND	Port	0.1ohm		
	V 1P8_S0_IVR		U3B2	C76254-001	V3P3_S0	GND	None			
	V1P8_S3_IVR	_	U4B1	G60296-001	V3P3_S0	GND	None			
	V3P3_S0		U10	G63512-001	V3P3_S0	GND	None			
	V3P3_S0_A									
	V3P3_S3		Load	Save	Port Naming Co	nvention	Hide RI C comp	onents		
	V3P3_S5									
	V5_ALW_ON									
	V5_PWR_JACK	- 1	Co	nfigure Simula	tion		Validate		Simulate.	
	VBUS1	•		ingule binitula			- arreation			



Validation Check

Iwave Work	dlow Wizard	•
	Import Component File	
	Import Stackup	
	😸 Verify Stackup	
	Verify Padstacks	•
	Verify Circuit Element Parameters	
	Verify Power/Ground Net Classification	n
	Sanitize Layout for Simulation	
	Assign S-parameter Capacitor Models	Launch Va
	Assign SPICE Netlists	Check I
	Configure DC IR Drop Analysis	Se
	Configure PI Analysis	🔽 Self
Always shi	ow this dialog after project import	V Disj
		DC-

Validation Check

- The validation check analyzes the entire setup to ensure it is ready for simulation.
- Increase the **Number of cores to use** for this validation step by pressing the up button.
- Click **OK** to start the validation check.

Validation Check Results

- The Validation Check can automatically repair certain geometry problems such as disjoint nets and overlapping vias.
- Press **OK** to close this window and apply any Auto Fix.

ameter Capacitor Models	Launch Validation Check	×	- Circular Loops:
: Netlists C IR Drop Analysis	Check List Select All Unselect All	Select a simulation mode SYZ-Parameters	- Others: Point-Connections: Disjoint Nets:
Analysis	 Self-Intersecting Polygons Disjoint Nets (Floating Nodes) DC-Short Errors Identical/Overlapping Vias Bondwire Collisions 	Minimum Area: 2 mm^2 Cutouts that are smaller than this minimum area will be ignored during validation check. This threshold can be changed in the Simulation -> Global Option window.	Identical/Overlappin Traces-Inside-Trace Collisions of Bondwir Illegal Connections (Identical Bondwires: Reversed Bondwires:
	 Illegal Bondwire Connections Misalignments Less Than Two Terminals 	Nets to be checked Some nets might not be included. Please refer the Simulation -> Global Option window. Number of cores to use: 4	Zero Via Plating: Nets With Less Than Warnings Misalignments (Plane Bondwires Misaligne Pins Shared By Multi OK



Configure PI Analysis, cont.



Simulation

- The check mark next to validation check will continue to display as a warning sign until it detects zero warnings or errors. Warnings will not stop simulation progress, but errors most likely will.
- (Optional) Run the validation check again to get a green check mark next to the Validate button.
- At this point, it is possible to run the SYZ sweep to obtain S-parameters. The results obtained here can be exported in touchstone or Full Wave SPICE formats and run in a circuit simulation. This exercise, however, is geared towards optimizing capacitor selection.
- Click Simulate to extract impedance profile
- Both the PI Configuration and SIwave Workflow Wizard windows will close.

Assign SPICE Netlists	PI Configuration	_								
	AGND_VCC 4	Ref. D	es. Part Number	Positive Net	Reference Net	Port	Ref. Imp.			
Configure DC IR Drop Analysis	BST_V1P0_S0	CR3M	1 C52251-001	V3P3_S0	VCC_FLASH	None				
	BST_V1P5_S5	FB1M1	656554-032	V3P3_S0	V3P3_S0_A	None				
Configure PI Analysis	BST_V3P3_S5	J4A2	G46739-001	V3P3_S0	GND	None				
how this dialog after project import	GND	Q1L1	C81974-001	V3P3_S0	V3P3_S0	None				
now this dialog after project import	RMII_S0_PFB	Q1L2	C81974-001	V3P3_S0	V3P3_S0	None				
	V1P05_S0_IVR	U1L1	D30400-001	V3P3_S0	GND	None				
	V1P0_S0	U1L2	D30400-001	V3P3_S0	GND	None				
	V1P0_S3_IVR	U1L3	D30400-001	V3P3_S0	GND	None				
	V1P0_S5_IVR	U1L4	D30400-001	V3P3_S0	GND	None				
	V1P5_S0	U2A5	IPD031-201	V3P3_S0	GND	Port	0.1ohm			
	V1P5_S3	U2B1	G83474-001	V3P3_S0	GND	None				
	V1P5_S5	U2M1	G94441-001	V3P3_S0	GND	Port	0.1ohm			
	V1P8_S0_IVR	U3B2	C76254-001	V3P3_S0	GND	None				
	V1P8_S3_IVR	U4B1	G60296-001	V3P3_S0	GND	None				
	V3P3_S0	U10	G63512-001	V3P3_S0	GND	None				
	V3P3_50_A V3P3_53 V3P3_55 V5_ALW_ON V5_PWR_JACK VRLIS1									

Setup and Launch Simulation

• Set Frequency Sweep as follow

- Start Freq
- Stop Freq
- Number of point 100
- Distribution
- By Decade

100HZ

5GHZ

- Interpolating Sweep relative error 0.005%
- Click Launch
- Wait for simulation to complete

Compute S	6YZ-param	eters					×				
Sweep S	ensitivity Dis	stributed Analys	sis (HP	(C)							
Simul	ation name:	SYZ Sw	eep 1			•					
Compute exact DC point											
Frequency Range Setup											
	Start Freq Stop Freq Num, Points / Step Size Distribution										
1 10	00Hz	5GHz	iGHz 100								
	dd Abovo	Add Bolo		Delete Selection	Provid	200					
			vv								
	Save	Load		Set Default	Clear [Default					
Sweep Selection Set FWS generation parameters Min Rise/Fall Time / s IE-10											
● In Re	terpolating S lative error fo	weep or S: 0.005 %		SIwave with 3D DDM Other solver options							
Export Touchstone® file after simulation completes File path: G:/Training/Oticon_Training_DEC2016/December201 Browse											
			Sa	ve Settings	Launch	Close					

ANS

Extract Impedance Profile

• In results window

- Double click on SYZ Sweep 1
- Select tab Z-parameter Plot

© 2016 ANSYS, Inc.

• Check only the plot as shown beside to extract impedance profile at U2A5

Mat	rix Entries	to Plot	
	Plot	Row	Col
		V3P3_S0_G94441-001_U2M1_PIFlow	V3P3_S0_G94441-001_U2M1_PIFlow
		V3P3_S0_G94441-001_U2M1_PIFlow	V3P3_S0_IPD031-201_U2A5_PIFlow
►	\checkmark	V3P3_S0_IPD031-201_U2A5_PIFlow	V3P3_S0_IPD031-201_U2A5_PIFlow



Release 2016.0

ANSYS

PI Advisor Workflow Diagram





Launching PI Advisor

Starting PI Advisor

- Click on the Simulation menu tab.
- Click the PI Advisor button to start PI Advisor.

			SINOLAIN		
	M	a		<mark>,</mark> <u> </u>	
Options Compute AC Compute SYZ	HFSS 3D	Options Comput	te Compute	PI	PDN Channel
Currents Parameters	Layout	RLGC	3D Mesh	Advisor	Builder
Sentinel-PSI		Q3D Extracto	r (TPA)		

STALLATION

• This will put you into the first step of PI Advisor.



ANSYS[®]

PI Advisor: Step 1



Choose Ports / Active Devices to Optimize

- Click the Enforce |Z| check box next to V3P3_S0_IPD031-201_U2A5_PIFlow1.
 - This is indicated by the
 graphic next to the port name
- Do not check the box for U2M1.

VRM Setup

- Change the Location of the VRM to **U2M1**.
 - ESL and ESR can be modified to match the VRM parameters.
 - The graph will update indicating the shift in impedance.

📱 PI Advisor Wizard Step 1

Check ports where impedance profile should be enforced during optimization

Port	Enforce Z
V3P3_S0_U2A5_V3P3_S0_IPD031-201_U2A5_PIFlow	~
V3P3_S0_U2M1_V3P3_S0_G94441-001_U2M1_PIFlow	



Impedance Mask Setup

- Click the Load |Z| Profile button.
- Choose the **Z_target.zprof** file and click **OK**.
- Alternatively, it is possible to right-click and add rows.
- Click the **Next** button to proceed to Step 2.

PI Advisor: Step 2

Choosing Capacitors to Optimize

- Click on the **Optimize** column header to place a check mark next to all capacitor instances.
- Uncheck the Optimize check box next to Reference Designator C3M9.
 - This is a 0603 part that we do not want to optimize. The remainder are 0402 parts.
- Click the **Next** button to proceed to Step 3.

3_S0_IPD031-2	Part Name	Ref. Dec	Value (E)	Ontimize	
		C3M9	1E-05	Optimize	
	EMK105B1104	C12	1E-07		
	EMK105B1104	C/B7	1E-07		
	EMK105BJ104	C1M13	1E-07		
	EMK105BJ104	C1M14	1E-07		
	EMK105BJ104	C3M13	1E-07		
	EMK105BJ104	C1M11	1E-07		
	EMK105BJ104	C1M12	1E-07		
	EMK105BJ104	C1M1	1E-07		
	EMK105BJ104	C2M4	1E-07		
	EMK105BJ104	C1M9	1E-07		
	EMK105BJ104	C1M2	1E-07		
	EMK105BJ104	C1M10	1E-07		
	EMK105BJ104	C3M10	1E-07		
	EMK105BJ104	C2B1	1E-07		
	JMK105F105	C1M6	1E-06		
	JMK105F105	C1L1	1E-06	\checkmark	
	JMK105F105	C1L2	1E-06	\checkmark	
	JMK105F105	C3B5	1E-06	\checkmark	
	TMK105BJ103	C2B13	1E-08	\checkmark	
	TMK105BJ103	C4B6	1E-08	\checkmark	
	TMK105SD102	C3M8	1E-09	\checkmark	
	TMK105SD102	C3M7	1E-09	\checkmark	
	TMK105SD102	C3M6	1E-09	\checkmark	
	TMK105SD102	C3M5	1E-09	\checkmark	
	TMK105SD102	C3M1	1E-09	\checkmark	
	TMK105SD102	C3M2	1E-09	\checkmark	
	TMK105SD102	C3L30	1E-09	\checkmark	

PI Advisor: Step 3

Release 2016.0

Potential Candidate Filter

- Select only Murata as a Vendor
- Select only 0402 for the EIA Size

	Part Name	Ref. Des.	Val 1
Δ	EMK105BJ104	C4B7	1E-
	EMK105BJ104	C1M13	1E-
	EMK105BJ104	C1M14	1E-
	EMK105BJ104	C3M13	1E-
	EMK105BJ104	C1M11	1E-
	EMK105BJ104	C1M12	1E-
	EMK105BJ104	C1M1	1E-
	EMK105BJ104	C2M4	1E-
	EMK105BJ104	C1M9	1E-
	EMK105BJ104	C1M2	1E-
	EMK105BJ104	C1M10	1E-
	EMK105BJ104	C3M10	1E-
	EMK105BJ104	C2B1	1E-
	JMK105F105	C1M6	1E [,]
	JMK105F105	C1L1	1E-
	JMK 105F 105	C1L2	1E-
	JMK105F105	C3B5	1E-
	TMK105BJ103	C2B13	1E-
	TMK105BJ103	C4B6	1E-
	TMK105SD102	C3M8	1E-
	TMK105SD102	C3M7	1E-
	TMK105SD102	C3M6	1E-
	TMK105SD102	C3M5	1E
	TMK105SD102	C3M1	1E-
	TMK105SD102	C3M2	1E-
	TMK105SD102	C3L30	1E

Vendor	Show		Series	Show	EIA Siz	Show		Filte	er C	Quantity	Min	Max
AVX			GA242) V	/alue (F)	1E-13	0.0027
Johanson			GA243	\checkmark	01005		=		S	RF Range (Hz)	0	2.10375E+10
Kemet		Ξ	GA255	\checkmark	0201				S	_min Range (dB)	-106.911	-7.97224
Murata	 Image: A set of the set of the		GA342	\checkmark	0306				E	SR Range (ohms)	4.99788E-05	19.1185
Panasonic			GA343	\checkmark	▶ 0402				E	ESL Range (H)	0	6.88769E-09
Samsung			GA352	\checkmark	0508				P	rice	0	0
Sanyo			GA355	\checkmark	0603							
Syfer		-	GC321	 . 	0612		-			Load Filters	Save Filter	rs l

Select Capacitor Instances

• Select all Capacitor Instances by using **Shift+Click** or **Ctrl+Click**. The warning icon indicates that there are no candidates assigned to the capacitor instances.

Select Candidates

• Select all filtered candidate instances by using **Shift+Click** or **Ctrl+Click** in the row indicator.

Vendor	Series	Part Name	Plot	Candidate	Value (F)	EIA Size	Price	L_mnt (H)	R_mnt (ohms)	SRF (Hz)	*
Murata	GRM15	GRM15XR71H681KA86		Add	6.8E-10	0402	0	1E-10	0.001	3.71472E+08	
Murata	LLL15	LLL153C70E105ME21		Add	1E-06	0402	0	1E-10	0.001	1.49852E+07	
Murata	LLL15	LLL153C70G474ME17		Add	4.7E-07	0402	0	1E-10	0.001	2.181E+07	
Murata	LLL15	LLL153C80G105ME21		Add	1E-06	0402	0	1E-10	0.001	1.54109E+07	
Murata	LLL15	LLL153C80J104ME01		Add	1E-07	0402	0	1E-10	0.001	6.45005E+07	
Murata	LLL15	LLL153C80J224ME14		Add	2.2E-07	0402	0	1E-10	0.001	4.34103E+07	
Murata	LLL15	LLL153R61A104ME01		Add	1E-07	0402	0	1E-10	0.001	6.45005E+07	-
•										+	

Assign Selected Candidate(s)

• Click the **Assign Selected Candidates** button with both Capacitor Instances and Selected Candidates to populated the Assigned Candidate Models.

Plot Assigned Candidate Models

• Select all of the Assigned Candidate Models by using Shift+Click or Ctrl+Click.

April 5, 2017

- Click the **Plot |Z11|** button to display the candidate model profiles. Your display should now appear similar to the graphic below.
- Click Next to proceed to Step 4.

PI Advisor: Step 4

Genetic Algorithm Settings

- The default settings for the genetic algorithm attempts to the number of capacitors as the goal. The sum total of A Weights should add up to 1.
- Members per generation: Number of trial designs per ite

PI Advisor Wizard S

▲ Simulation Name

- Number of generations: Total number of iterations.
- Number of schemes to report: Subset of members to report

SYZ Sweep Settings

- Click the Edit button.
- Set the following Sweep Definition:
 - Start Frequency: 100Hz
 - Stop Frequency: 5GHz
 - Num. Points / Step Size: 100
 - Distribution: By Decade
- Set the Sweep Selection to:
 - Interpolating Sweep
 - Relative error for S: 0.005
- Click Other solver options...

		PI Advisor Solution Frequency Range	x
tempts to roduce		0	
liempis to reduce		Sweep	
total of Attribute		Compute exact DC point	
		· · ·	
		Frequency Range Setup	\neg
ns per iteration.		Start Freq Stop Freq Num. Points / Step Size Distribution	- I
		1 100Hz 5GHz 100 By Decade	
OUS.		by becaue	
oro to 100			
ers to report.			
		Add Above Add Below Delete Selection Preview	
Advisor Wizard Step 4		Swaan Salastian	
		Sweep Selection Restore Default Sweep	
Simulation		Discrete Sweep	
Name	PI Opt Sim 1	Min Rise/Fall Time / s	ī l
S-parameter Source	[Recompute]	1E-10	-
S-parameter Solver	Slwave	Interpolating Sweep	
Authority Author		Relative error for S: 0.005	
Total price Tatal symplect of access 3		SIwave with 3D DDM	
Total number of capacitors Total number of capacitors		Other solver an income	
Total number of capacitor types Total capacitor accor		Outer solver options	
Attribute Weighte			
Price weight	0		
Number of capacitors weight	1		
Number of capacitor types weight	0		
Capacitor area weight	0		
Optimizer Control Parameters	-		
Members per generation	100		
Number of generations	40		
Number of schemes to report	10		
Thresholds			
Maximum total price (\$)	5.00		
Maximum number of capacitors	100		
Maximum number of capacitor types	20	ОК С	lose
Maximum total capacitor area (mm^2)	757.418		
S-parameter Simulation Options			
Impedance Mask Range	100Hz -> 1E+09H	Z. C.	
Sweep Range	5000Hz -> 5E+09	Iz, 601 points	
S-parameter Sweep Configuration		Edit	
Previo	us Launch Optin	izer 🔁 Cancel 🔏	

Slwave Options

- SI/PI tab
 - Choose Balanced
 - The slider bar allows you to choose between three predefined settings.
 To see what settings are changed, move the slider bar to different positions and click on the SI/PI Advanced tab.

SIwave O	ptions						×
SI/PI	SI/PI Advanced	DC DC /	Advanced	Multiprocessing	Net Processing		
© SI	simulation						
	0-14-0-1-1		Deleses		0-1-1-		
	Optimum speed		balance	a	Optimum accuracy		
● PI	simulation						
	Optimum speed		Balance	d	Optimum accuracy		
Cu	istom (selecting this	s option allows	you to co	nfigure advanced	solver settings)		
						OK	Cancel

- SI/PI Advanced tab
 - Note that we are only solving for cavity fields for this balanced PI simulation and Automatic Mesh Refinement is turned on.

Multiprocessing (High Performance Computing, HPC)

- For a PI simulation, HPC can distribute the solver across multiple cores.
- Click on the **Multiprocessing** tab.
- Ensure the following options are set:
 - Number of cores to use: Max (increase until it stops incrementing)
 - Use HPC Licensing: Enable
 - HPC Pack: Selected
 - Max: 80% of total RAM
- Click **OK** to close this window.

SIwave C	ptions							x
SI/PI	SI/PI Advanced	DC	DC Advanced	Multiprocessing	Net Processing			
_ Mu	ltiprocessing							
N	umber of cores to u	use:	4					
	Use HPC licensing	. ©	HPC Pool					
		۲) HPC Pack					
	Max.	80	% of total					
Simula	ation server name:	localh	ost	Port: 3100	D			
						ſ	ОК	Cancel

- Genetic Algorithm and SYZ Sweep Settings, cont.
 - Click **OK** to apply the S-parameter sweep settings.
 - Click Launch Optimizer to begin the PI Advisor simulation.

Advisor Solution Frequency Range	PI Advisor Wizard Step 4
weep	4 Simulation
	Name PLOnt Sim 2
Compute exact DC point	S-parameter Source [Recompute]
Frequency Range Setup	S-parameter Solver Sliwave
	A Attributes to Minimize
Start Freq Stop Freq Num. Points / Step Size Distribution	✓ Total price
1 100Hz 5GHz 100 By Decade	✓ Total number of capacitors
	Total number of capacitor types
	✓ Total capacitor area
	▲ Attribute Weights
Add Above Add Below Delete Selection Preview	Price weight 0
	Number of capacitors weight 1
Sweep Selection	Number of capacitor types weight 0
Restore Default Sweep	Capacitor area weight 0
Min Rise/Fall Time / s	▲ Optimizer Control Parameters
1E-10	Members per generation 100
Interpolating Sweep	Number of generations 40
Relative error for S: 0.005 SIwave with 3D DDM	Number of schemes to report 10
	▲ Thresholds
Other solver options	Maximum total price (\$) 5.00
	Maximum number of capacitors 100
	Maximum number of capacitor types 20
	Maximum total capacitor area (mm ²) 757.418
	S-parameter Simulation Options
	Impedance Mask Range 100Hz -> 1E+09Hz
	Sweep Range 100Hz -> 5E+09Hz, 771 points
I	S-parameter Sweep Configuration Edit
OK Close	Cancel 🔉

SYZ Sweep and PI Advisor Simulation Status

Process Monitor and Information / Errors / Warnings

- The process monitor shows the simulation status and steps taken by the solver.
- Information / Errors / Warnings alerts you to any potential issues that may arise during the solution process.

PI Advisor Results

29

PI Advisor Results

Viewing Results

- The results window displays ten capacitor selections that come the closest to the specified criteria and the corresponding [Z11].
- Each Scheme is able to be applied back to the project or exported as a Bill of Materials (BOM) change.
- Select Scheme 9 from the Schemes window.
- Click the **Show impedance mask** check box.
- If multiple Active Devices were specified, the Port field would enable selection of those ports.

ANSYS

PI Advisor Results, cont.

Viewing Results

- Selecting multiple lines accumulates |Z11| for all available schemes.
- Click **Close** to close the PI Advisor Results window.

PI Advisor Results

Plotting and Exporting Loop Inductance

- From the Results workspace, Right-click PI Opt Sim 1 > View Loop Inductance for Port > V3P3_S0_OPD031-201_U2A5_PIFlow
- This plot shows the loop inductance to each capacitor as seen from the selected active device. The inverse relationship of this loop inductance shows that lower values can contribute to higher frequency resonances. This inductance value is the geometry portion of the loop inductance not inclusive of ESL from a placed capacitor (*L*_{geometry}).
- A text file of these loop inductances can be exported from the results option Export Loop Inductance Table.

