The diagram in slide 2 describes the simplified architecture for a FPGA graphic accelerator card connected to a server motherboard by a standard PCIe* edge connector (slot).

System components for the PCIe channel (marked in orange color):
- IC1000 → FPGA with PCIe I/O
- X1000 → board edge connector
- X2000 → socket connector for PCIe
- IC2000 → PCIe multiplexer IC
- IC3000 → PCIe switch IC
- IC4000 → CPU with PCIe I/O

Requirements:
1) Define full channel PCIe routing recommendations for the FPGA graphic accelerator card and server motherboard based on pre-layout transient simulation
2) Route the PCIe interface for the FPGA graphic accelerator card and server motherboard PCBs in a dedicated CAD environment
3) Verify channel compliance to PCIe standard by using s-parameter extraction (post-layout)
4) Verify impact of random jitter on differential signaling timing parameters

*PCIe (Peripheral Component Interconnect Express), officially abbreviated as PCIe or PCI-e is a high-speed serial computer expansion bus standard.
TIEplus 2018 Subject

IC1000
- FPGA with PCIe IOs
  - 8 GByte DDR3 x72 @1066 MT/s

IC4000
- PCIe Switch
- 2:1 Mux/Demux
- PCI Express x4 slot

IC2000
- PCI Express x4 slot

CPU 1
- 2x DDR4 DIMM
- PCH
- Network MAC/PHY
- Disk 0, Disk 1, Disk 2, Disk 3
- SAS/SATA Controller

CPU 2
- 2x DDR4 DIMM

Power Supplies
- Configurator
- Clocks

USB

PCI Edge Connector

Continental
CETTI
ANSYS
CST