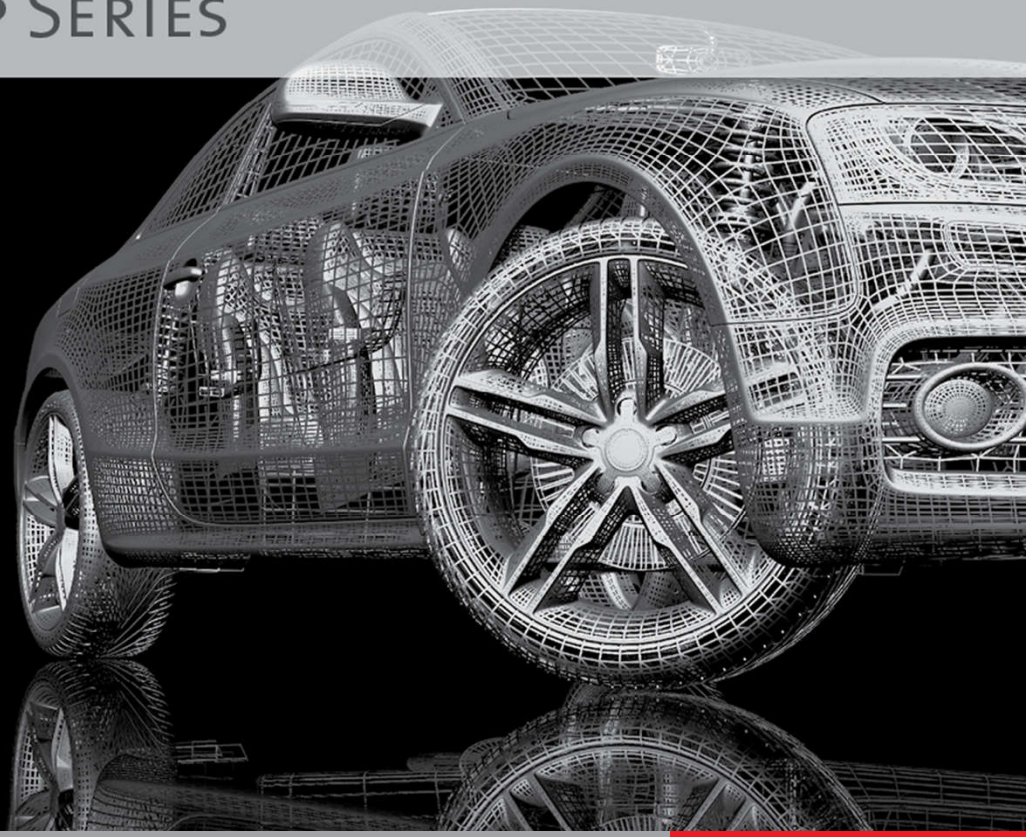
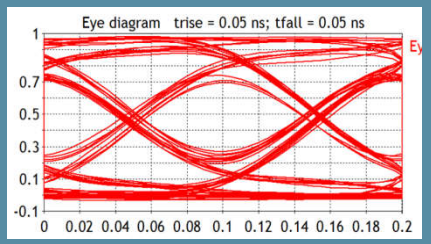
CST STUDIO SUITE®

AUTOMOTIVE WORKSHOP SERIES

Automotive PCB SI and PI analysis

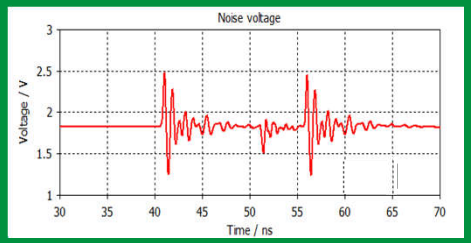


SI – PI Analysis



Signal Integrity

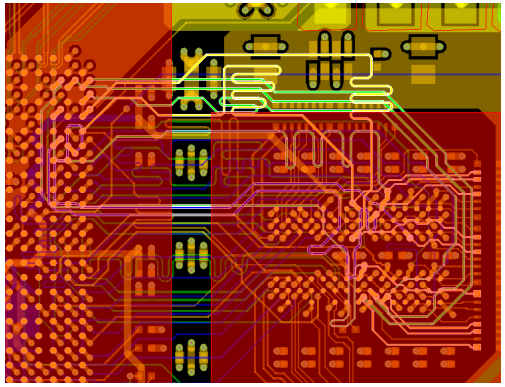
- S-Parameter
- Timing analysis
- Eye diagram



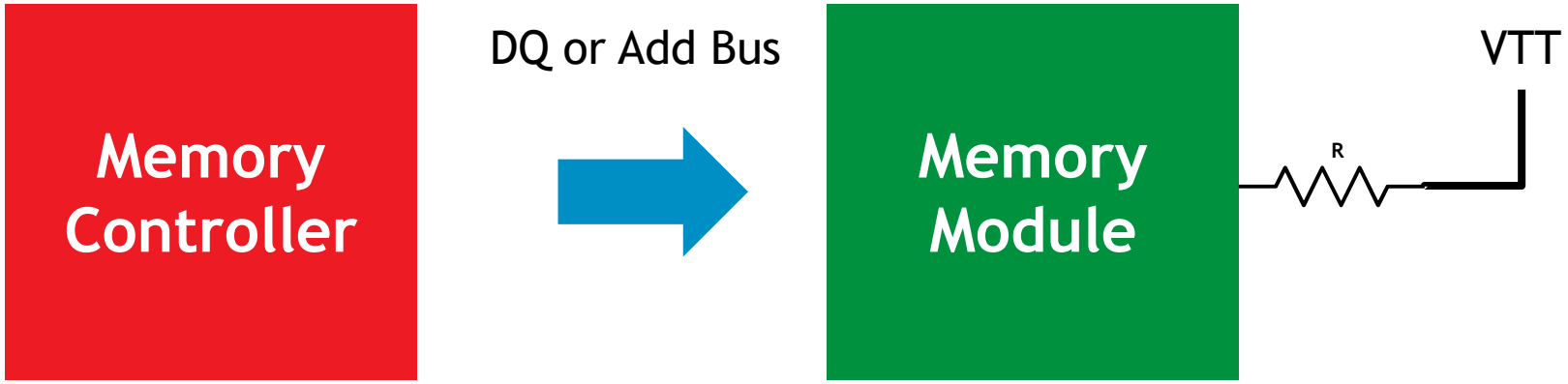
Power Integrity

- Loop / Partial inductance
- DC IR-Drop
- AC PDN Impedance
- Power Aware SI

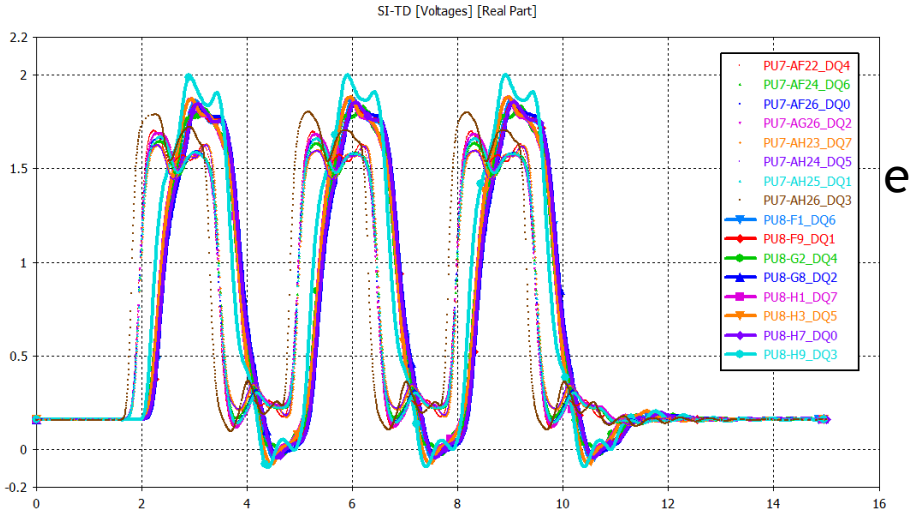
Signal Integrity



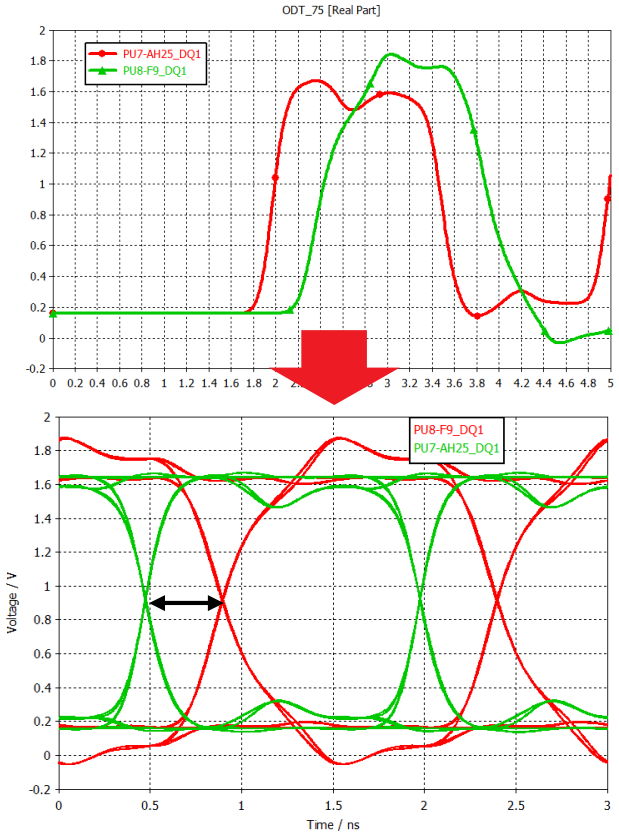
- 8 bits DDR2 lines
- IBIS model for the driver (controller) and the receiver (DRAM)
- Using 2DTL Method



SI-TD Analysis – Timing Analysis



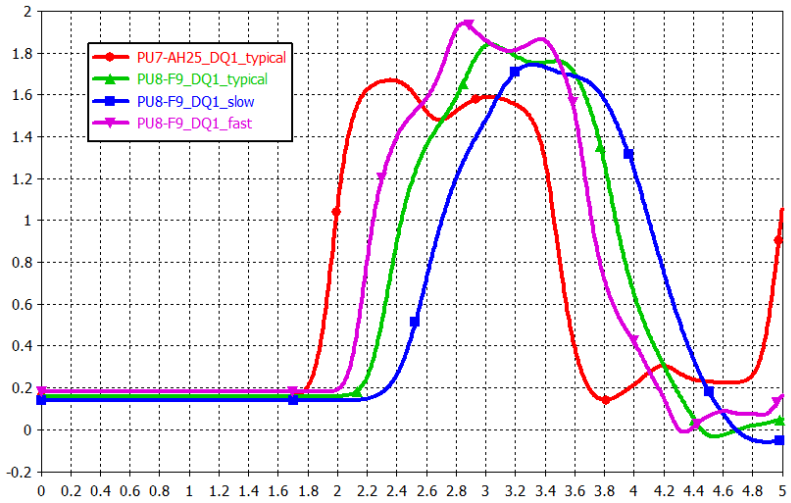
e.g. DQ1



Receiver results for “typical” IBIS Model

400ps delay driver → receiver

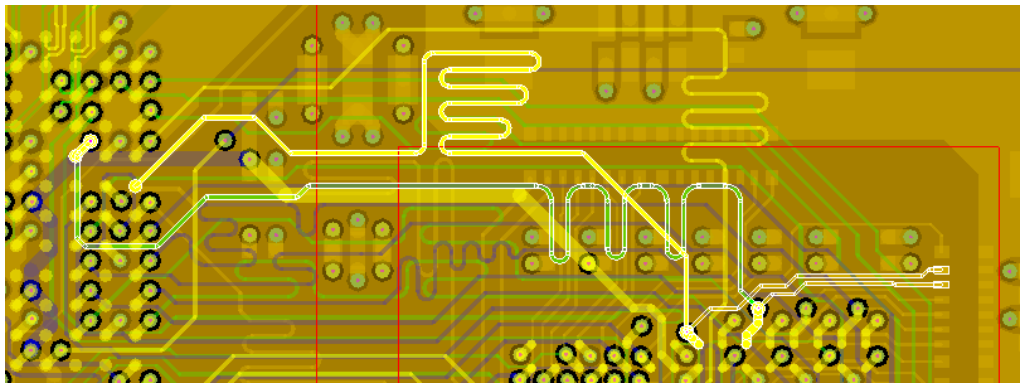
Timing Analysis for Different IBIS Model

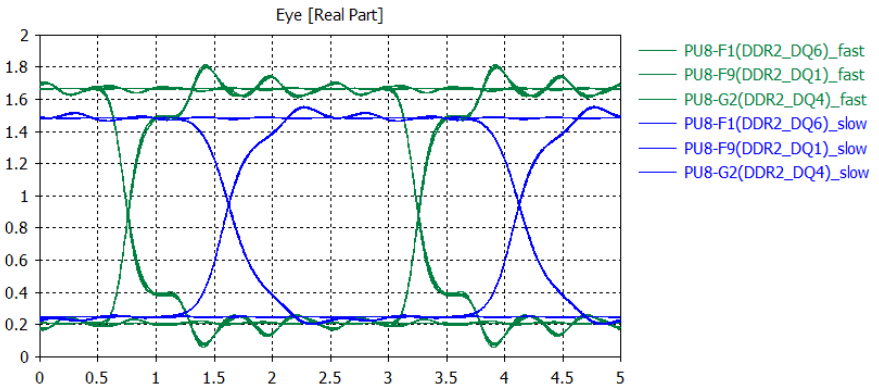


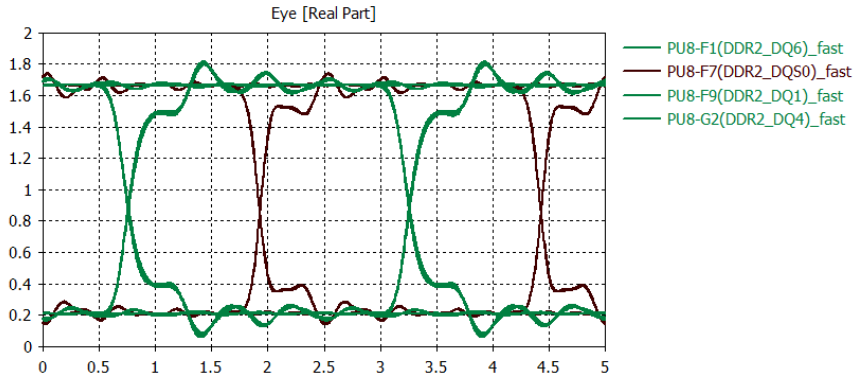
- Buffers characteristic are process, voltage, and temp dependent.
- “fast”: high voltage and
- low temp
- “slow”: low voltage and
- high temp

Recommended to simulate both “slow” and “fast” (envelope)

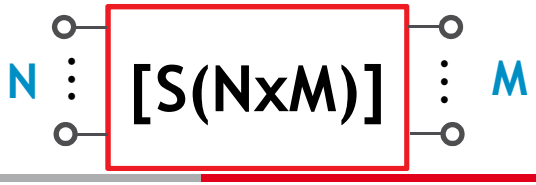
Timing Analysis - Eye diagram

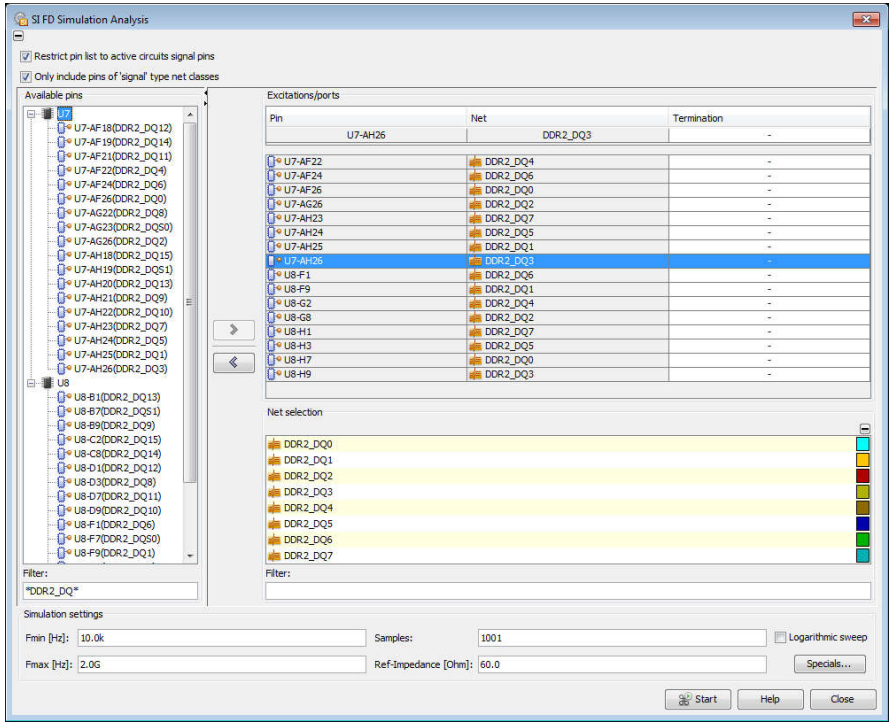


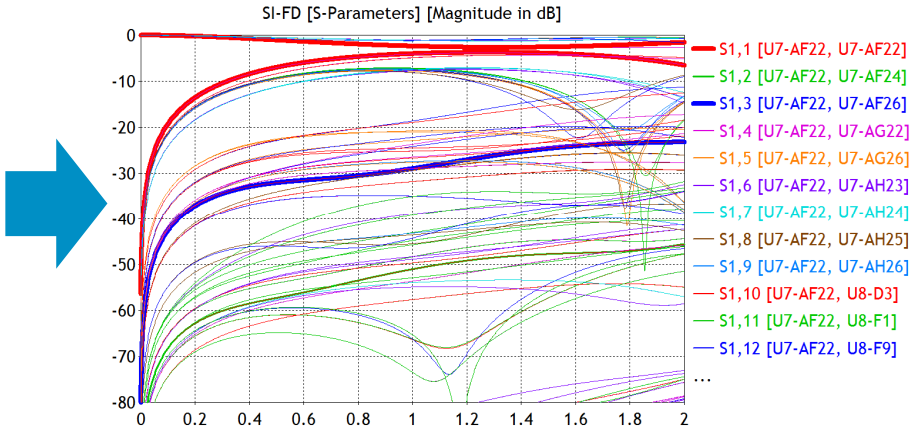




SI-FD



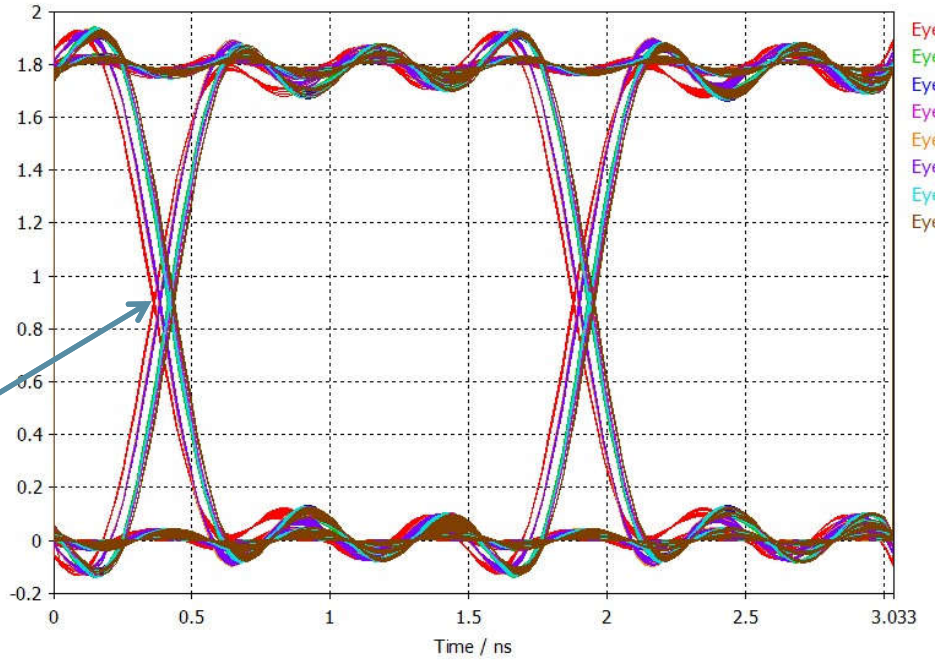




Deliver the transfer function spectrum (s-parameter) of the DQ lines

Post Processing

Quick eye diagram generation with high bit rates, z.B. PRBS with N=7

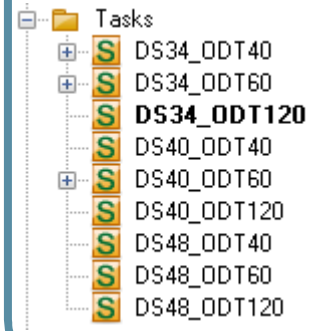


70ps skew between the data lines

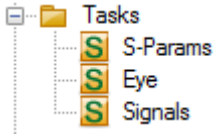
Create Simulation Projects

Net Selection

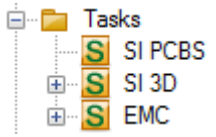
Termination



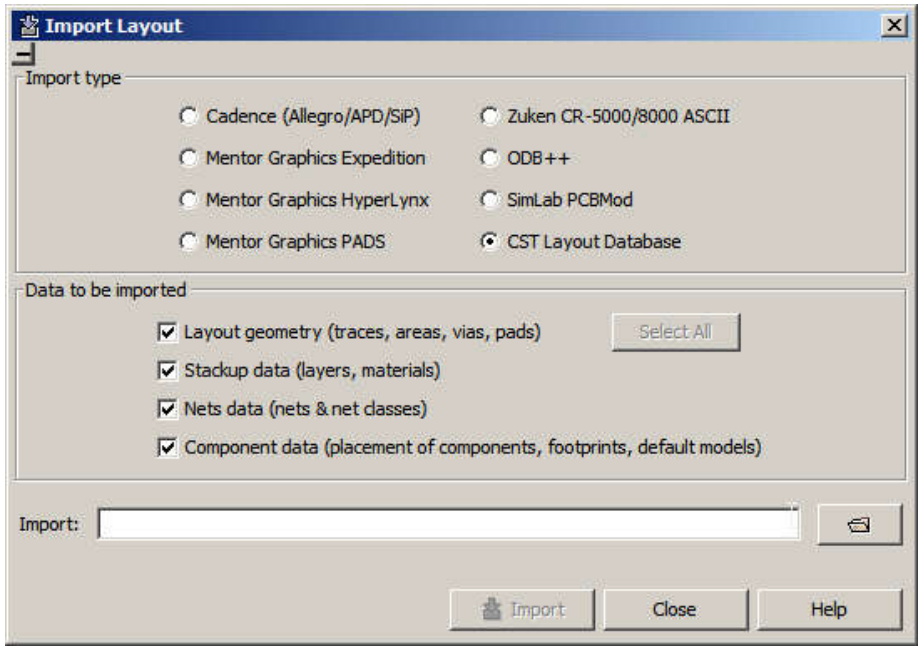
Results

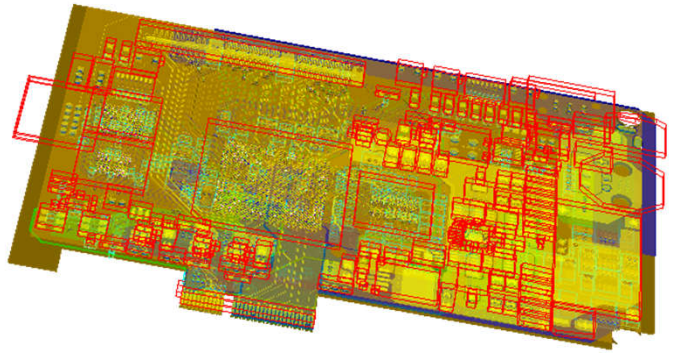


2D / 3D

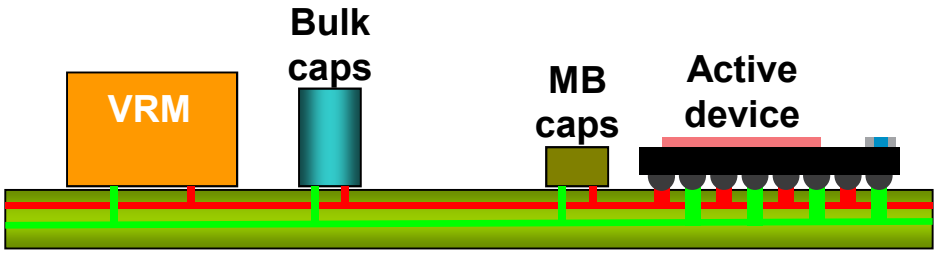


Exchange Layout



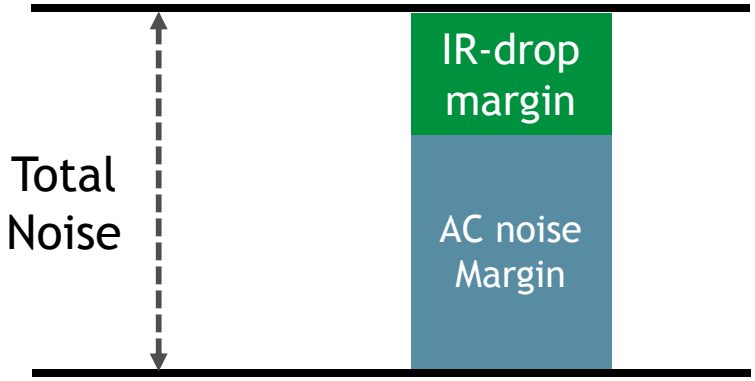


Power Integrity



VRM → PDN → Die

- DC analysis: IR-drop
- PDN Impedance
- Time domain simulation

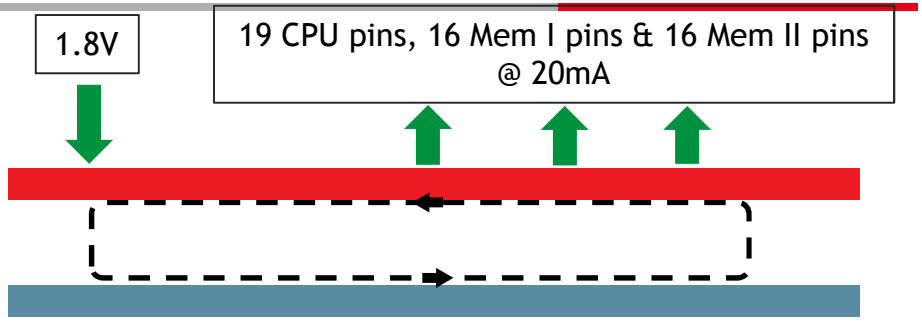


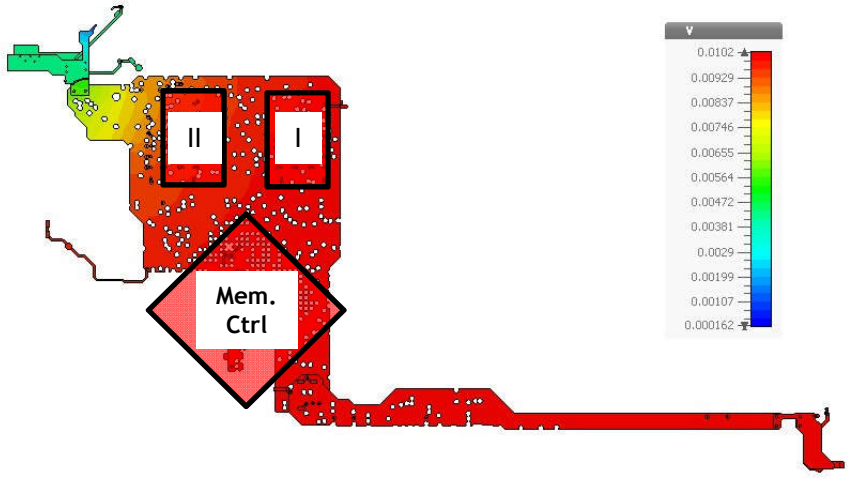
IR-Drop Simulation

Component	Voltage (V)	VDD Drop (V)	GND Drop (V)	DC Resistance
Memory controller Group	1.78849	10.507m	1.007m	575mOhm
Memory Module I Group	1.7889	10m	0.969m	498mOhm
Memory Module II Group	1.789	9.409m	0.929m	469mOhm

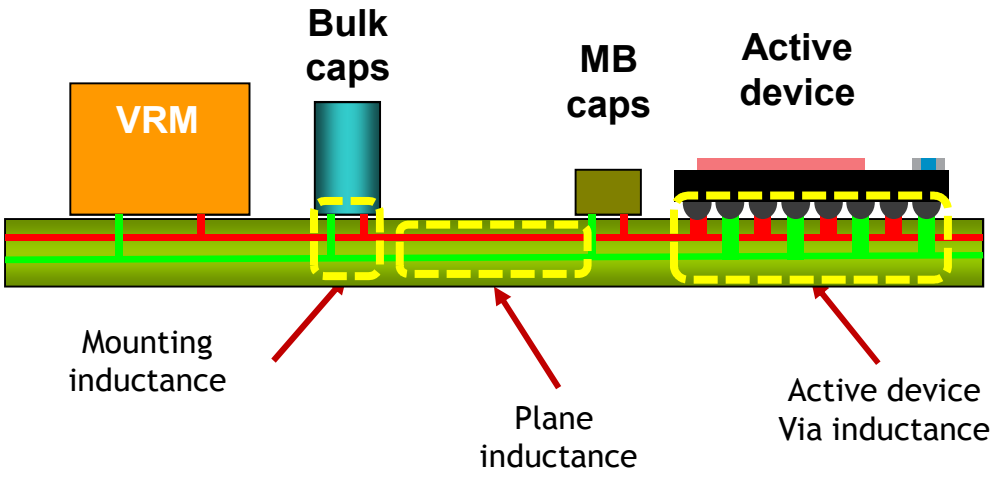
Symbol	Parameter	Rating		
		Min.	Typ.	Max.
VDD	Supply Voltage	1.7	1.8	1.9
VDDL	Supply Voltage for DLL	1.7	1.8	1.9
VDDQ	Supply Voltage for Output	1.7	1.8	1.9
VREF	Input Reference Voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ
VTT	Termination Voltage	VREF - 0.04	VREF	VREF + 0.04

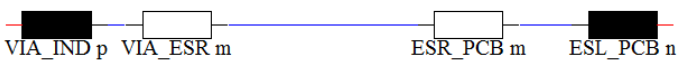
JEDEC 79-2F

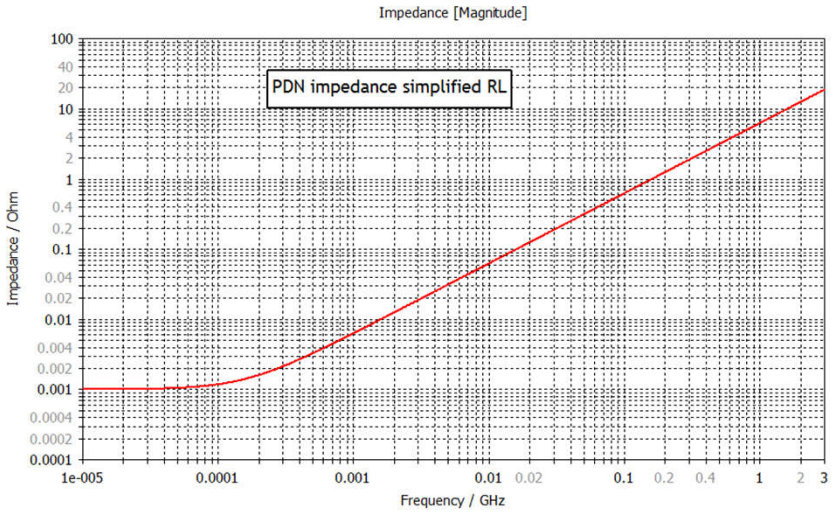




Power Delivery Network (PDN) Impedance







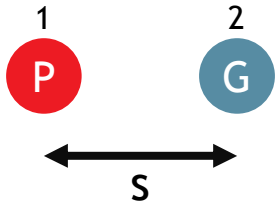
PCB inductance and via inductance contribute at higher frequency

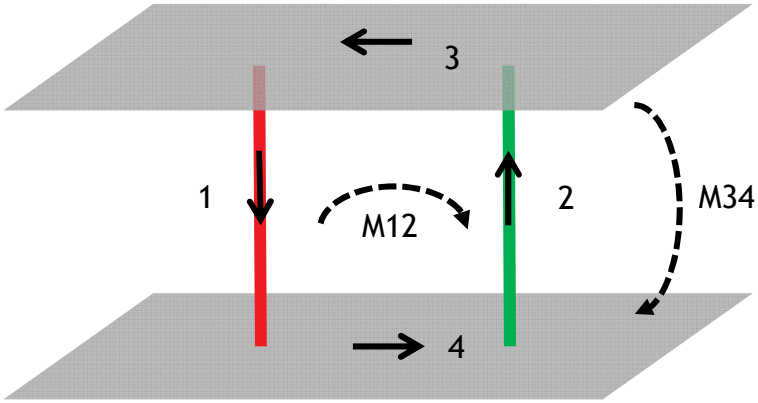
➔ Increasing the impedance between source and load

Vias Characterization

$$L_{loop} = L_{11} + L_{22} + L_{33} + L_{44} - 2M_{12} - 2M_{34}$$

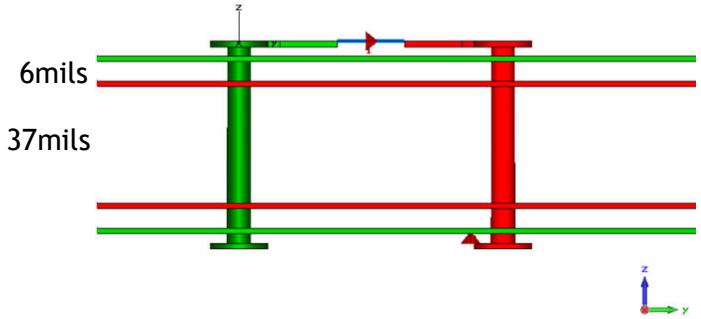
Via Loop Inductance

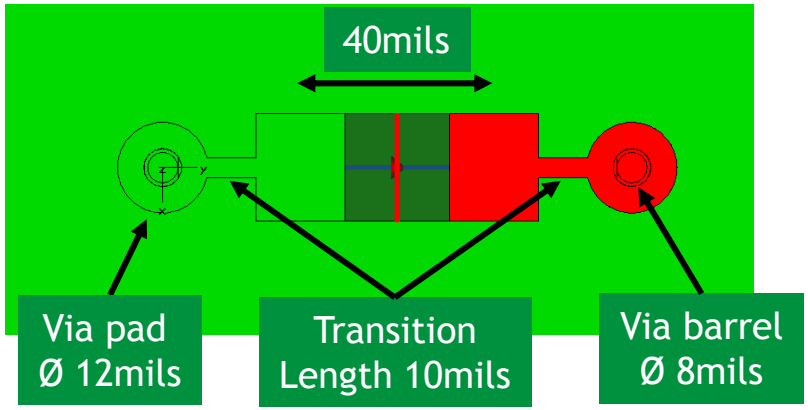




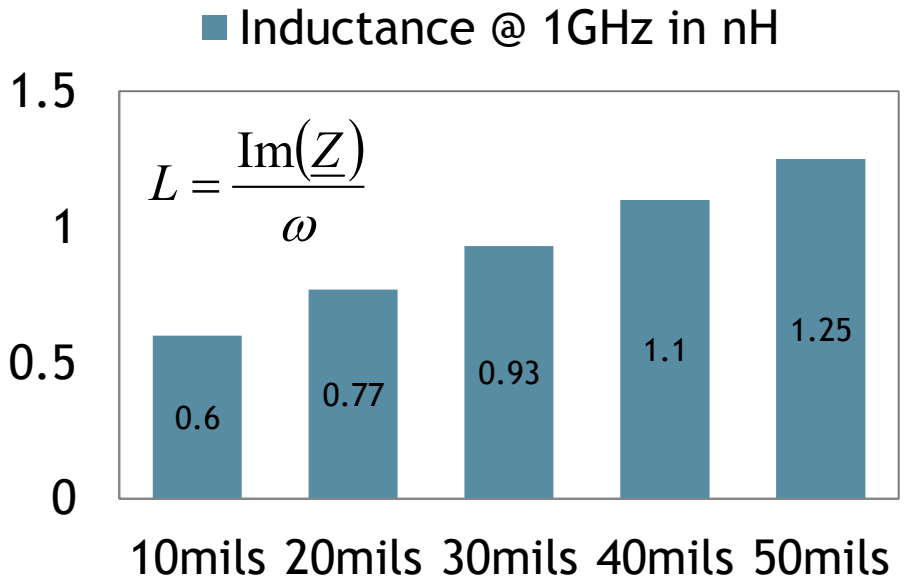
Partial Inductance of Via $L = 5.08h\left[\ln\left(\left(\frac{2h}{d}\right) - 1\right)\right]$ [pH] and mils

Simulation Setup

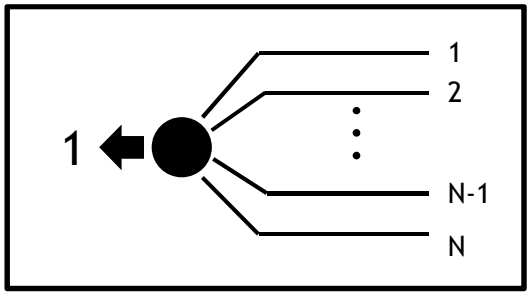


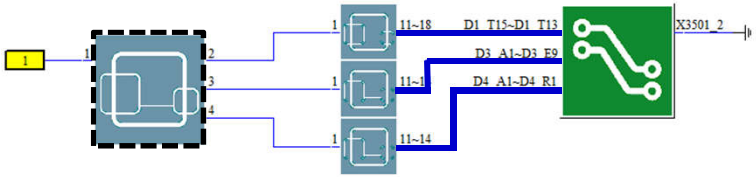


Inductance is influenced by the loop area

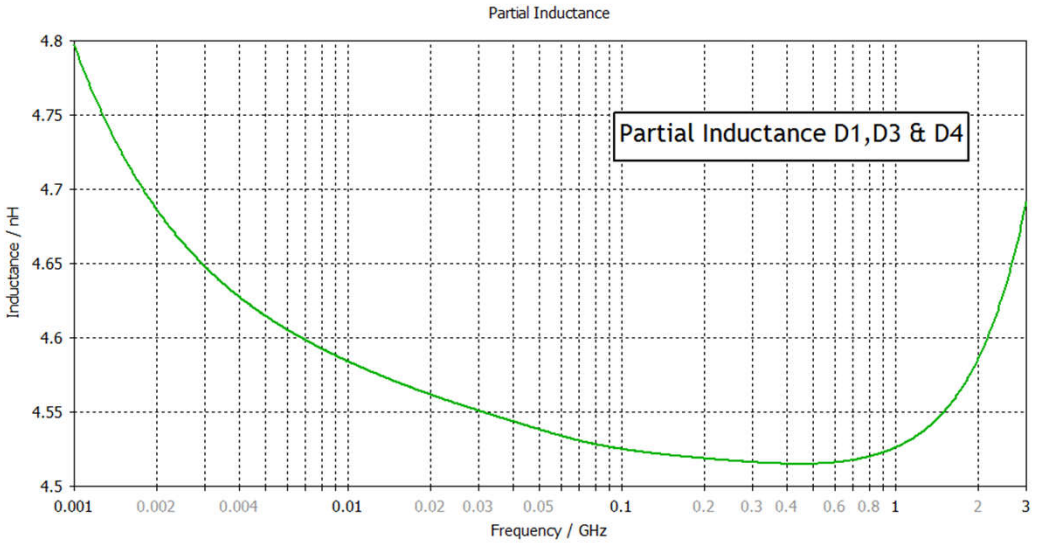


Plane Partial Inductance



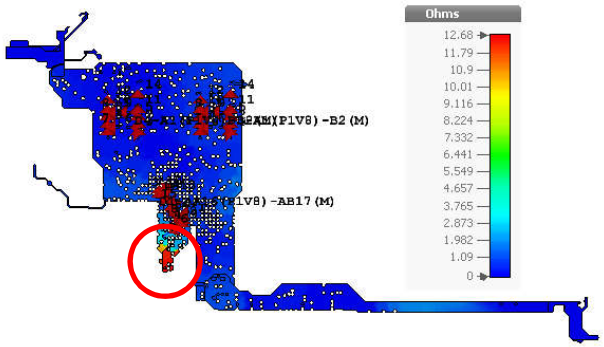


All the power pins are group together

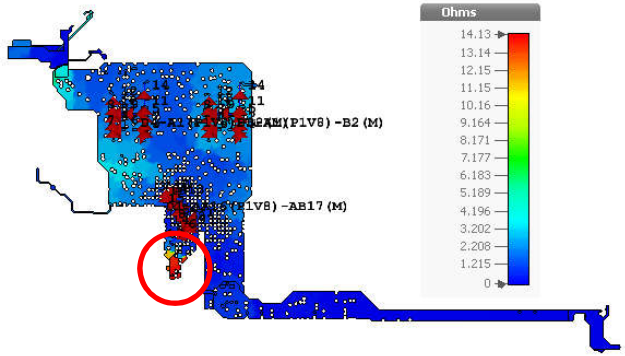


PEEC Method

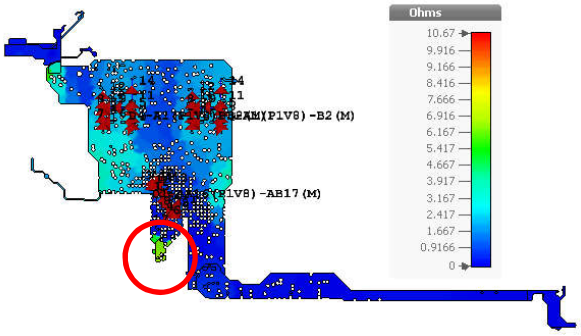
Spatial PDN Impedance Plot



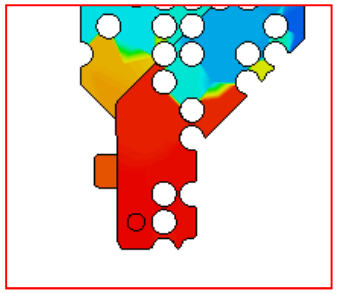
Impedance plot on P1V8 plane seen from memory controller

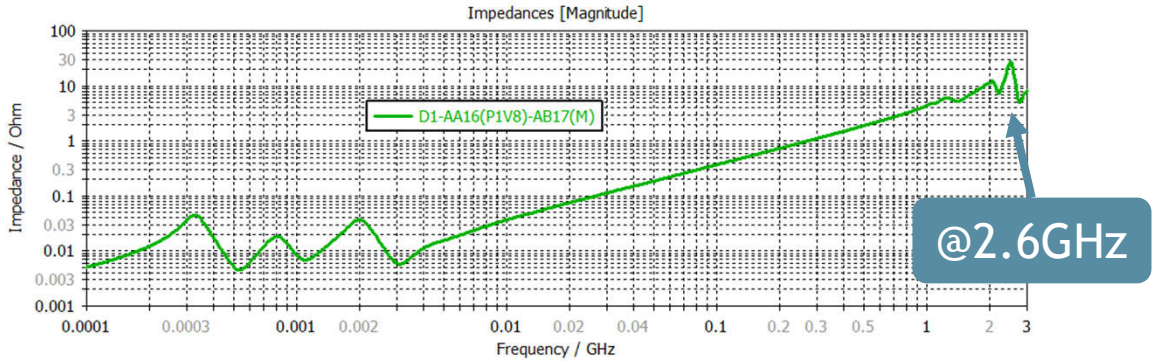


Impedance plot on P1V8 plane seen from memory module I

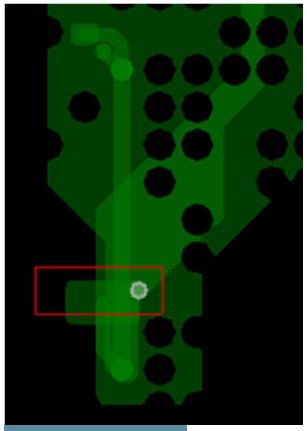


Impedance plot on P1V8 plane seen from memory module II

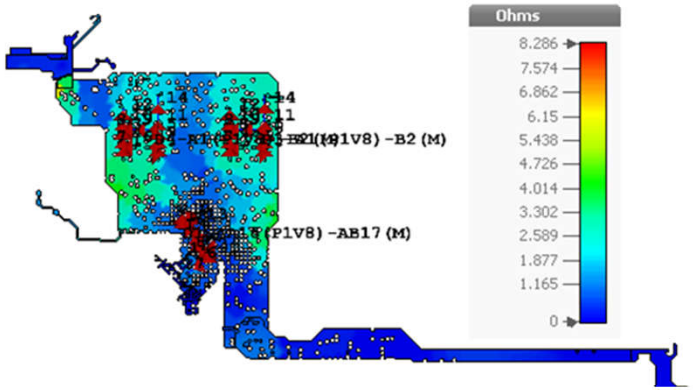


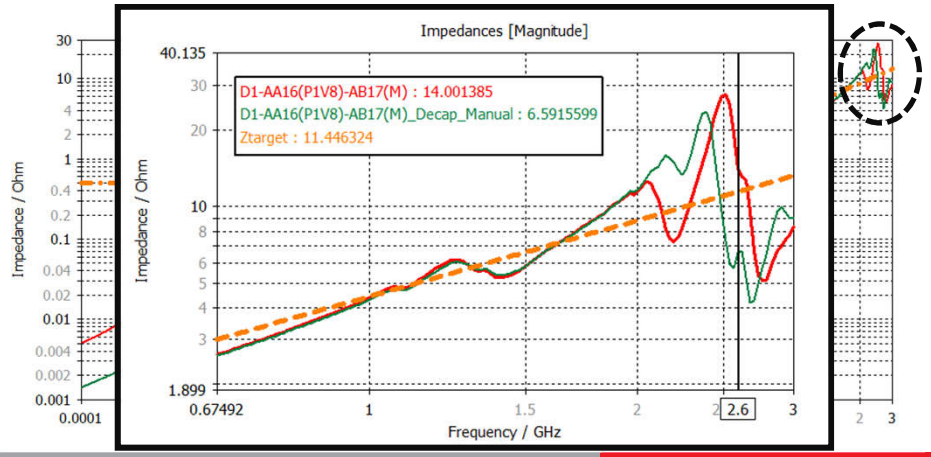


Decap Placement



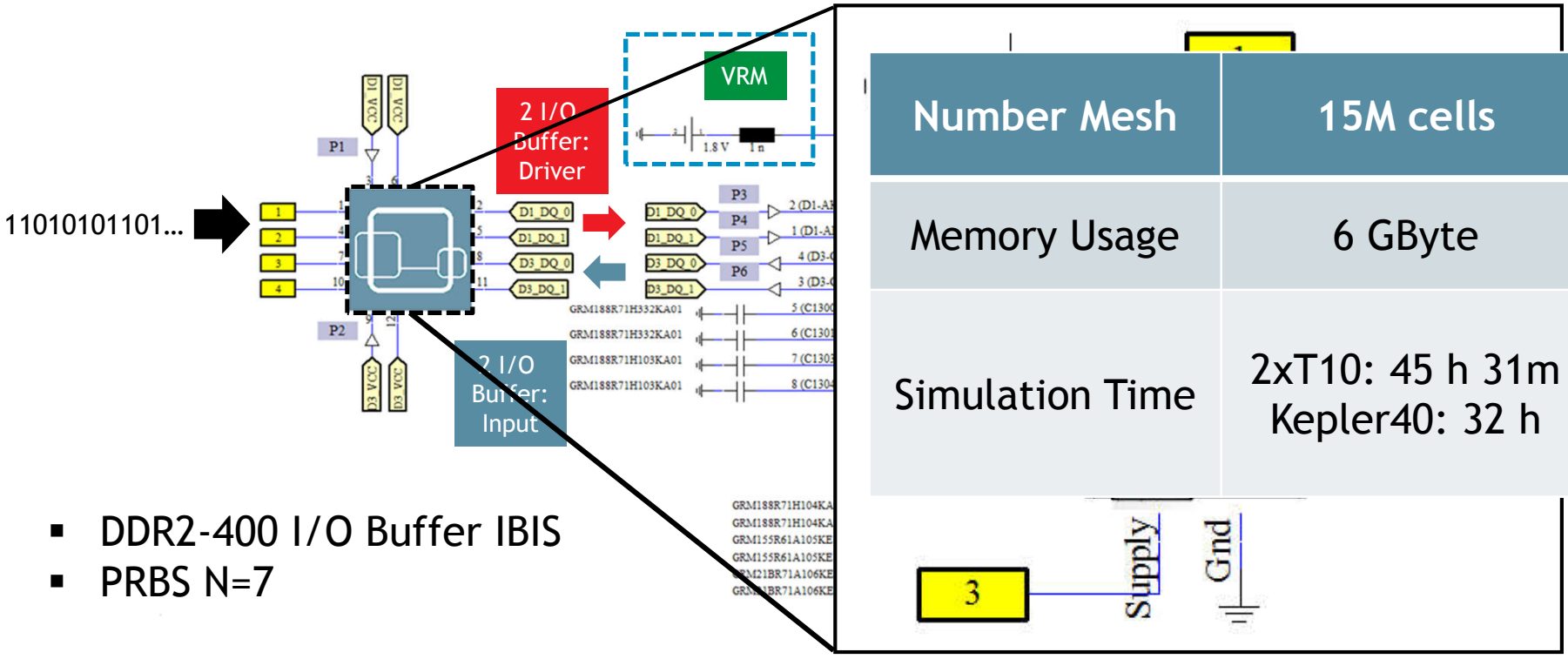
220pF





Decaps shifts the high impedance at its placement area

SSO Analysis for 2 DQ lines

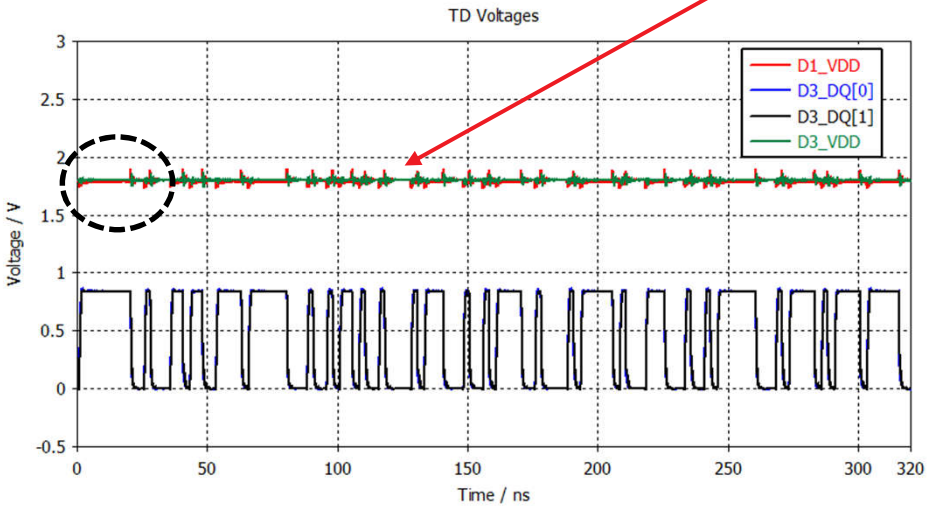


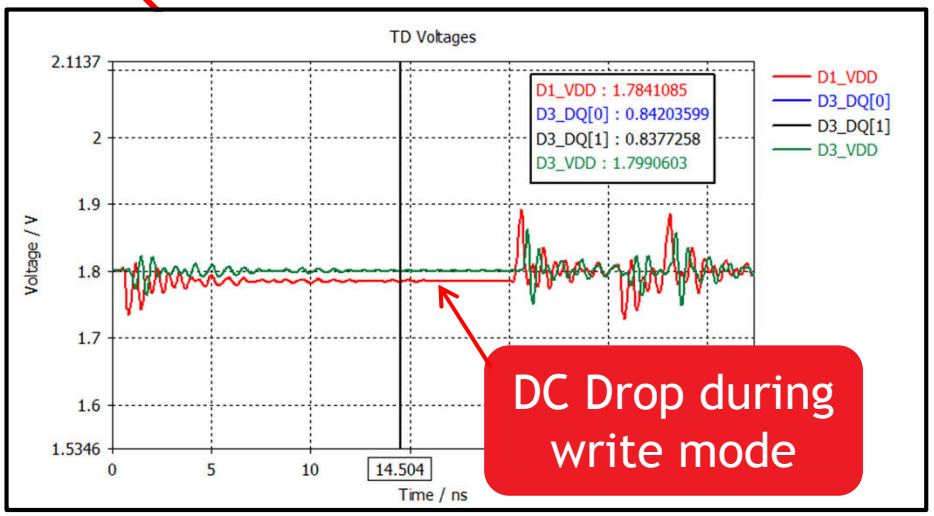
Number Mesh	15M cells
Memory Usage	6 GByte
Simulation Time	2xT10: 45 h 31m Kepler40: 32 h

- DDR2-400 I/O Buffer IBIS
- PRBS N=7

Transient Response

Power Supply VDD





DC Drop during write mode

With Decaps

No Decaps

Decap Analysis Tool

Over designing the PCB ➔ Additional BOM cost

→ slightly or without performance improvement

Multiple goals:

- Optimizing the BOM cost
- Optimizing the PDN impedance

Define the target impedance

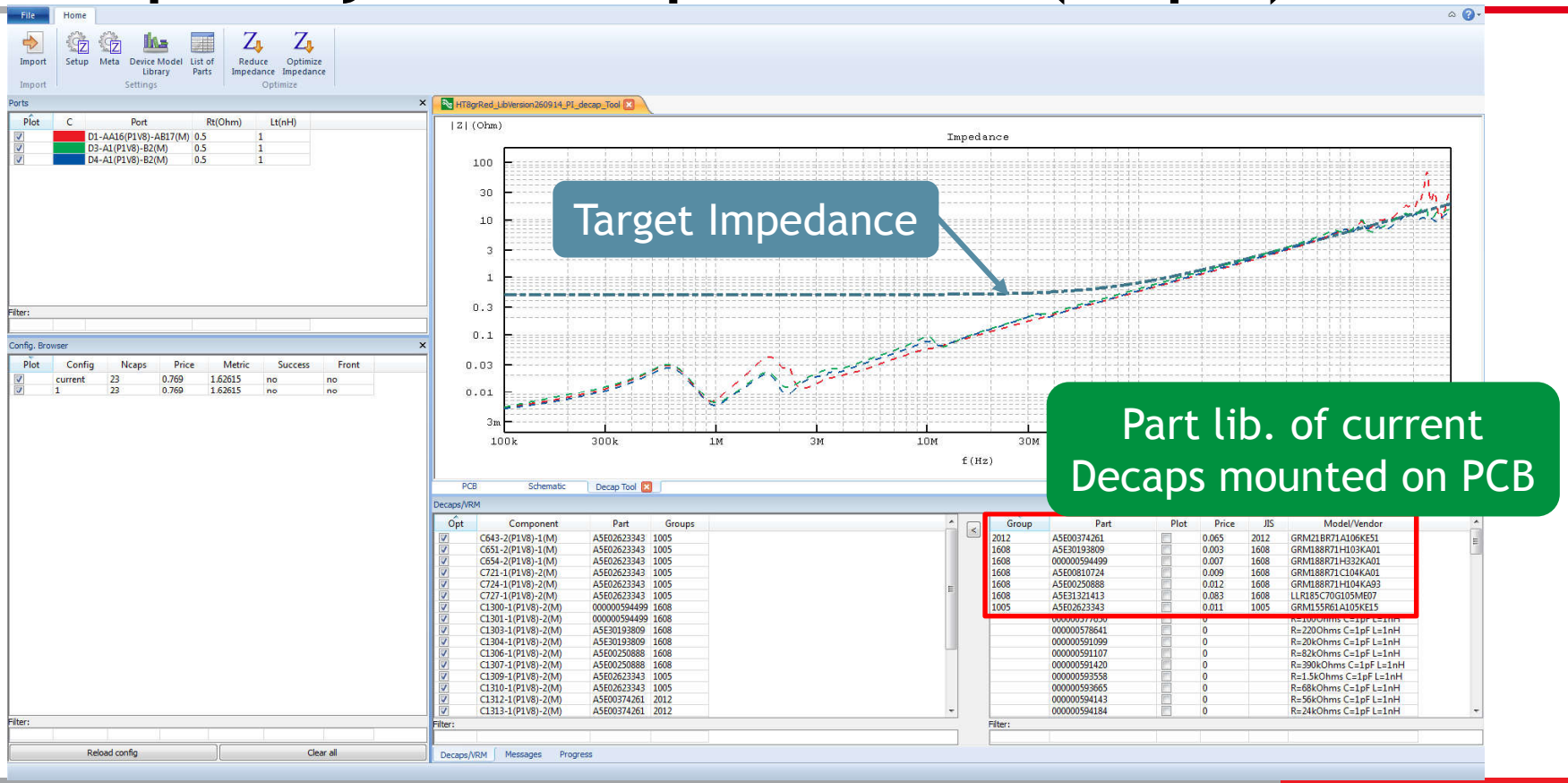
⬇

Define the list of parts for optimization

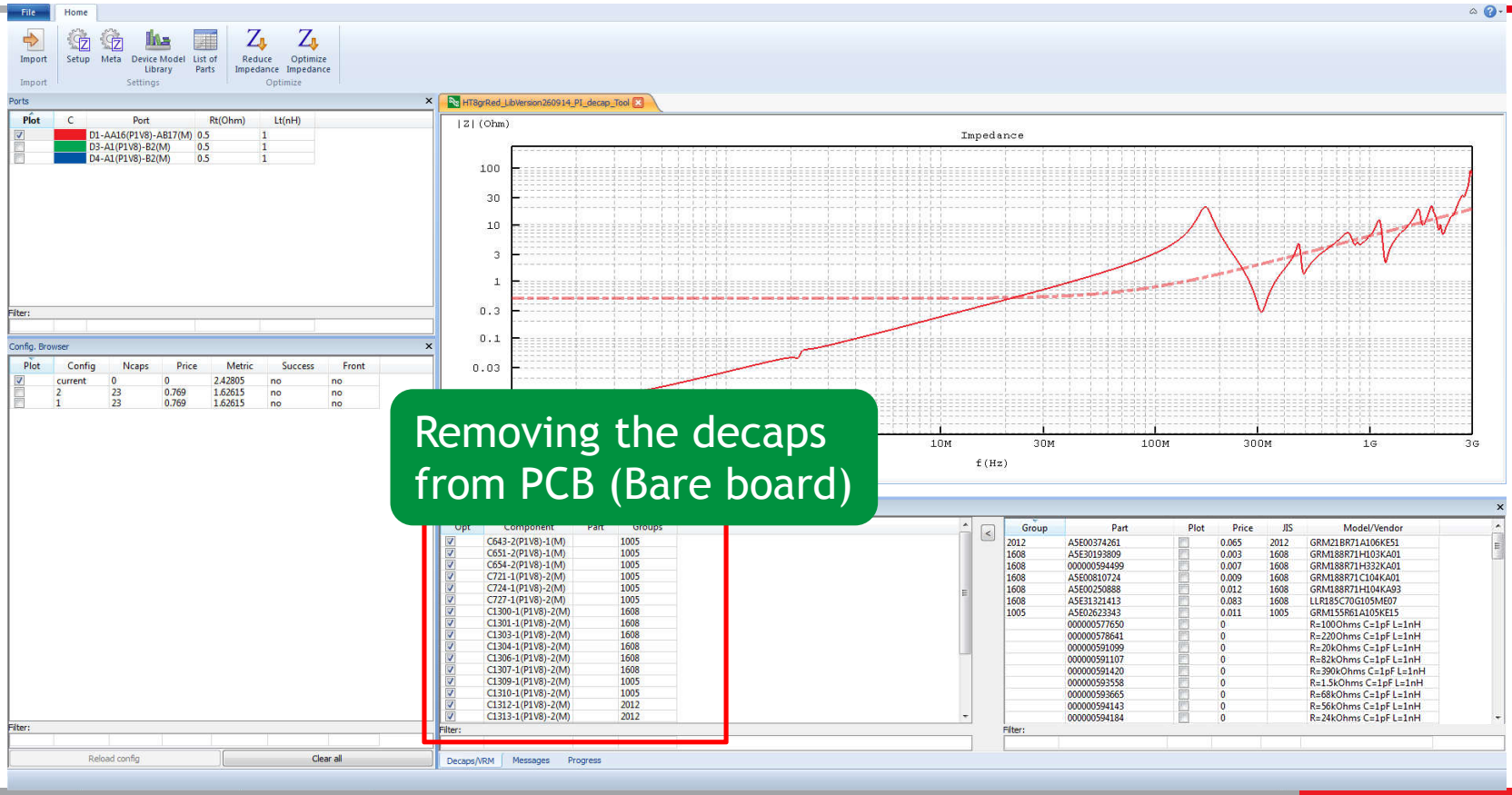
⬇

Start the optimization

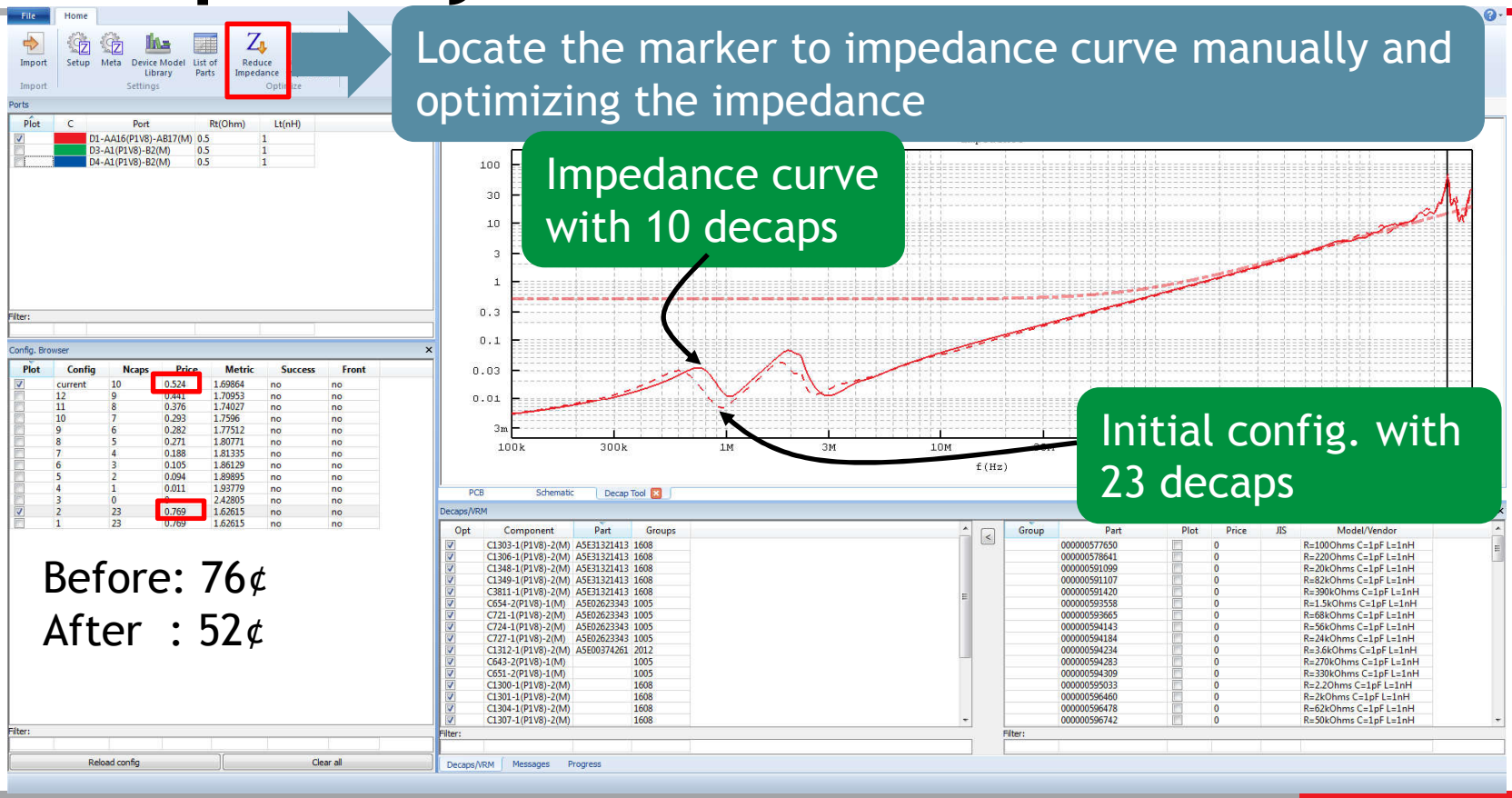
Decap Analysis Tool Optimization (Step 1)



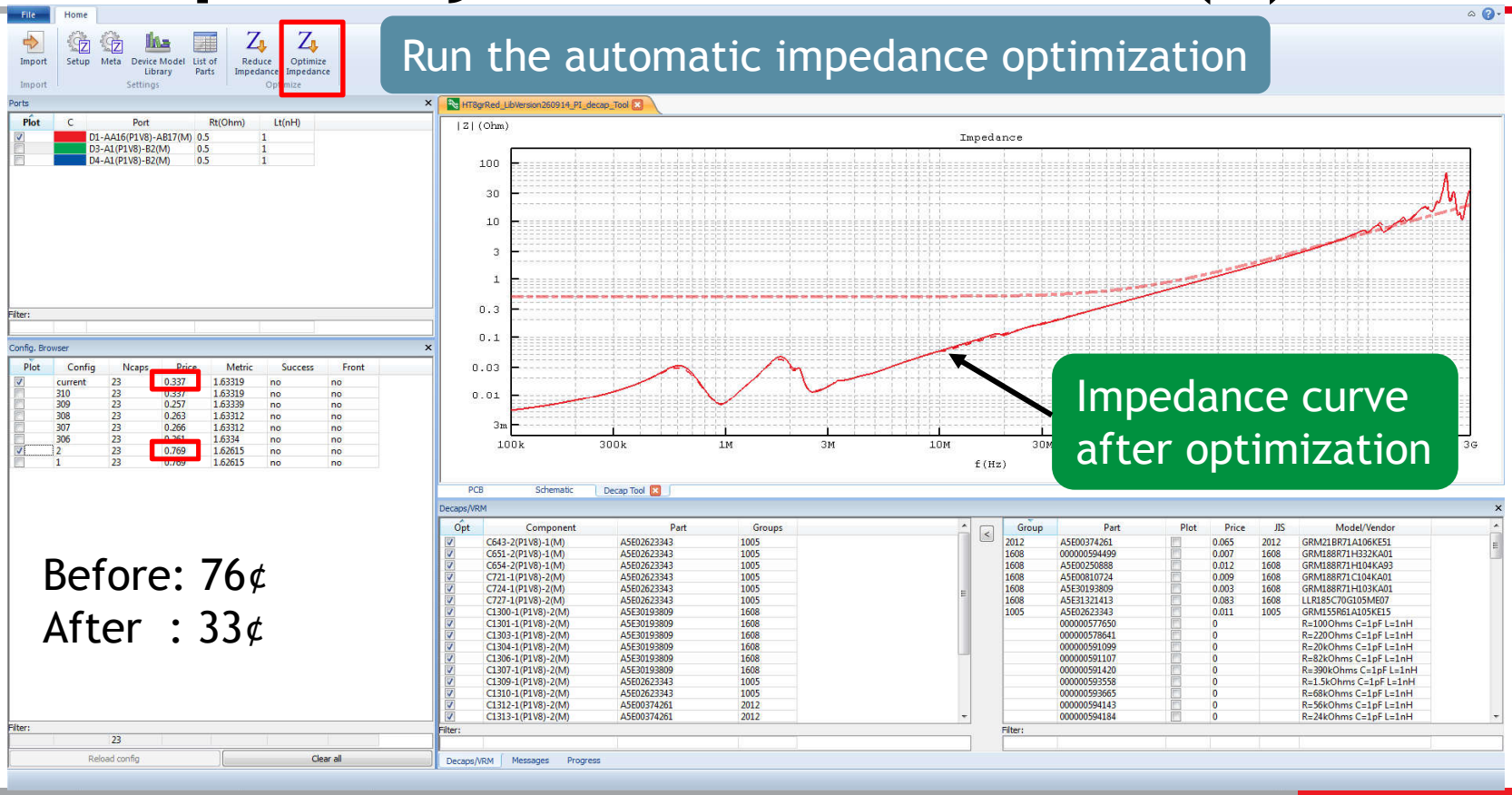
Decap Analysis Tool Optimization (Step 2)



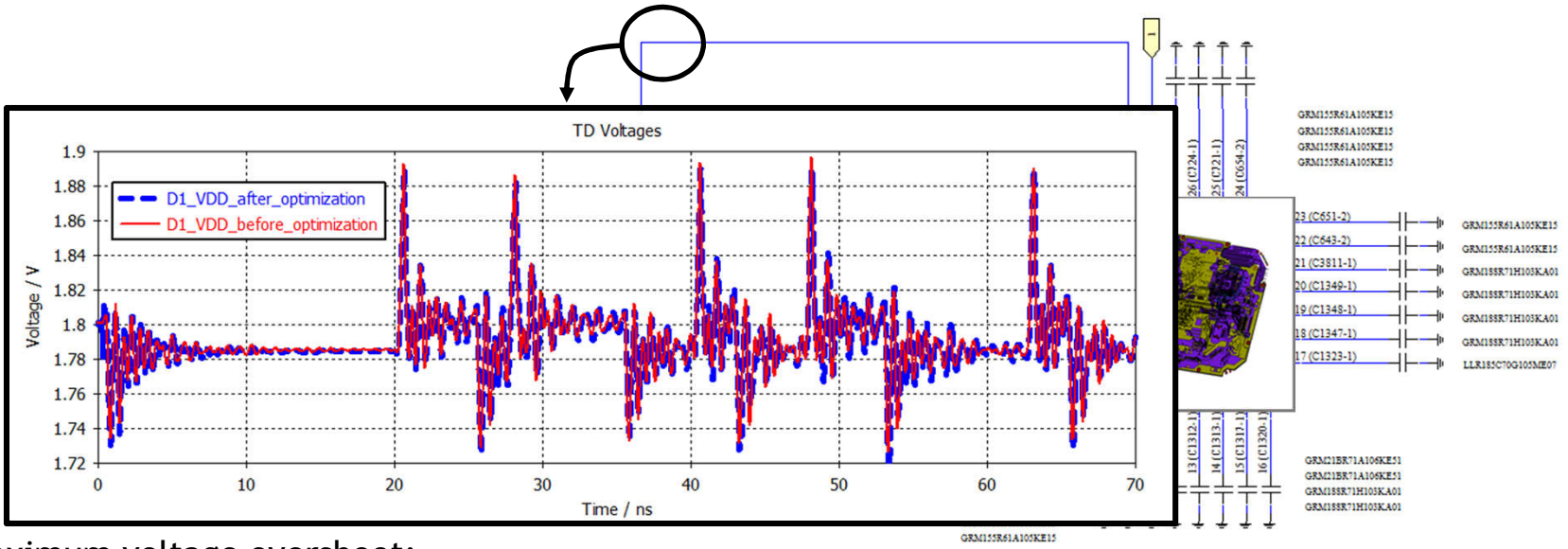
Decap Analysis Tool - Results



Decap Analysis Tool - Results (II)



Transient Simulation Schematic



Maximum voltage overshoot:

- Before: 1.8961V→After: 1.8906V

Number of components:

- Before: 23 → After: 23

56%

Save 43¢

VDD Specification

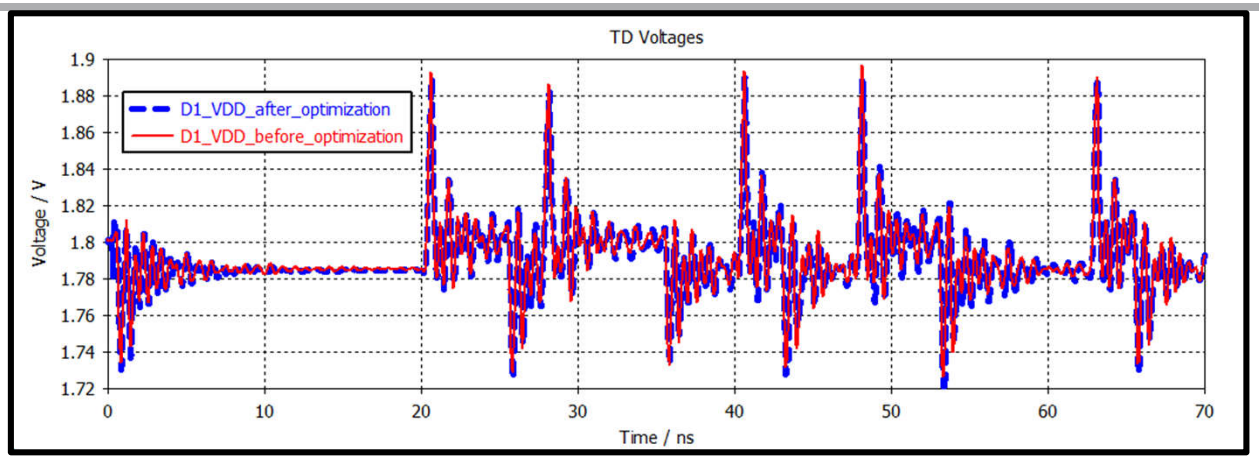


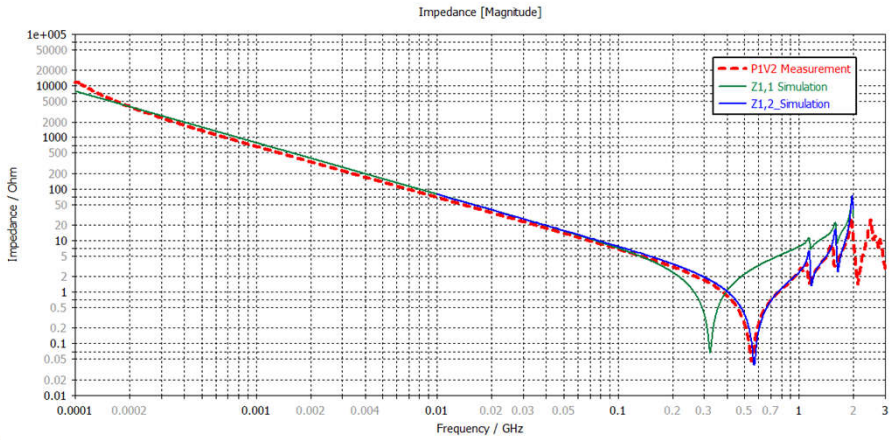
Table 17 — Recommended DC operating conditions (SSTL_1.8)

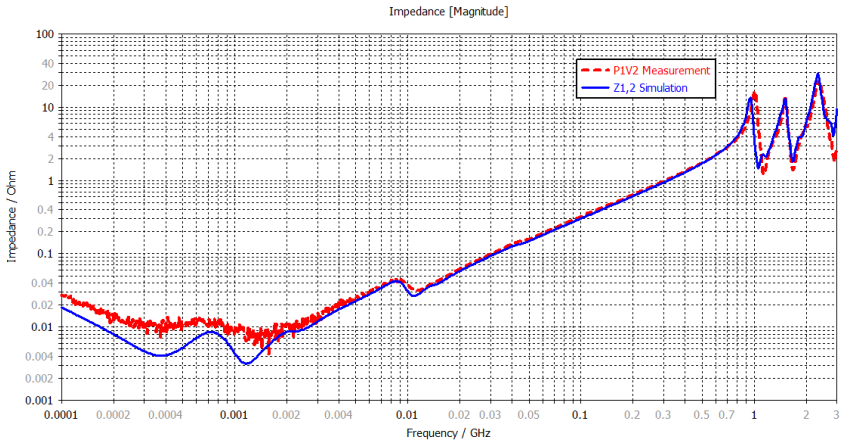
Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	mV	2, 3
VTT	Termination Voltage	VREF - 0.04	VREF	VREF + 0.04	V	4

NOTE 1 There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must be less than or equal to VDD.
NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2 % VREF(dc).
NOTE 4 VTT of transmitting device must track VREF of receiving device.
NOTE 5 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

The VDD specification:
VDD_min= 1.7 – 2% of VDDQmin = 1.66 V
VDD_max= 1.9 + 2% of VDDQmax = 1.938V

Comparison





Measurement of bareboard

Measurement with decaps

Conclusions

Signal Integrity

- Efficient SI simulation with 2DTL method
- Corner simulation for different IBIS model, fast and slow
- Exchange layout and SAM capability for case study

Power Integrity

- PEEC method for Inductance calculation
- Decap tool analysis for optimizing the PDN impedance
- SSO simulation incl. IBIS I/O buffer for more realistic result
- Excellent prediction of simulation result compare to measurement