Automotive PCB SI and PI analysis
SI - PI Analysis

**Signal Integrity**
- S-Parameter
- Timing analysis
- Eye diagram

**Power Integrity**
- Loop / Partial inductance
- DC IR-Drop
- AC PDN Impedance
- Power Aware SI
Signal Integrity

- 8 bits DDR2 lines
- IBIS model for the driver (controller) and the receiver (DRAM)
- Using 2DTL Method
SI-TD Analysis — Timing Analysis

Receiver results for “typical” IBIS Model

400ps delay driver → receiver

e.g. DQ1
Timing Analysis for Different IBIS Model

- Buffers characteristic are process, voltage, and temp dependent.
  - “fast”: high voltage and low temp
  - “slow”: low voltage and high temp

Recommended to simulate both “slow” and “fast” (envelope)
Timing Analysis - Eye diagram
Deliver the transfer function spectrum (s-parameter) of the DQ lines
Post Processing

Quick eye diagram generation with high bit rates, z.B. PRBS with N=7

70ps skew between the data lines
Create Simulation Projects

Net Selection
- DATA Nets
- ADDR Nets
- USB
- Ethernet

Termination
- DS34_ODT40
- DS34_ODT60
- DS34_ODT120
- DS40_ODT40
- DS40_ODT60
- DS40_ODT120
- DS48_ODT40
- DS48_ODT60
- DS48_ODT120

Results
- S-Params
- Eye
- Signals

2D / 3D
- SI PCBS
- SI 3D
- EMC
Exchange Layout
Power Integrity

- DC analysis: IR-drop
- PDN Impedance
- Time domain simulation

VRM → PDN → Die

Total Noise

IR-drop margin

AC noise Margin
### IR-Drop Simulation

<table>
<thead>
<tr>
<th>Component</th>
<th>Voltage (V)</th>
<th>VDD Drop (V)</th>
<th>GND Drop (V)</th>
<th>DC Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory controller Group</td>
<td>1.78849</td>
<td>10.507m</td>
<td>1.007m</td>
<td>575mOhm</td>
</tr>
<tr>
<td>Memory Module I Group</td>
<td>1.7889</td>
<td>10m</td>
<td>0.969m</td>
<td>498mOhm</td>
</tr>
<tr>
<td>Memory Module II Group</td>
<td>1.789</td>
<td>9.409m</td>
<td>0.929m</td>
<td>469mOhm</td>
</tr>
</tbody>
</table>

![Diagram](image)

**JEDEC 79-2F**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply Voltage</td>
<td>1.7</td>
</tr>
<tr>
<td>VDDL</td>
<td>Supply Voltage for DLL</td>
<td>1.7</td>
</tr>
<tr>
<td>VDDQ</td>
<td>Supply Voltage for Output</td>
<td>1.7</td>
</tr>
<tr>
<td>VREF</td>
<td>Input Reference Voltage</td>
<td>0.49 x VDDQ</td>
</tr>
<tr>
<td>VTT</td>
<td>Termination Voltage</td>
<td>VREF - 0.04</td>
</tr>
</tbody>
</table>

**19 CPU pins, 16 Mem I pins & 16 Mem II pins @ 20mA**
Power Delivery Network (PDN) Impedance

PCB inductance and via inductance contribute at higher frequency

- Increasing the impedance between source and load
Vias Characterization

Via Loop Inductance

\[ L_{\text{loop}} = L_{11} + L_{22} + L_{33} + L_{44} - 2M_{12} - 2M_{34} \]

Partial Inductance of Via

\[ L = 5.08h \left[ \ln\left(\frac{2h}{d}\right) - 1 \right] \] [pH] and mils
Simulation Setup

Inductance is influenced by the loop area

\[ L = \frac{\text{Im}(Z)}{\omega} \]

<table>
<thead>
<tr>
<th>10mils</th>
<th>20mils</th>
<th>30mils</th>
<th>40mils</th>
<th>50mils</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.6</td>
<td>0.77</td>
<td>0.93</td>
<td>1.1</td>
<td>1.25</td>
</tr>
</tbody>
</table>

Via pad Ø 12mils
Transition Length 10mils
Via barrel Ø 8mils

6mils
37mils

40mils
Plane Partial Inductance

All the power pins are group together

PEEC Method
Spatial PDN Impedance Plot

Impedance plot on P1V8 plane seen from memory controller

Impedance plot on P1V8 plane seen from memory module I

Impedance plot on P1V8 plane seen from memory module II

@2.6GHz
Decap Placement

Decaps shifts the high impedance at its placement area

220pF
SSO Analysis for 2 DQ lines

- DDR2-400 I/O Buffer IBIS
- PRBS N=7

**Diagram:***
- 11010101101...
- 2 I/O Buffer: Driver
- 2 I/O Buffer: Input
- VRM

**Table:**

<table>
<thead>
<tr>
<th>Number Mesh</th>
<th>15M cells</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Usage</td>
<td>6 GByte</td>
</tr>
<tr>
<td>Simulation Time</td>
<td>2xT10: 45 h 31m Kepler40: 32 h</td>
</tr>
</tbody>
</table>
Transient Response

With Decaps

No Decaps

Power Supply VDD

DC Drop during write mode
Over designing the PCB ➔ Additional BOM cost ➔ slightly or without performance improvement

**Decap Analysis Tool**

Multiple goals:
- Optimizing the BOM cost
- Optimizing the PDN impedance

1. Define the target impedance
2. Define the list of parts for optimization
3. Start the optimization
Decap Analysis Tool Optimization (Step 1)

Target Impedance

Part lib. of current Decaps mounted on PCB
Decap Analysis Tool Optimization (Step 2)

Removing the decaps from PCB (Bare board)
Decap Analysis Tool - Results

Locate the marker to impedance curve manually and optimizing the impedance

Impedance curve with 10 decaps

Initial config. with 23 decaps

Before: 76¢
After: 52¢
Decap Analysis Tool - Results (II)

Run the automatic impedance optimization

Impedance curve after optimization

Before: 76¢
After : 33¢
Transient Simulation Schematic

Maximum voltage overshoot:
- Before: 1.8961V → After: 1.8906V

Number of components:
- Before: 23 → After: 23

56% Save 43¢
VDD Specification

The VDD specification:

VDD\_min = 1.7 - 2% of VDDQ\_min = 1.66 V
VDD\_max = 1.9 + 2% of VDDQ\_max = 1.938V
Comparison

Measurement of bareboard

Measurement with decaps
Conclusions

Signal Integrity

- Efficient SI simulation with 2DTL method
- Corner simulation for different IBIS model, fast and slow
- Exchange layout and SAM capability for case study

Power Integrity

- PEEC method for Inductance calculation
- Decap tool analysis for optimizing the PDN impedance
- SSO simulation incl. IBIS I/O buffer for more realistic result
- Excellent prediction of simulation result compared to measurement