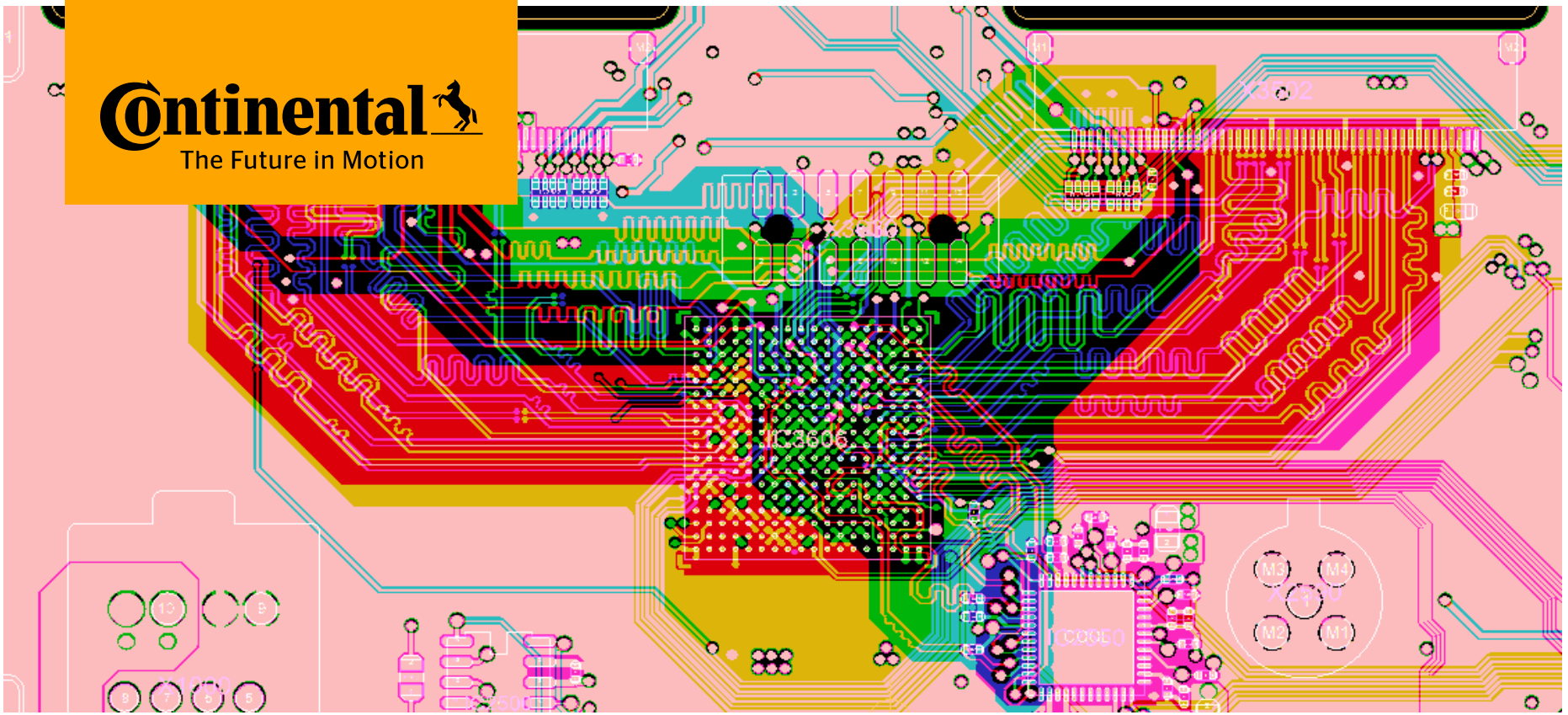
Continental
The Future in Motion



TIE Plus.

The step towards interconnect simulation technology

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Team Leader - EE Simulation & Controller Platforms
Technical Expert - Signal & Power Integrity
Continental Automotive, Interior Division

Agenda

1. The world of virtual prototyping
2. TIE Plus definition and objectives
3. Why signal integrity ?
4. SI Design & Simulation Flow
5. SI simulation software
6. TIEplus 2015 review
7. A look at TIEplus 2015 subject
8. Contest topics and recommended bibliography
9. Contest workflow

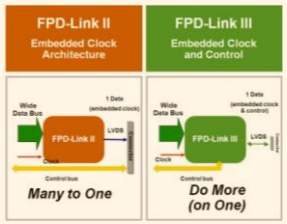
Today’s electronic market drivers

Technologies

ddr3 A JEDEC STANDARD

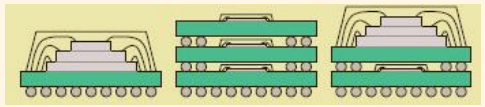
DDR4

3D Graphical Processors



High-Speed Serial Links

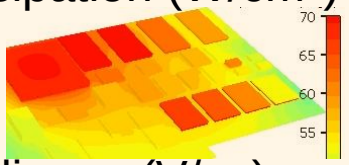
Wireless Data transfer



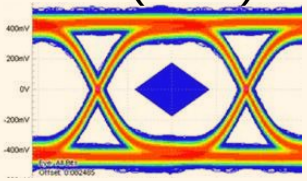
Packaging Technologies (SiP, SoC)

Challenges

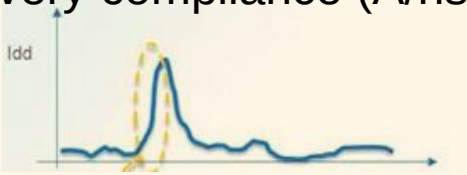
- ❑ thermal dissipation (W/cm^2)



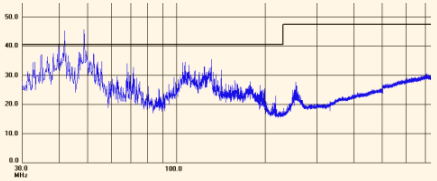
- ❑ signal compliance (V/ns)



- ❑ power delivery compliance (A/ns)

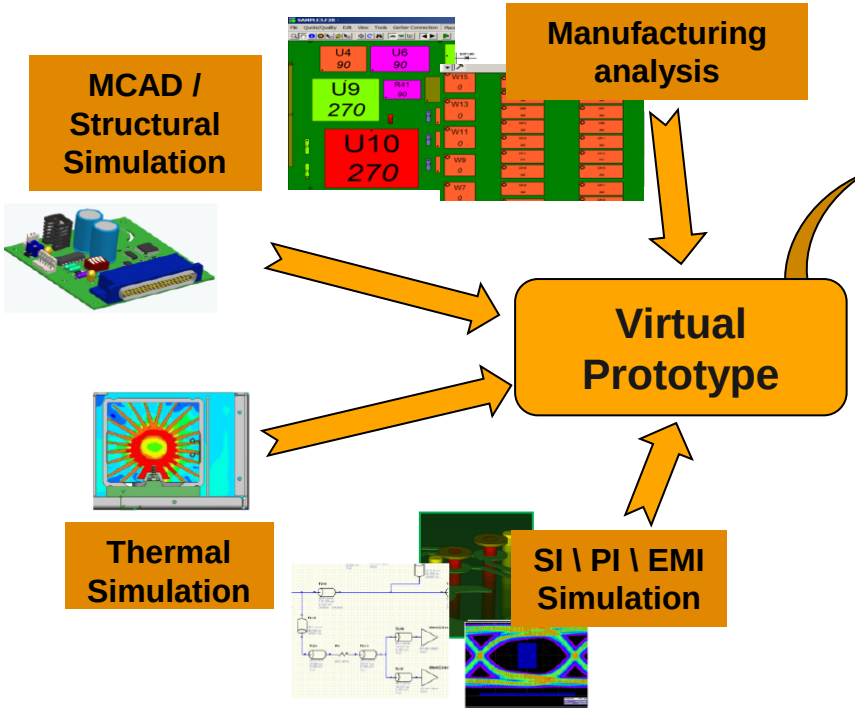


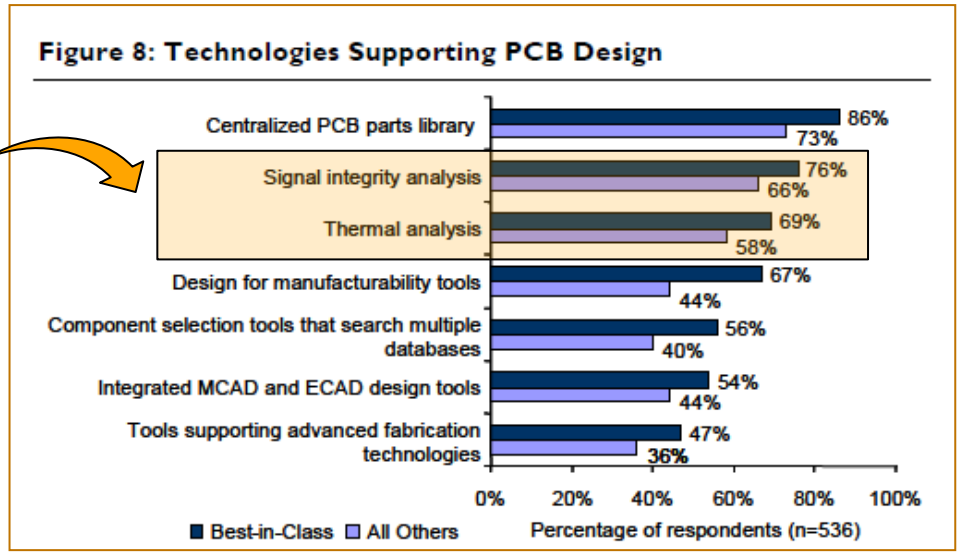
- ❑ EM compatibility (dBuV/m)



Virtual Prototyping

- Virtual prototyping = the usage of computer based modeling and simulation techniques for the definition of a multidisciplinary model of the device under development (with the goal of predicting physical behavior in different use cases)





Source: Aberdeen Group Market Study "Why PCB Design Matters to the Executive", Feb. 2010

- "Ideal world" goal → Get it right the first time !
- "Real R&D world" goal → Reduce number of design loops, prototype costs, development time

TIE Plus Objectives

- TIE Plus = a new contest challenge under the TIE brand, dedicated to virtual prototyping disciplines that support high-complexity PCB design
- Objectives:
  - Promoting simulation based PCB design disciplines in universities and R&D centers
  - Stimulating the development of future specialist in the field of interconnect simulation in a accordance to best-in-class companies demands
  - Create a collaborative-competitive environment where the contestants presents their technical solutions, but also exchange ideas on simulation approaches and get in touch other PCB design professionals
- Subject topics for upcoming editions of TIE plus:
  - Signal Integrity (SI) -> simulations for signal integrity associated with wired data transmissions at PCB and system level
  - Power Integrity (PI) -> simulation power supply distribution networks in high frequency digital applications

Why SI & PI as primary topics for TIE Plus?

Job add for HP - PCB Designer-1384259

Desired Skills

- Advanced knowledge of PCB Design Guidelines, including a working knowledge of electronics including signal integrity issues and design constraints, and demonstrated ability to recommend and implement layout solutions to improve circuit functionality and signal integrity.
- Advanced knowledge in the use of ECAD/ECAE/ECAM software including the ability to create process improvements and enhancements.
- Demonstrated experience and ability with PCB layout and DRC applications, specifically Cadence Allegro, Allegro Design Workbench, Constraint Manager, Mentor BoardStation, and Valor NPI
- Demonstrated ability to modify and/or develop scripts and macros used in the PC board layout, verification, and interfacing processes.
- In-depth knowledge of multiple (at least two) PC board fabrication and assembly process technologies.

Experience:

- Experience with HP internal documentation requirements
- Experience designing high-performance PCB layouts for use in consumer products
  - Rules Driven Designs (Constraint Manager, Constraint Editor)
  - Schematic and CAD Library Creation and Maintenance
  - Signal Integrity / Design Verification
  - High Speed Backplane / Mid-plane Design
  - Single Ended and Differential Controlled Impedance Design
  - Design for Manufacture / Test / Assembly
  - Micro BGA / Micro Via / Blind & Buried Vias
- Experience working on all phases of new product design and manufacturing
- Experience working with external vendors to produce and qualify new parts and tools

Job add for Seagate
Electrical PCB Designer -151953

Typical duties:

- Determines design approaches and parameters.
- Review – advise on vendor technology capability to support development.
- Exercises judgment in selecting methods, techniques and evaluation criteria for obtaining results.
- Determines methods and procedures on new assignments.

Qualifications

Required skills

- 5+ years of mixed signal PCB and Flex Circuit layout experience.
- Experience with Mentor Graphics DxDesigner, CES, and Expedition PCB.
- Experience with power integrity/power distribution.

Preferred skills

- Bachelor's degree in Engineering.
- Experience routing high speed signals (to 12 GHz range) for signal integrity.

Job add for Analog Devices
Sr PCB Layout Engineer - 150620

Qualifications

- BSET or 10-15 years experience as a PCB Designer
- Experience with Cadence Allegro & Concept HDL version 16.5 required
- Design of printed circuit boards requiring differential pairs, high speed and controlled impedance
- Knowledge of IPC standards
- Knowledge of latest PCB materials and finishes, fabrication and assembly process.
- Proven practical experience of the complete design process from understanding of customer requirements through the release to manufacturing.
- Experience with blind/buried vias and via in pad with sequential lamination and .5mm BGA's.
- Candidate must have good communication skills - both written and oral.
- Flex/Rigid Flex experience is a plus
- Knowledge of Unix/Linux computers a plus

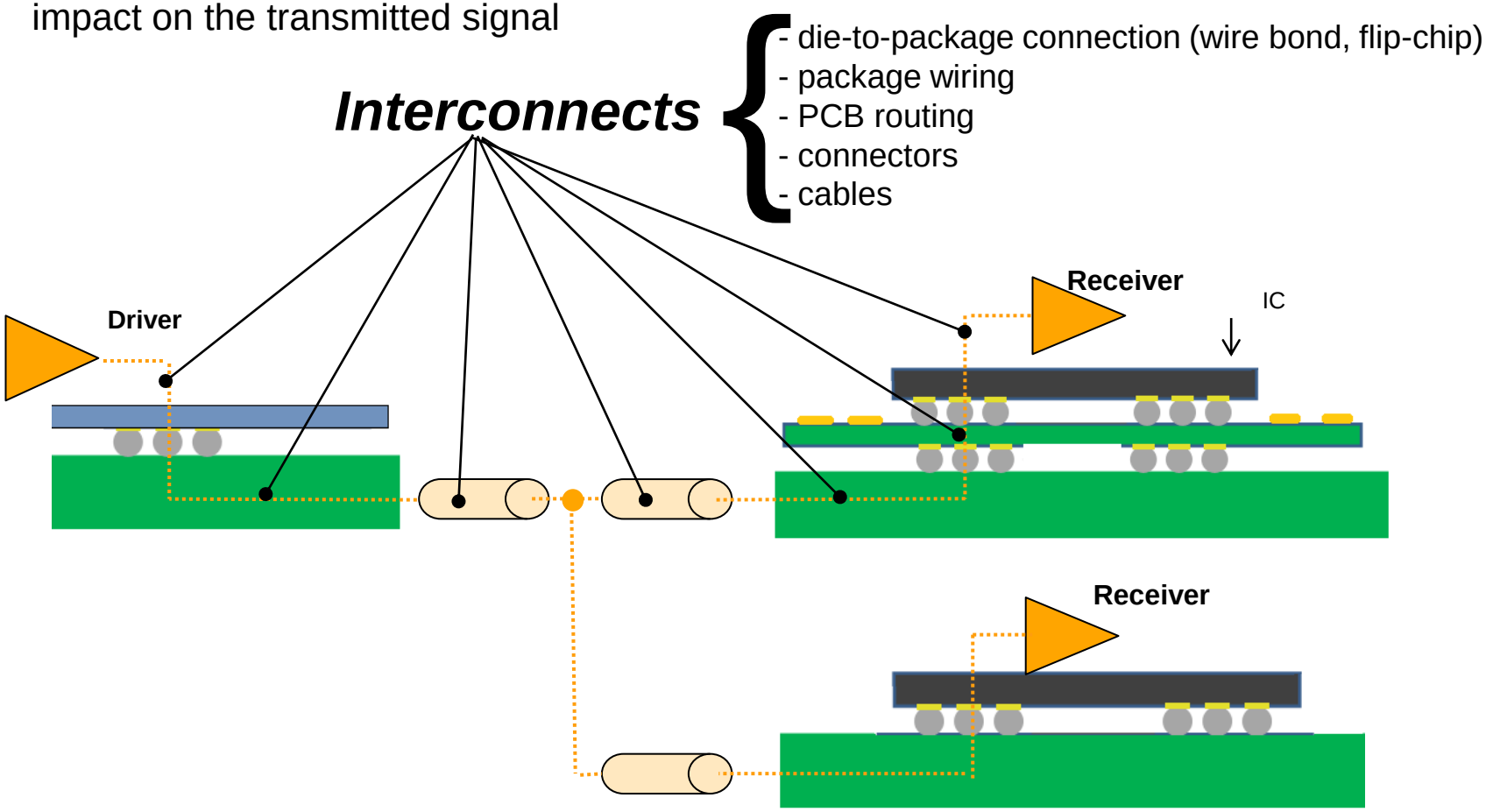
What is high speed ?

- As the variation speed of electric signals increases, physical properties of the interconnect structures can induce unwanted signal distortion
- Due to the need of high data rates (implying high frequency), the signal's rise&fall times become smaller and smaller (for DDR interfaces tr~0.2-1 ns)
- The interconnect path can be no longer modeled as an RLC structure, but as a transmission line with a electrical behavior described by the telegraphers equations

- The following items fall in to the high speed domain and must be considered in the analysis:
  - interconnect reflections
  - losses due to skin effect
  - crosstalk (near end and far end)
  - interconnect timing delays
  - IC package parasitics
  - IC driver\receiver circuit characteristics

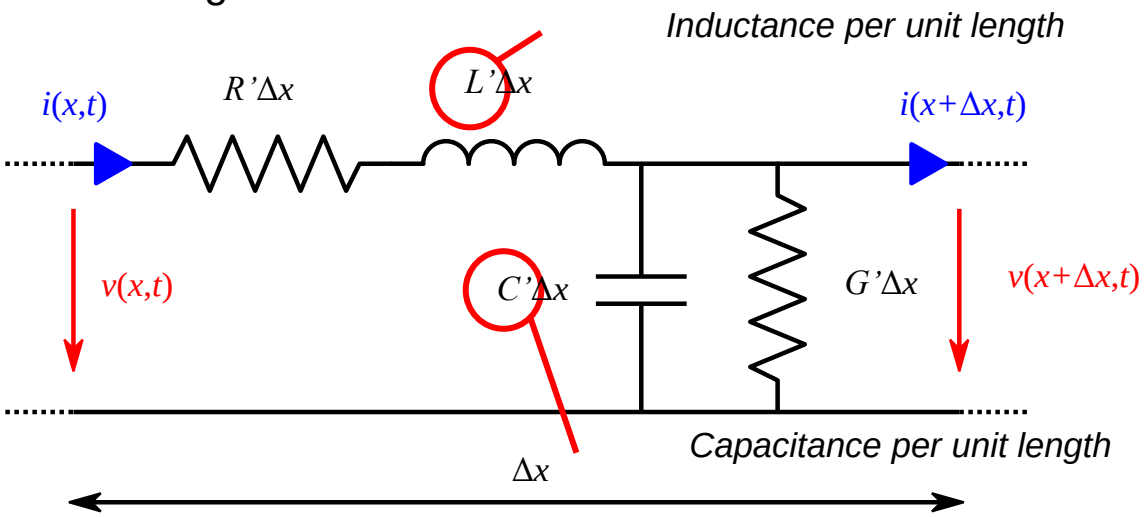
What can be considered an interconnect ?

› Every electrical connection element placed in the signal path is a potential source for signal degradation and its electrical behavior must be characterized in order evaluate the impact on the transmitted signal

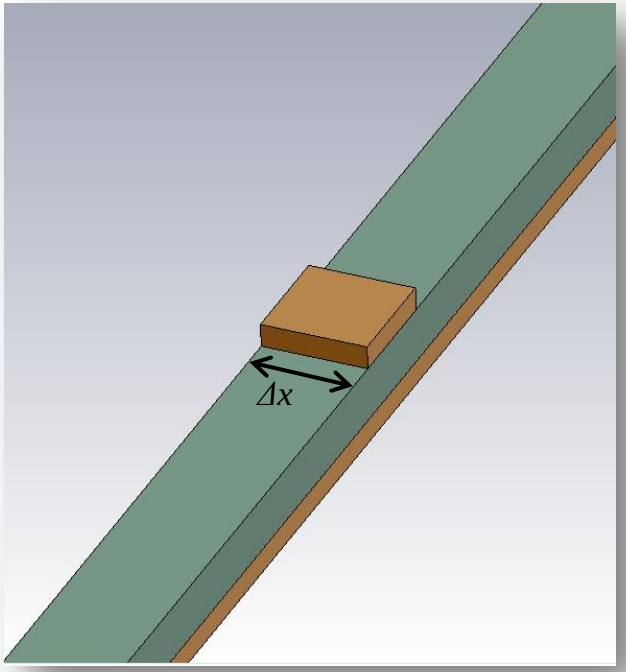


What is a transmission line?

- (At least) two parameters determine a transmission line
  - Propagation speed
  - Characteristic impedance Z_L
- A transmission line can be cut in short pieces having the length Δx:



Transmission Line RLCG segment



What is high speed ?

When do these effects become critical? Rule of thumb (for FR4):

$$l_{max} / \text{inch} < t_r / \text{ns}$$

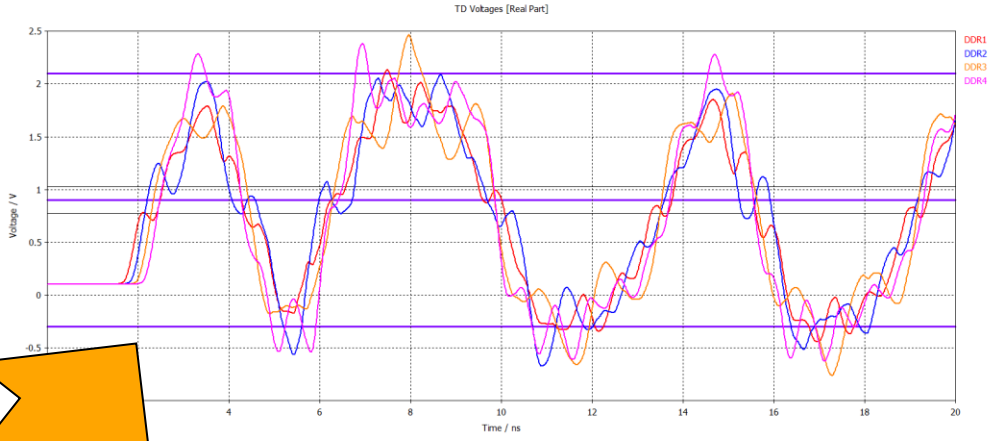
$$l_{max}(mm) <\sim 25 \times t_r(\text{ns})$$

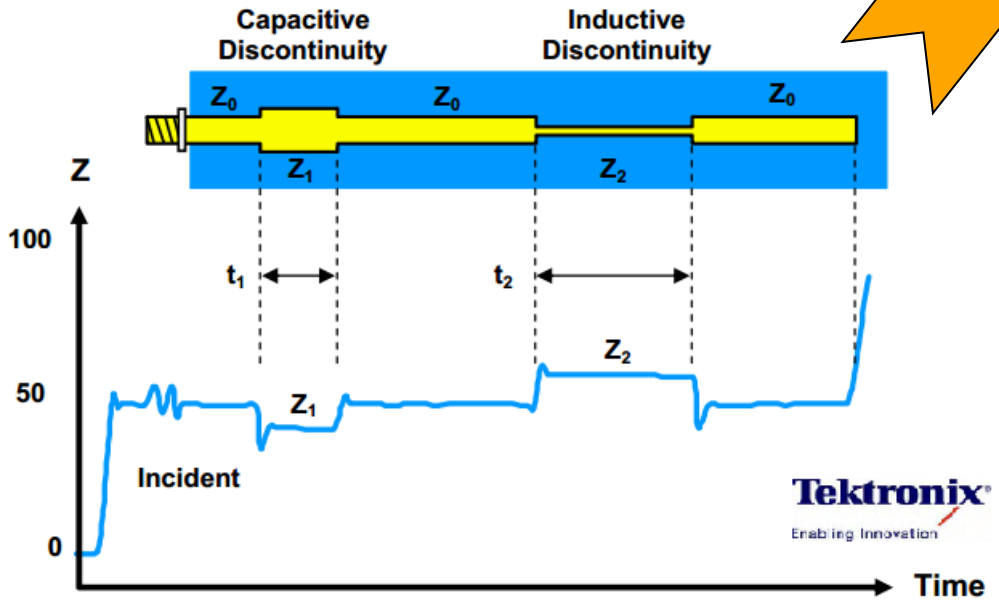
- *Source: Eric Bogatin, Signal and Power Integrity – Simplified, Prentice Hall, 2004*
- *…so for a 25mm trace length, a signal with a rise time < 1ns (for 3.3V logic this would mean ~2V/ns) creates already a SI risk if the interconnect is not properly designed*
- and properly designed for SI means impedance matching at circuit level

- The term “high speed” indicates an unhappy combination of interconnect length and variation speed

Impedance Discontinuities

Changes in interconnect impedance over the signal transmission path will cause distortion depending on driver characteristics (every IC I/O has a non-linear impedance curve) and interconnect discontinuity characteristics.



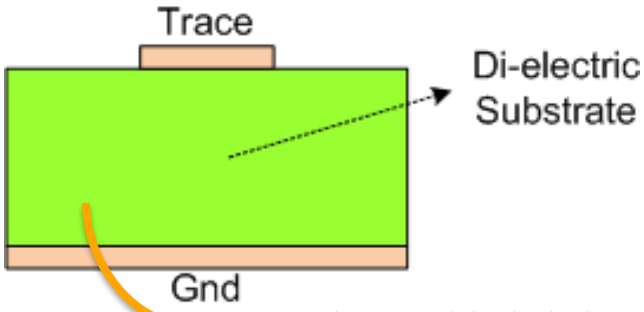


Impedance discontinuities have consequences:

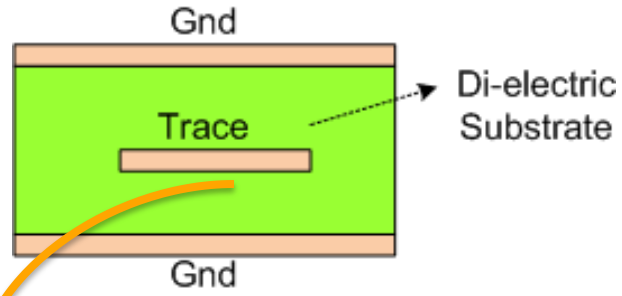
- ❑ overshoot \ undershoot
- ❑ reflections in the triggering region
- ❑ false logic triggering
- ❑ interconnect added jitter
- ❑ timing deviations

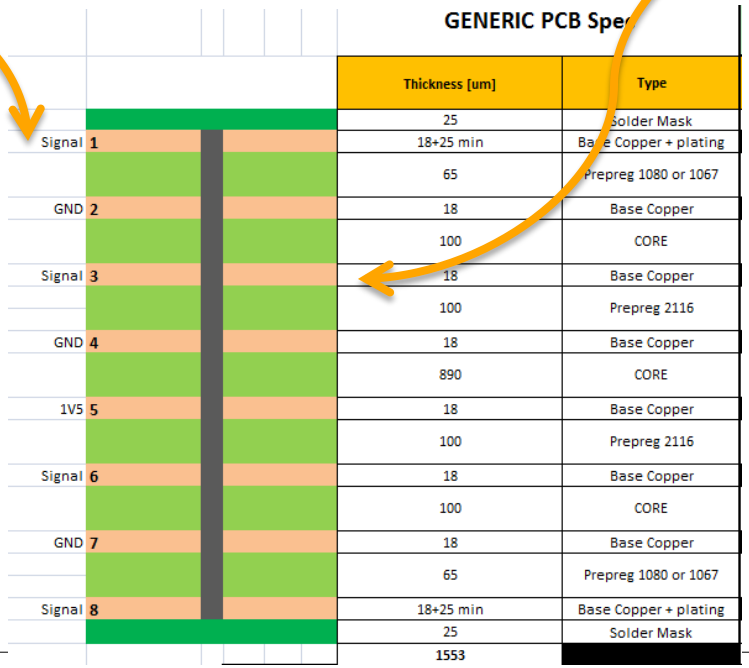
Controlled Impedance Routing

Microstrip



Stripline



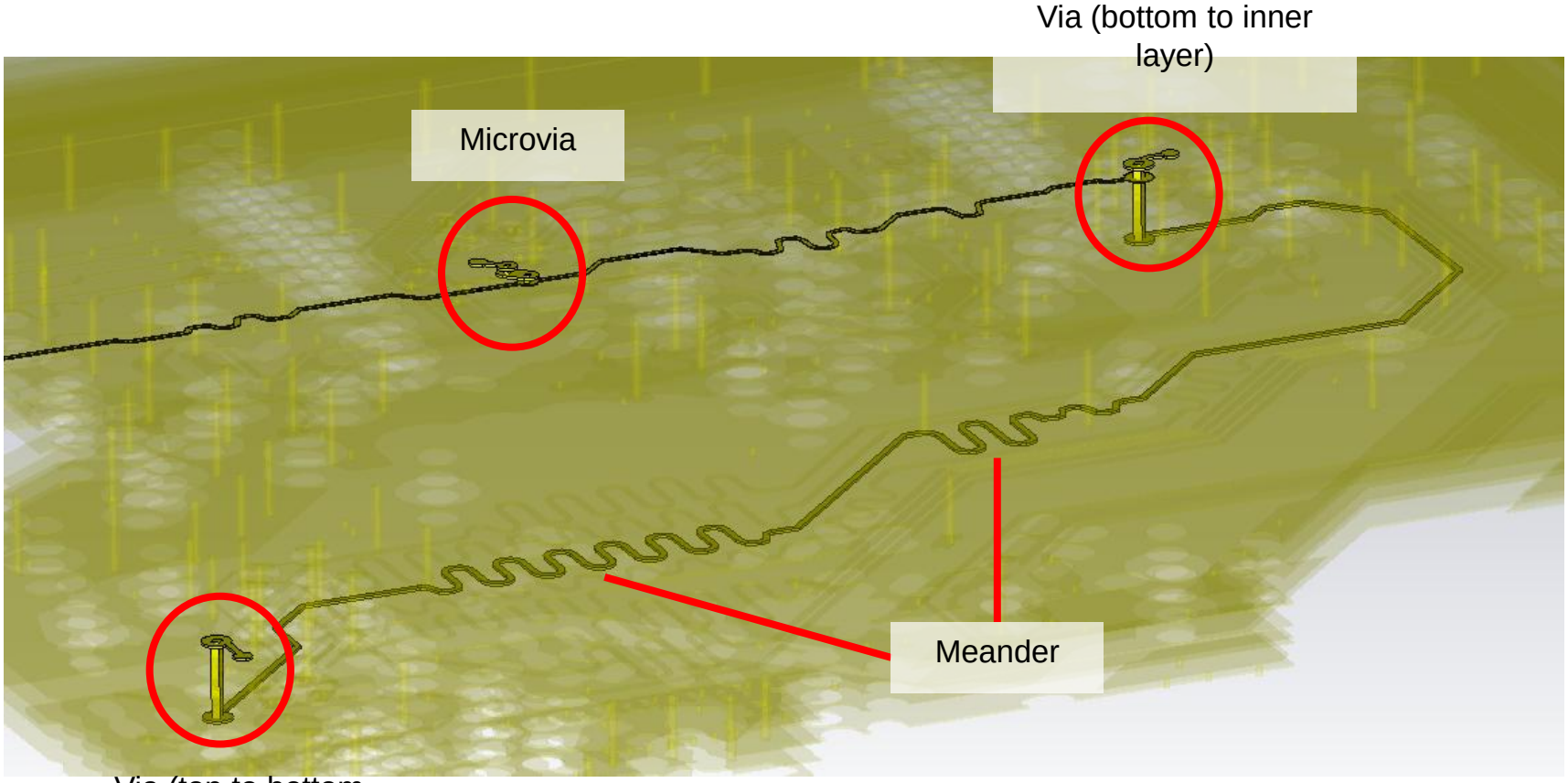


GENERIC PCB Spe

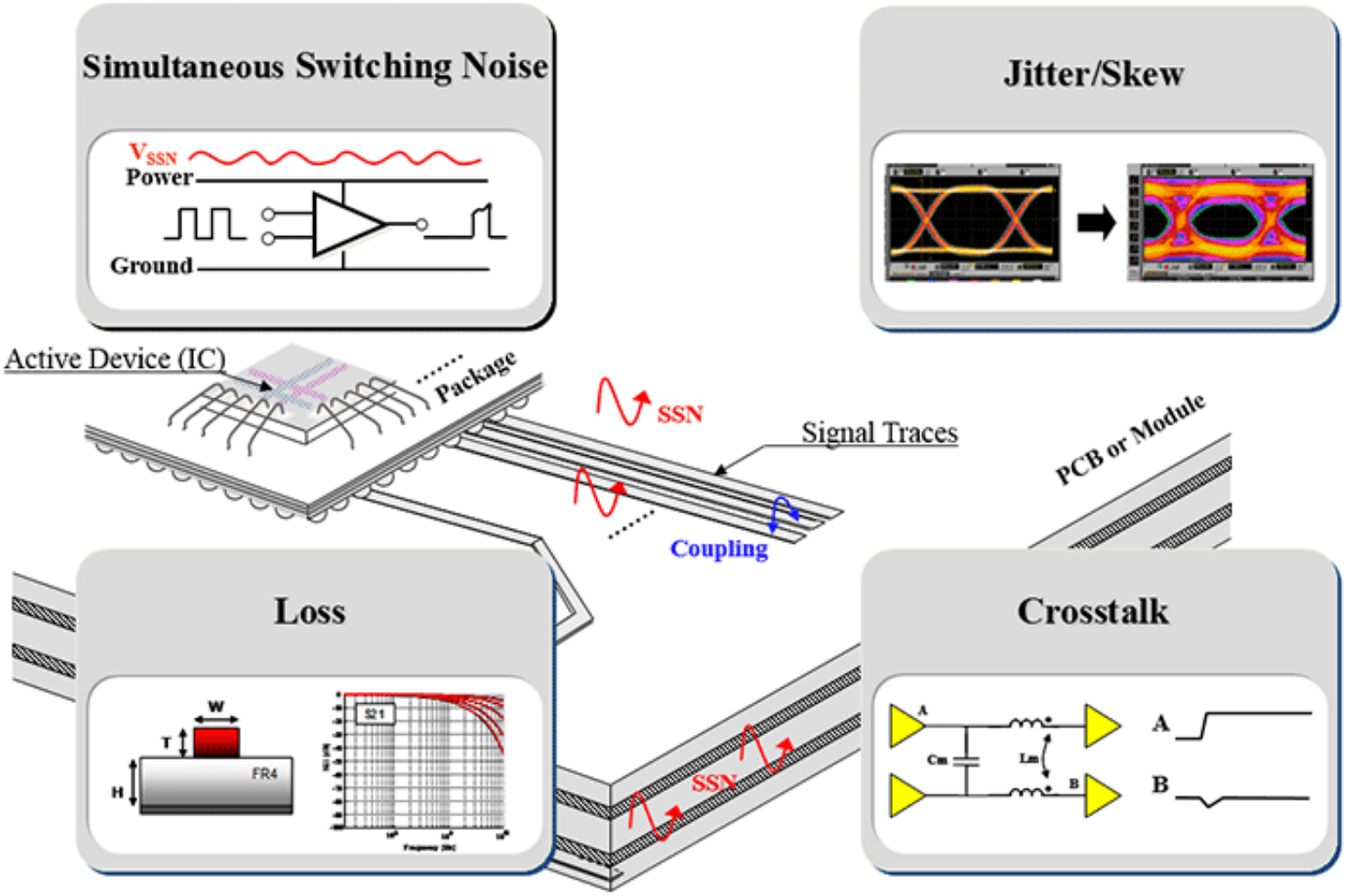
		Thickness [um]	Type
		25	Solder Mask
Signal	1	18+25 min	Base Copper + plating
		65	Prepreg 1080 or 1067
GND	2	18	Base Copper
		100	CORE
Signal	3	18	Base Copper
		100	Prepreg 2116
GND	4	18	Base Copper
		890	CORE
1V5	5	18	Base Copper
		100	Prepreg 2116
Signal	6	18	Base Copper
		100	CORE
GND	7	18	Base Copper
		65	Prepreg 1080 or 1067
Signal	8	18+25 min	Base Copper + plating
		25	Solder Mask
		1553	

But some things can not be avoided …….

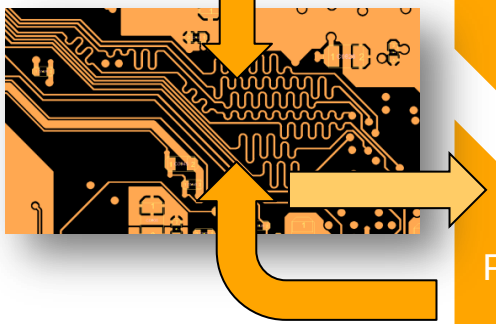
› Reality may look something like this



….and there are some additional EM effects



SI \ PI Workflow



PCB design

layout directives

optimization fine-tuning troubleshooting

Problem Formulation

- evaluate of system\ interface requirements
- define design targets
- define modeling approach

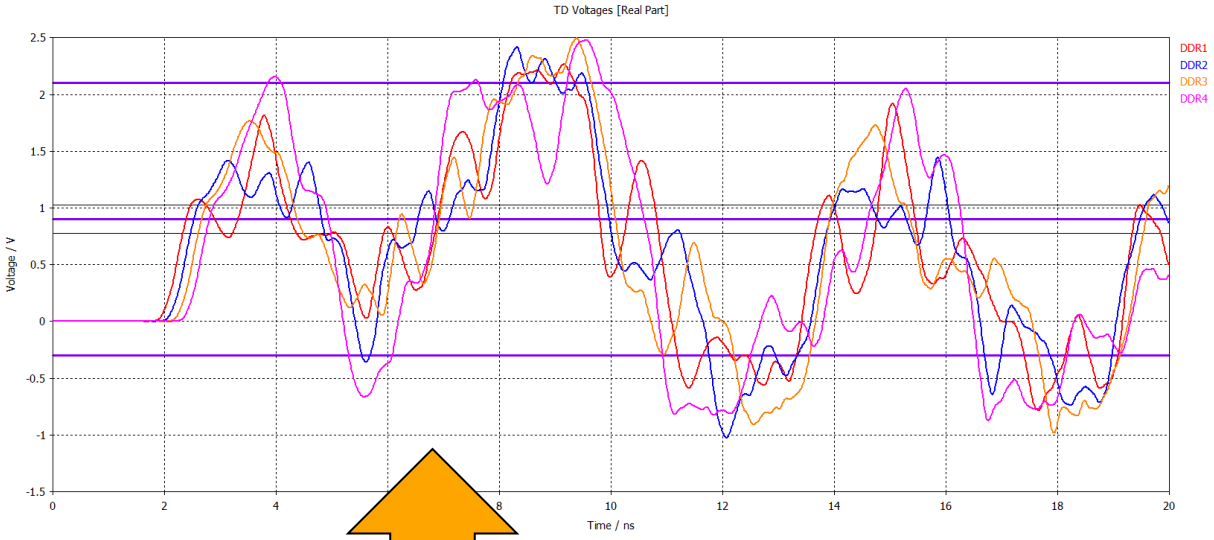
Pre-layout Analysis

- define PCB stack-up (layers, materials)
- “what-if” simulations – explore design possibilities in order to meet interface requirements, obtain best performance/cost ratio

Post-layout Analysis

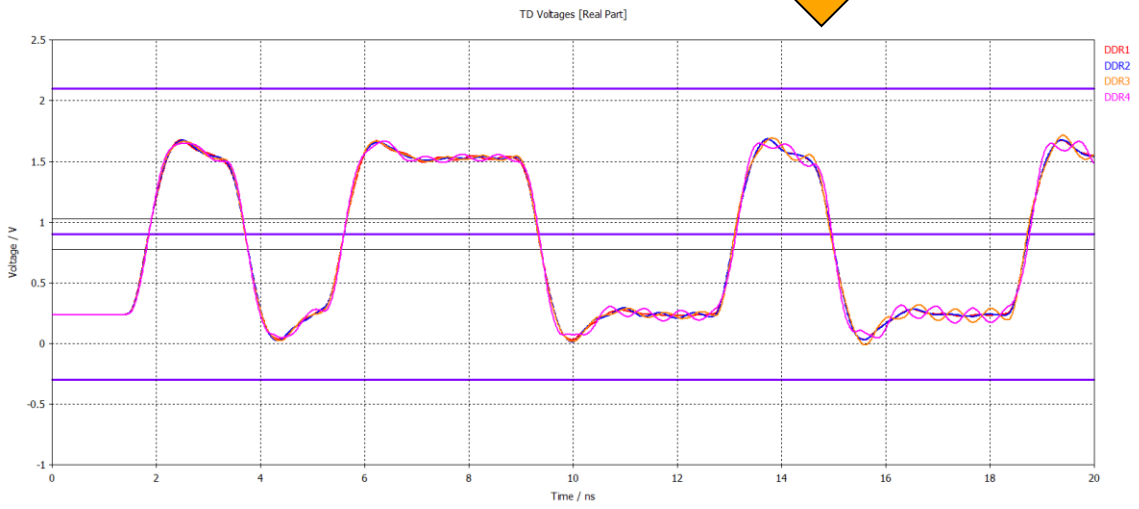
- PCB stack-up and CAD represent the inputs for the simulation
- Identify potential problems that were not considered in pre-layout
- debugging of a physical prototype problem; identify root cause and define possible remedies

High Speed Design makes the difference

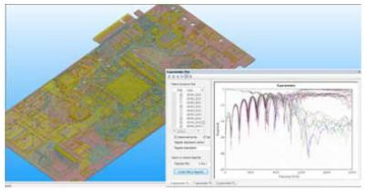


Address line waveforms for a DDR3 multi-drop system before optimization

….and after optimization

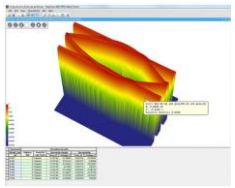


SI & PI Simulation Tools



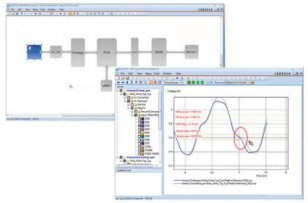
ANSYS

Designer SI, HFSS, SIWave



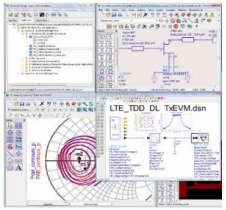
Mentor Graphics

HyperLynx



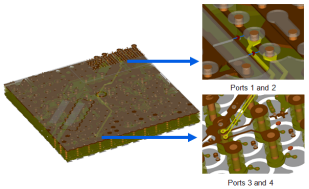
cadence

Allegro Sigrity



KEYSIGHT TECHNOLOGIES

Advanced Design System (ADS)



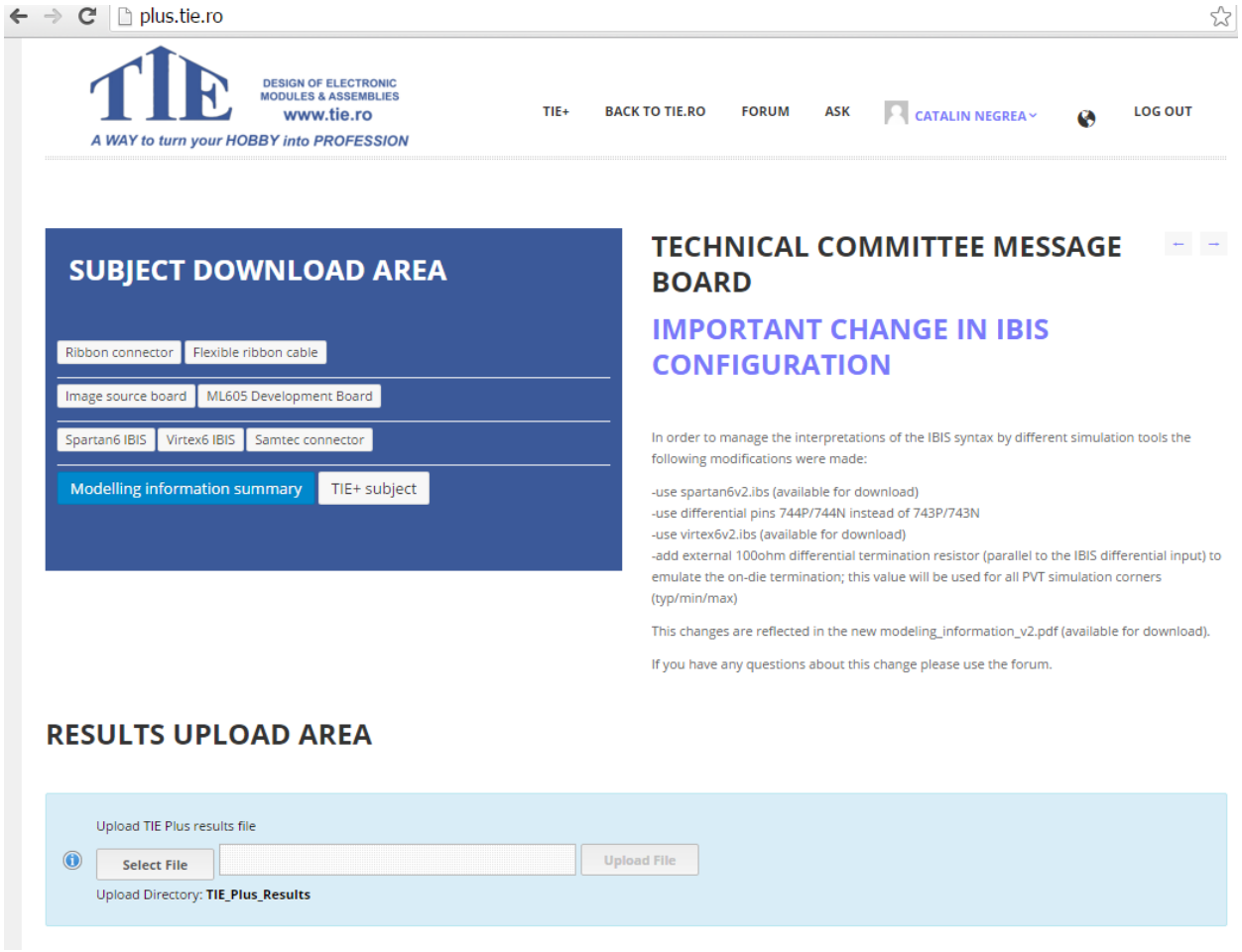
CST

COMPUTER SIMULATION TECHNOLOGY

TIEplus 2015 Review

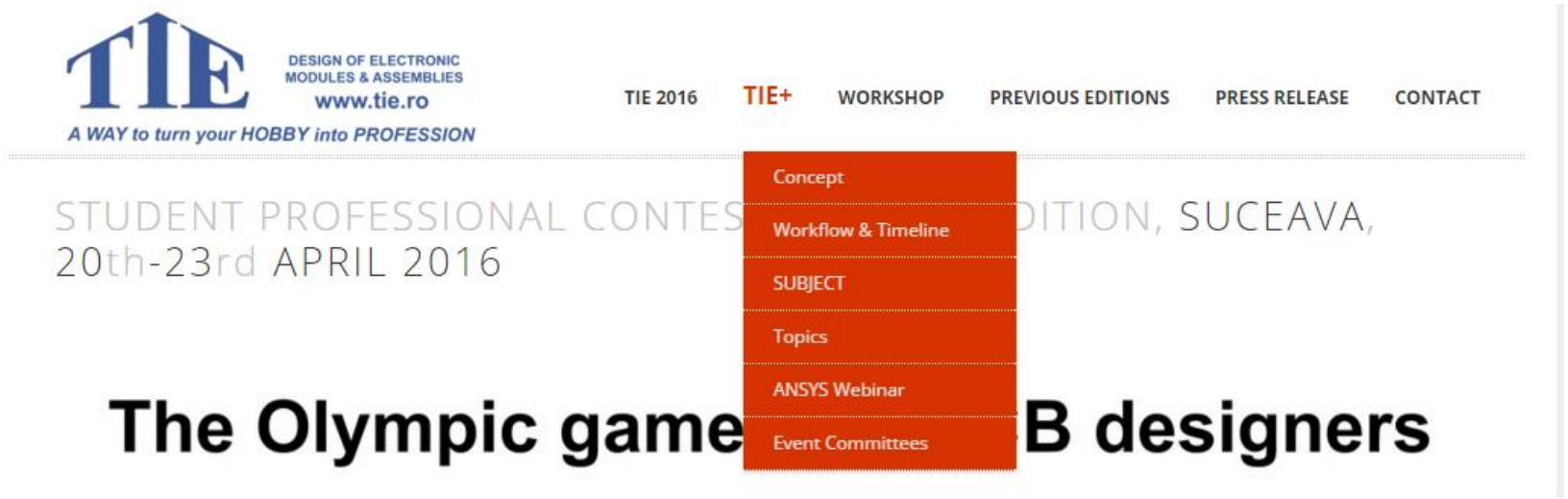
TIE+ 2015 review

› The contest started based on an online platform; the contestants received login credentials after their registration profile has been validated



TIE+ 2015 review

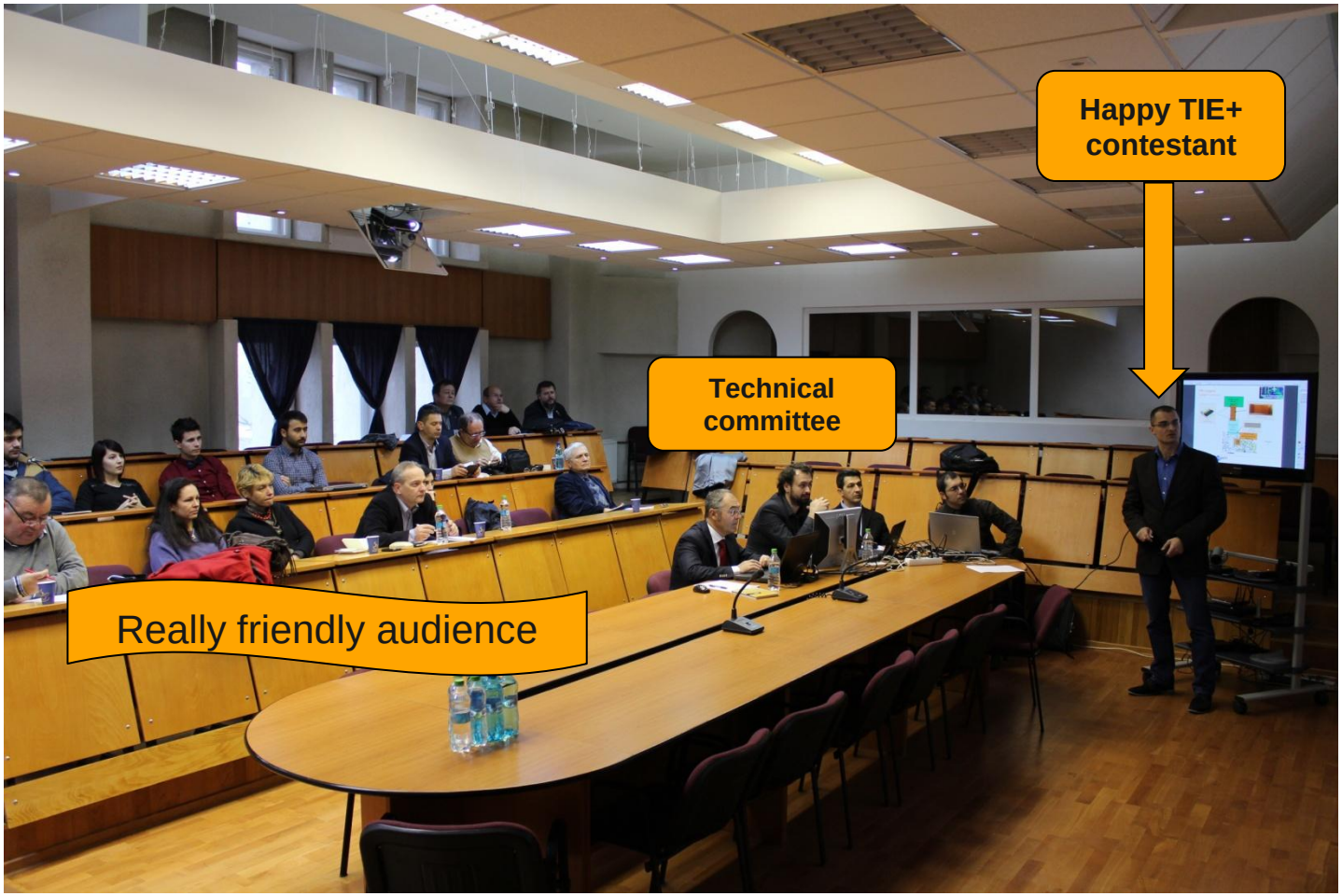
The TIE+ info for the 2015 edition is still available online



- After a 2 week period dedicated to solving the subject the contestants finally got the chance to present their simulation results
- ***The final stage of TIE+ took place at the Stefan cel Mare University of Suceava the next day after the standard TIE seminar***

…. But let's see how TIE+ really looked like…..

Open discussions and dissemination of the obtained results



Each contestant had ~20 minutes to present their work

Then, there is an Q&A session with technical relevant question

In the end everyone was a winner

TIE+2015 group picture

Summary of the first edition

- 11 registered participants from 6 universities
- 4 bachelor students, 5 master students, 2PhD students
- 5 participants made it to Suceava and presented their solutions
- Used software for the solving of the subject: ANSYS, Hyperlynx, CST
- 3 of the participants reached a good level in providing a feasible technical solutions
- The top 3 contestants received a “Certificate of competence in Signal Integrity Simulation”

TIEplus 2015 SUBJECT

TIE+ Subject
General circuit description

The multi-board system overview presented in figure 1 is given, describing an high resolution image acquisition system for quality compliance testing. Figure 2 presents the PCB board connectivity and signal flow.

System description:

- Board 1
  - represents the image source device containing the image source driver IC100 (IBIS model: Spartan6.ibs); the high speed interface consists out of 13 (1*CLK + 12*Data) differential pairs following RSDS specifications (Reduced Swing Differential Signaling)
  - the RSDS signals exit Board1 PCB trough connector B1.X100 and are propagated by a flexible ribbon cable to Board 2
  - the Board1 PCB interconnect model is provided as touchstone file
- Board 2
  - represents the an intermediate connectivity board that is used to connect and organize the RSDS lines to match Board 3 requirements
  - this PCB is under development and requires pre-layout routing directives that will result from the signal integrity analysis
  - the PCB stack-up is provided
- Board 3
  - represents a ML605 development board containing a Virtex6 FPGA
  - the receiver for the RSDS signals of interest and is represented by U1, a Virtex6 FPGA (IBIS Model: Virtex6.ibs)
  - PCB CAD data in ODB++ format and stack-up information are provided

TIE+ Subject
System Overview

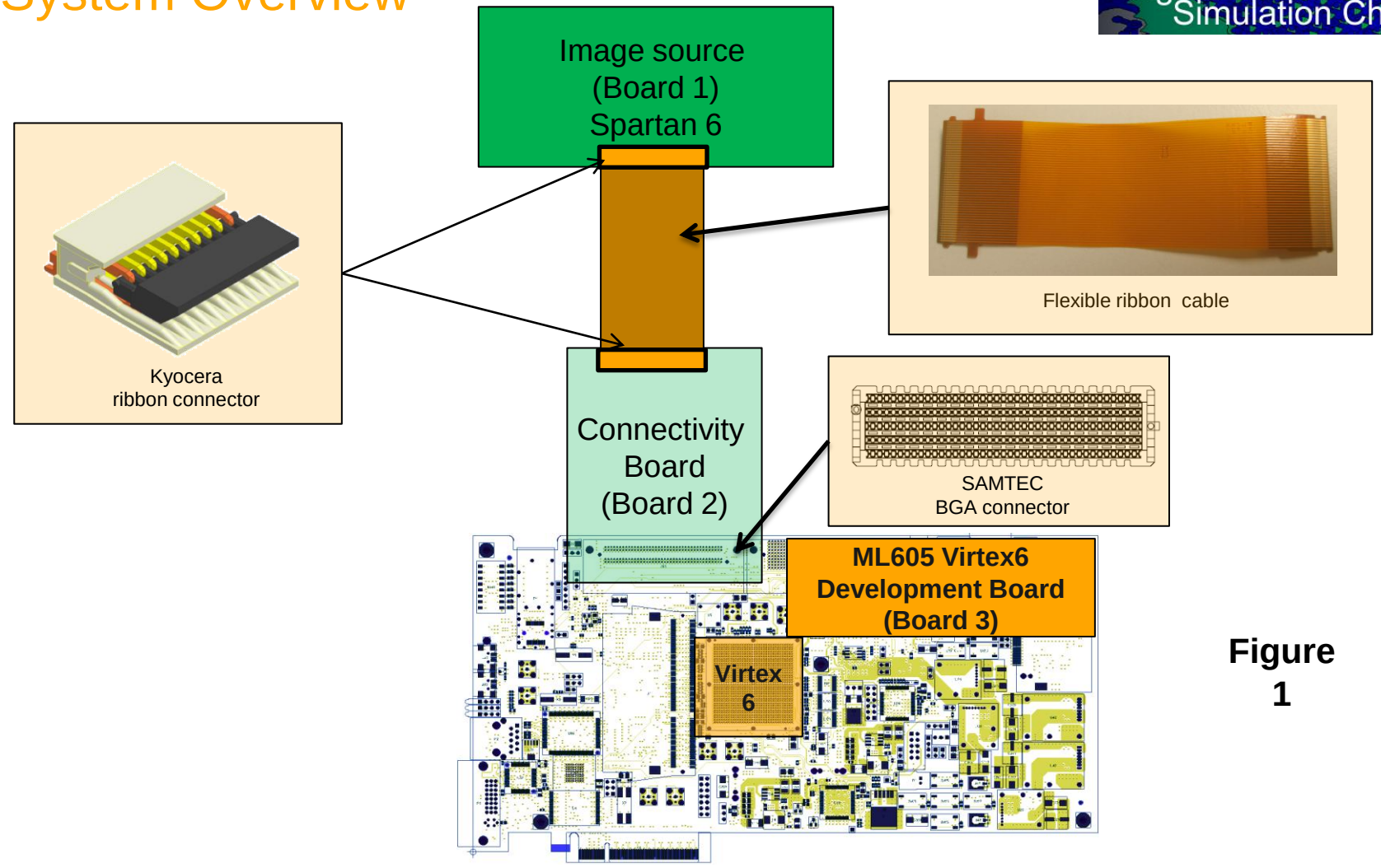


Figure 1

TIE+ Subject

Multi-board system diagram. Signal flow diagram.

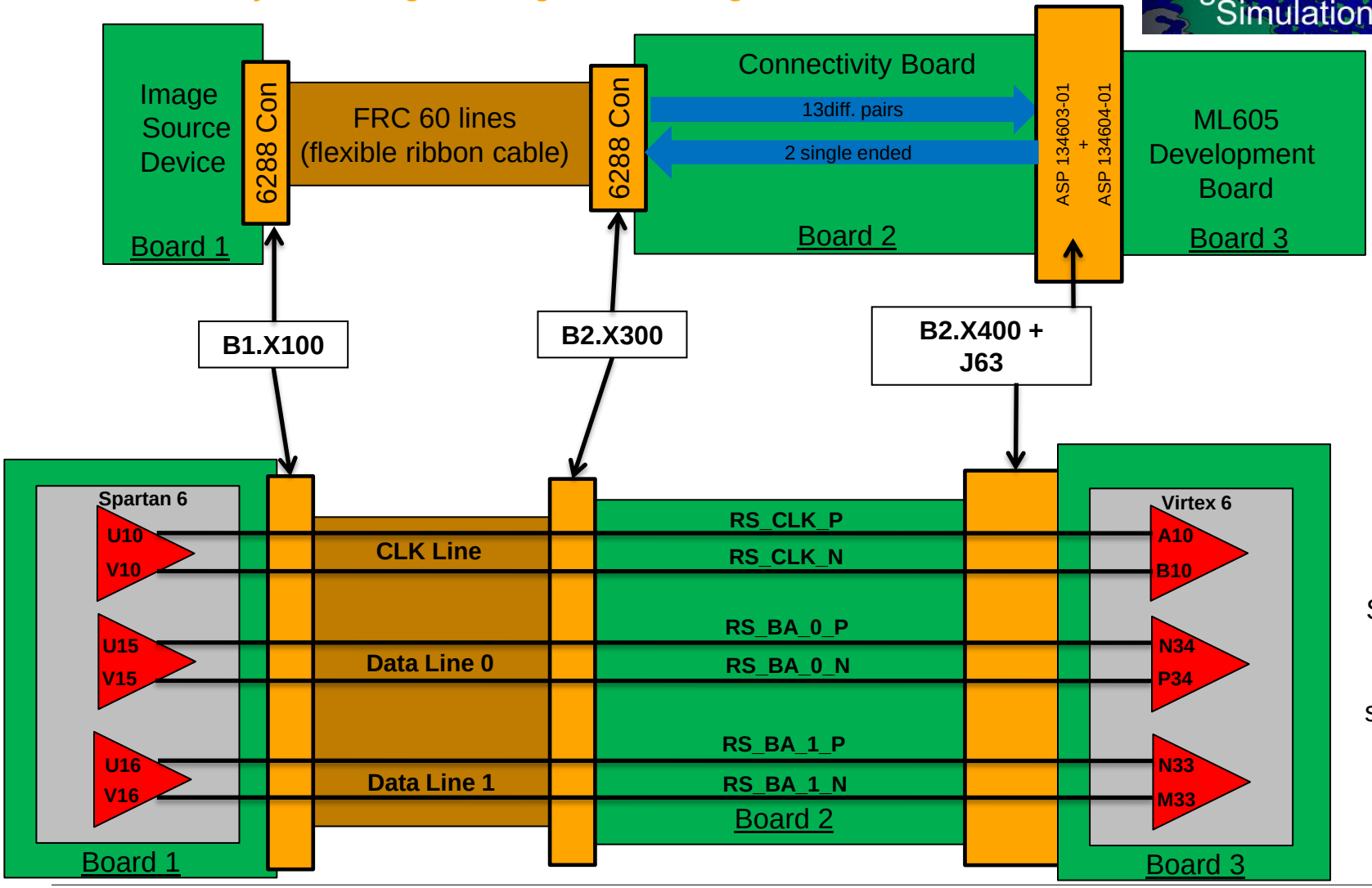


Figure 2

Signals of interest for the simulation

TIE+ Subject
Requirements

Based on the previous system description it is required to analyze signal integrity aspects for the signals RS_CLK_P, RS_CLK_N, RS_BA_P_0, RS_BA_N_0 , RS_BA_P_1, RS_BA_N_0 based on the signal flow diagram from figure 2.

Requirements

A) Define the routing directives for Board 2 PCB specifying: routing layers, routing topology options (microstrip/stripline), differential and common-mode impedance, inter-pair spacing (spacing between the traces of the same pair), trace width.

B) Evaluate the need of series resistors placement on Board 2 for signal integrity improvements (e.g. reflections, crosstalk) .

C) Evaluate VIA propagation delays on Board 2 and establish if there is a need for inter-pair and pair-to-pair VIA number matching.

D) Evaluate pair-to-pair far-end crosstalk at system level. Define a Vp-p crosstalk vs. pair-to-pair spacing chart. Define the minimum acceptable pair-to-pair spacing for Board 2 based on the obtained data.

E) Evaluate the following signal parameters at receiver end (Virtex6 input pins): rise\fall slew rate SE, overshoot & undershoot values SE, high\low time differential.

F) Evaluate the following timing parameters at receiver end (Virtex6 input pins): setup time to CLK (differential); hold time to CLK (differential)

* All simulation data must be provided for MIN (slow), TYP(typical), MAX(fast) IBIS model PVT IBIS corners (assume the logical worst case for the target analysis)

Simulation conditions:

CLK frequency: 125MHz, duty cycle: 50%
Single Data Rate transfer (positive edge)
Unit Interval =1 *CLK period = 8ns

Receiver signal requirements:

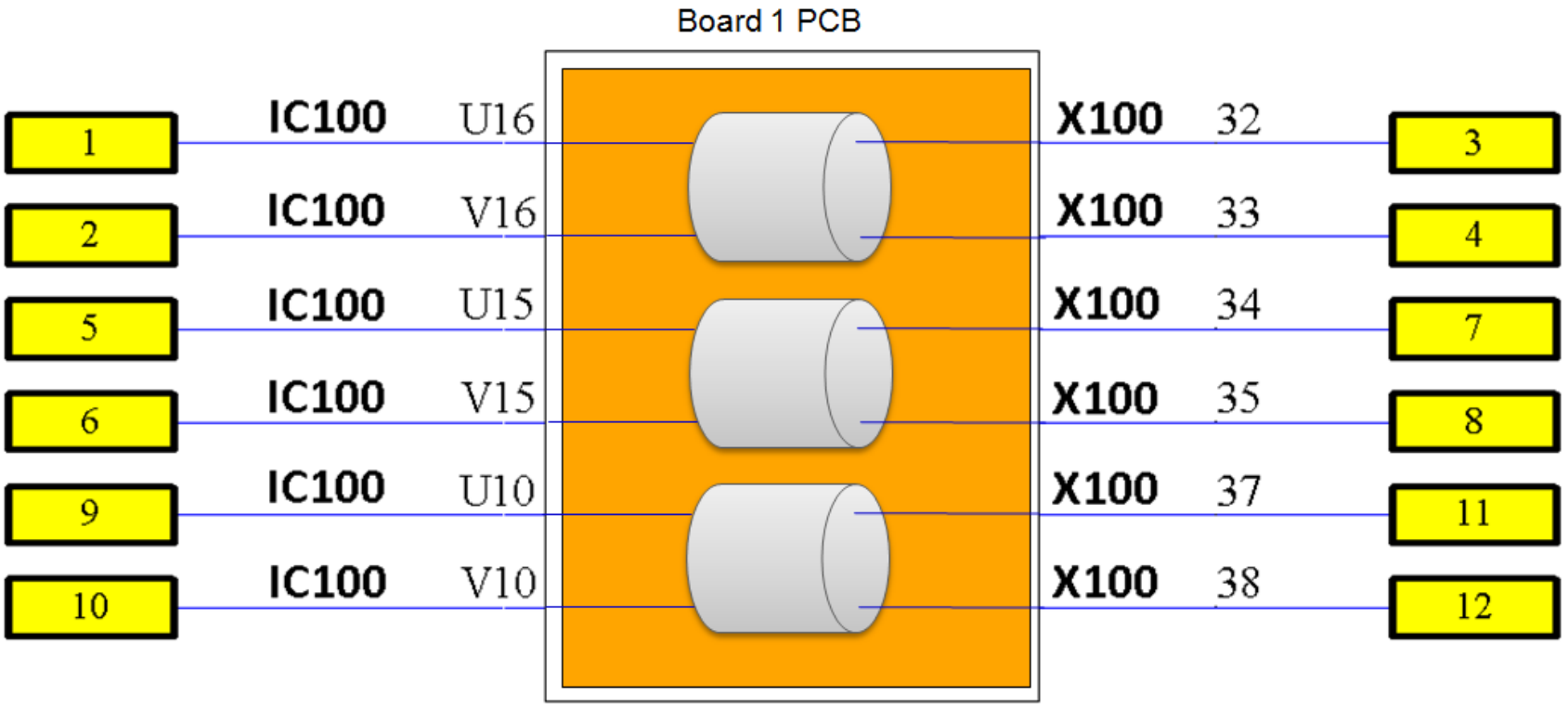
Data-to-CLK max. pair-to-pair skew = +/- 50 ps
Max. inter-pair skew = +/- 10 ps
Max. differential signal crosstalk =10 mVpp
High Input Voltage = +100mV
Low Input Voltage = -100mV

Part information\modeling summary

Part Name \ Reference	Description	Modeling information
Board1 ref: IC100 IC: Spartan 6 FPGA IC code: XC6SLX45 3CSG324	Driver IC	IBIS model: *spartan6.ibs* - use CSG324 package parasitics - use differential pins 743P\743N corresponding to driver model RSDS_25_TB_25
Board 1 PCB	DUT board	The 3 diff pairs are extracted (2D field solver) in Touchstone model : *Board1_sparam_1000pts.s12p*
B1.X100, B2X300	Ribbon connector	Touchstone model for 8 pins: SERIES_6288_8Pin.s16p S-parameter port definition: 6288_sim_model.pdf
Flexible ribbon cable	Length: 60mm	Touchstone model for 8 lines*: FRC_model_log.s16p,* Mechanical drawing: *FRC_data.pdf*
Board 2	PCB under development	4 layer stack-up presented on slide 6 board mechanical drawing is presented *adapter_drawing.pdf*
B2.X400 + J63	Adapter board – ML605 connector pair	HSpice simulation model: *HM_seam035_seaf065.mlm* Mechanical drawing: *ASP-134604-01-mkt.pdf*
Board_3 PCB	ML605 Virtex 6 development board	16 layer stack-up on slide 9 board ODB++: ML605_odb.zip
Board3 ref: U1 IC: Virtex 6 FPGA IC code: XC6SLX45 3CSG324	Receiver IC	IBIS model: *virtex6.ibs* - use FF1156 package parasitics - use differential pins 132P\132N corresponding to driver model LVDS_25

Board 1 (Image Source) Model

S-parameter model port assignment for files
Board1_sparam_10kpts.s12p (10000 frequency points, 10GHz, log distribution)
Board1_sparam_1000pts.s12p (1000 frequency points, 10GHz, log distribution)

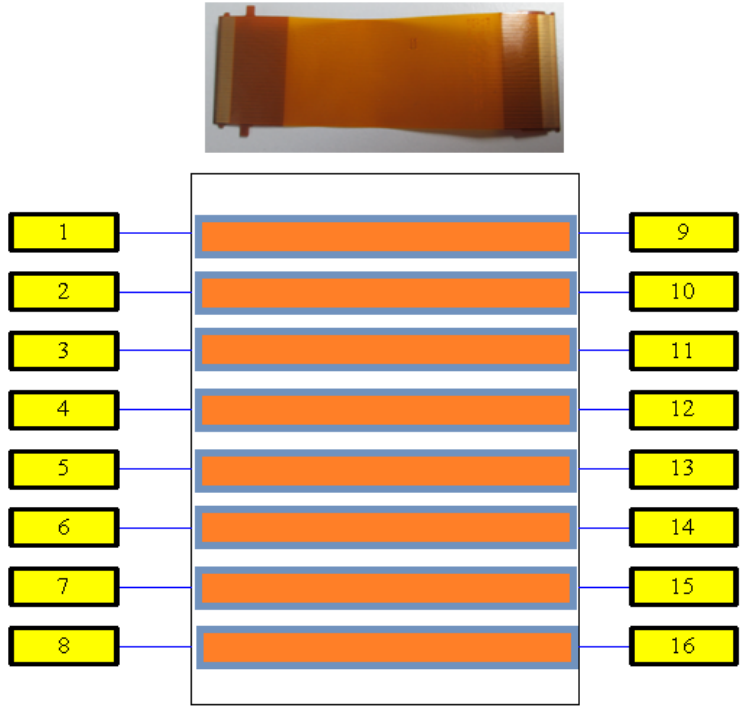


Passivity and causality checked using Hyperlynx Touchstone viewer V2.1; no errors found

Ribbon cable model

S-parameter model port assignment for files
FRC_model_log.s16p (1000 frequency points, 1GHz, log distribution)
FRC_model_lin.s16p (1000 frequency points, 1GHz, linear distribution)

Mechanical dimensions can be found in FRC_data.pdf



Recommendations:
- connect the 2 unused lines to ground

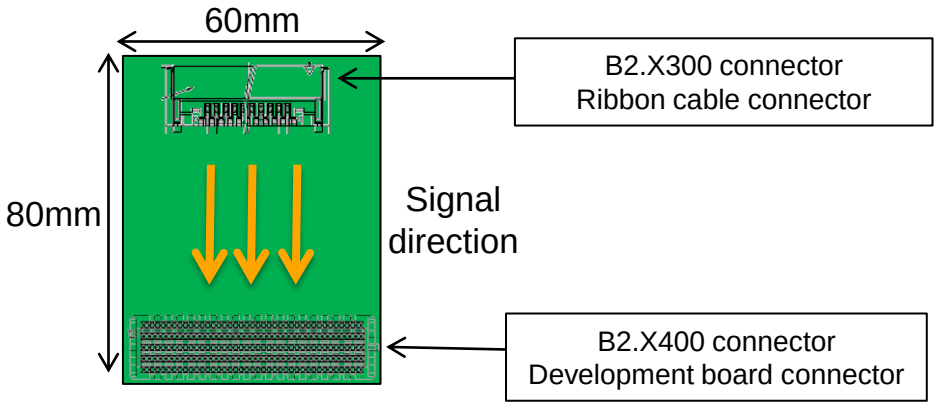
Passivity and causality checked using Hyperlynx Touchstone viewer V2.1; no errors found

Part information\modeling

Stack-up

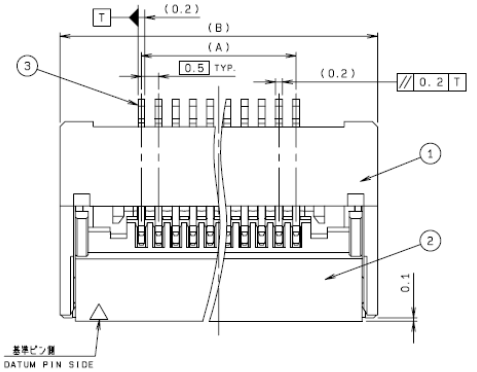
	Dielectric Constant @100MHz	Loss Tangent @100MHz	Thickness [um]	Type
	4.6	0.02	25	Solder Mask
1			60	Copper (35 base + 25 plating)
	4.1	0.011	100	2116 Prepreg
2			18	Copper
	4.5	0.013	1200	CORE
3			18	Copper
	4.1	0.011	100	2116 Prepreg
4			60	Copper (35 base + 25 plating)
	4.6	0.02	25	Solder Mask
		Total thickness	1606	

Layout & Dimensions

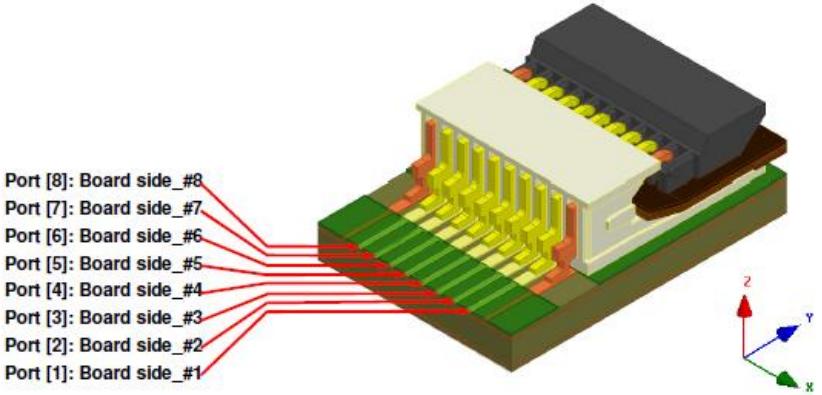


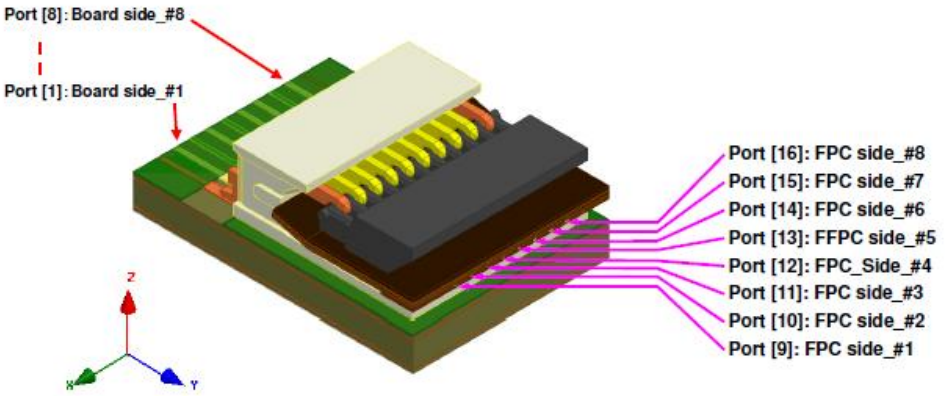
B1.X100, B2.X300
Ribbon cable connector

› Kyocera 6288 FPC connector / 60 pin format



› Touchstone model provided in file SERIES_6288_8Pin.s16p for a reduced 8 pin model; port assignments is presented below

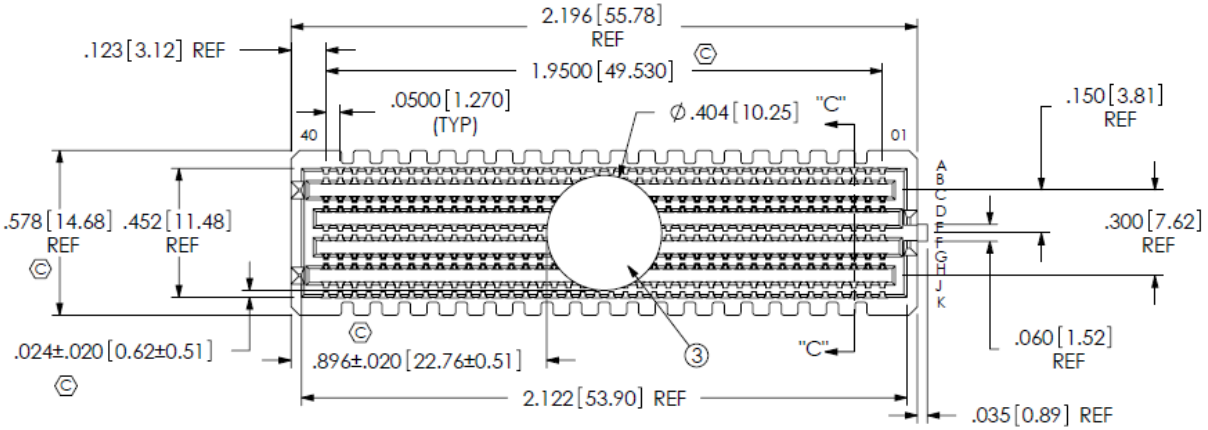




Passivity and causality checked using Hyperlynx Touchstone viewer V2.1; ignore minor causality violations

B2.X400, J63 (ML605 Board)
BGA development board connector

› Samtec ASP-134604-01



› H-Spice model provided in file HM_seam035_seaf065.mlm (model valid up to 7GHz)

› Port assignment:
RS_CLK_N =>1505(B2.X400)->12505(J63) ; RS_CLK_P =>1506(B2.X400)->12506(J63) ;
RS_BA_P_0 =>1401(B2.X400)->12401(J63); RS_BA_N =>1402(B2.X400)->12402(J63);
RS_BA_1_P =>1502(B2.X400)->12502(J63); RS_BA_1_N=>1503(B2.X400)->12503(J63);

› Hint: in order to reduce simulation times insert the Samtec connector model only for system level simulations; due to the model complexity this significantly increases the simulation time but the influence on signal integrity is low

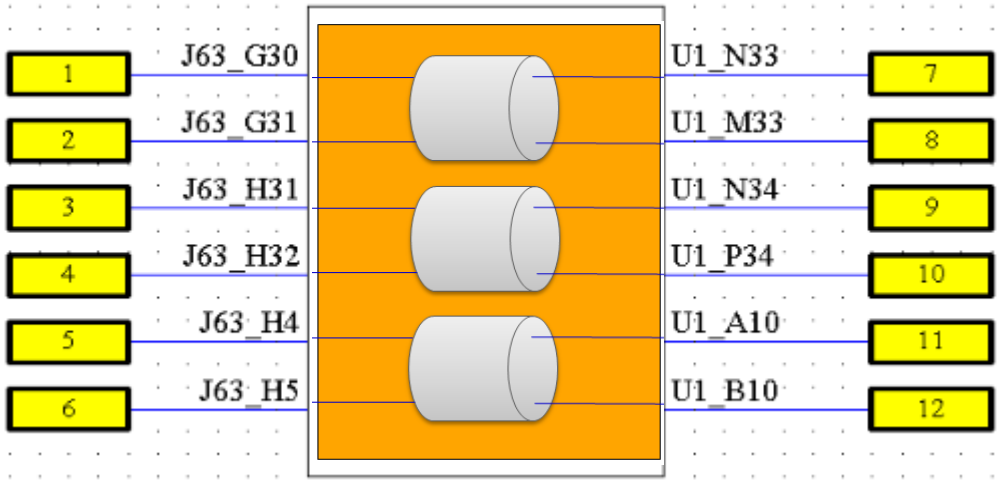
ML605 Board
Virtex6 development board

- The CAD is contained in the file ML605_odb.tgz
- The stack-up information is presented below (all thickness dimensions in mm)

ML605 Board stack-up (16 layers)

Layer Name	Type	Number	Material	Thickness	Permittivity	Loss Angle ...	Fill
SMT	Dielectric	-	FR4	0.0254	4.3	0.02	-
TOP	Signal	1	Copper	0.0508	-	-	Above
SUBSTRATE-1	Dielectric	-	FR4-4.5	0.0762	4.5	0.017	-
02_GND1	Signal	2	Copper	0.01524	-	-	Above
SUBSTRATE-2	Dielectric	-	FR4-4.5	0.0889	4.5	0.017	-
03_SIG1	Signal	3	Copper	0.01524	-	-	Below
SUBSTRATE-3	Dielectric	-	FR4-4.5	0.08636	4.5	0.017	-
04_GND2	Signal	4	Copper	0.01524	-	-	Above
SUBSTRATE-4	Dielectric	-	FR4-4.5	0.0889	4.5	0.017	-
05_SIG2	Signal	5	Copper	0.01524	-	-	Below
SUBSTRATE-5	Dielectric	-	FR4-4.5	0.08636	4.5	0.017	-
06_GND3	Signal	6	Copper	0.01524	-	-	Above
SUBSTRATE-6	Dielectric	-	FR4-4.5	0.0889	4.5	0.017	-
07_SIG3	Signal	7	Copper	0.01524	-	-	Below
SUBSTRATE-7	Dielectric	-	FR4-4.5	0.08636	4.5	0.017	-
08_GND4	Signal	8	Copper	0.01524	-	-	Above
SUBSTRATE-8	Dielectric	-	FR4-4.5	0.0762	4.5	0.017	-
09_PWR1	Signal	9	Copper	0.03048	-	-	Below
SUBSTRATE-9	Dielectric	-	FR4-4.5	0.09144	4.5	0.017	-
10_PWR2	Signal	10	Copper	0.03048	-	-	Above
SUBSTRATE...	Dielectric	-	FR4-4.5	0.0762	4.5	0.017	-
11_GND5	Signal	11	Copper	0.01524	-	-	Below
SUBSTRATE...	Dielectric	-	FR4-4.5	0.08636	4.5	0.017	-
12_SIG4	Signal	12	Copper	0.01524	-	-	Above
SUBSTRATE...	Dielectric	-	FR4-4.5	0.0889	4.5	0.017	-
13_GND6	Signal	13	Copper	0.01524	-	-	Below
SUBSTRATE...	Dielectric	-	FR4-4.5	0.08636	4.5	0.017	-
14_SIG5	Signal	14	Copper	0.01524	-	-	Above
SUBSTRATE...	Dielectric	-	FR4-4.5	0.0889	4.5	0.017	-
15_GND7	Signal	15	Copper	0.01524	-	-	Below
SUBSTRATE...	Dielectric	-	FR4-4.5	0.0762	4.5	0.017	-
BOTTOM	Signal	16	Copper	0.0508	-	-	Below
SMB	Dielectric	-	FR4	0.0254	4.3	0.02	-

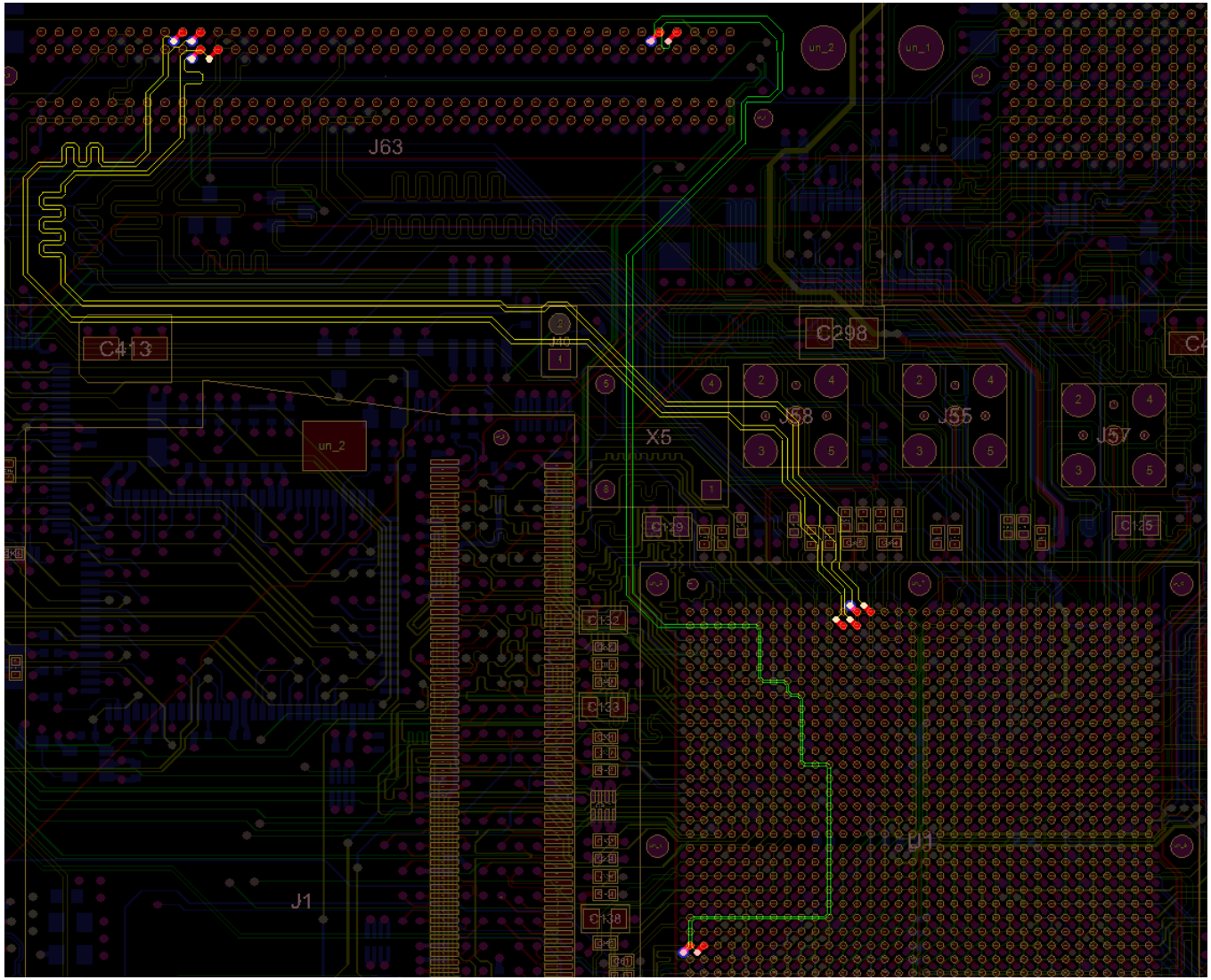
ODB++ Net names for extraction:
FMC_LPC_CLK0_M2C_P, FMC_LPC_CLK0_M2C_N – CLK Line
FMC_LPC_LA28_P, FMC_LPC_LA28_N – Data 1 line
FMC_LPC_LA29_P, FMC_LPC_LA29_N – Data 0 line



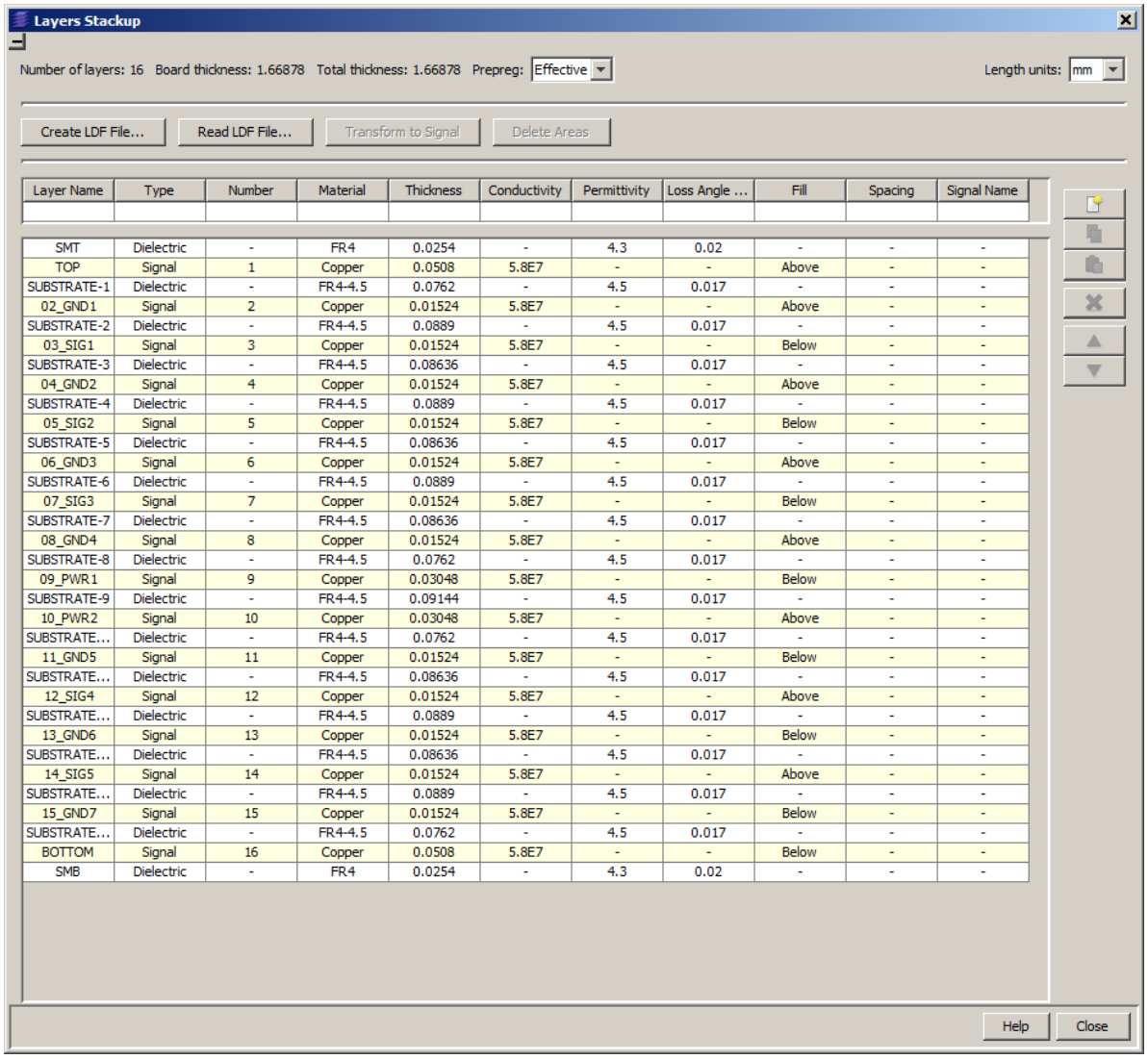
Example of equivalent circuit model obtained after extraction

* J63 connector pins and U1 (Virtex6) pins are indicated
* the presented port assignment is not mandatory

ML605 Board Nets

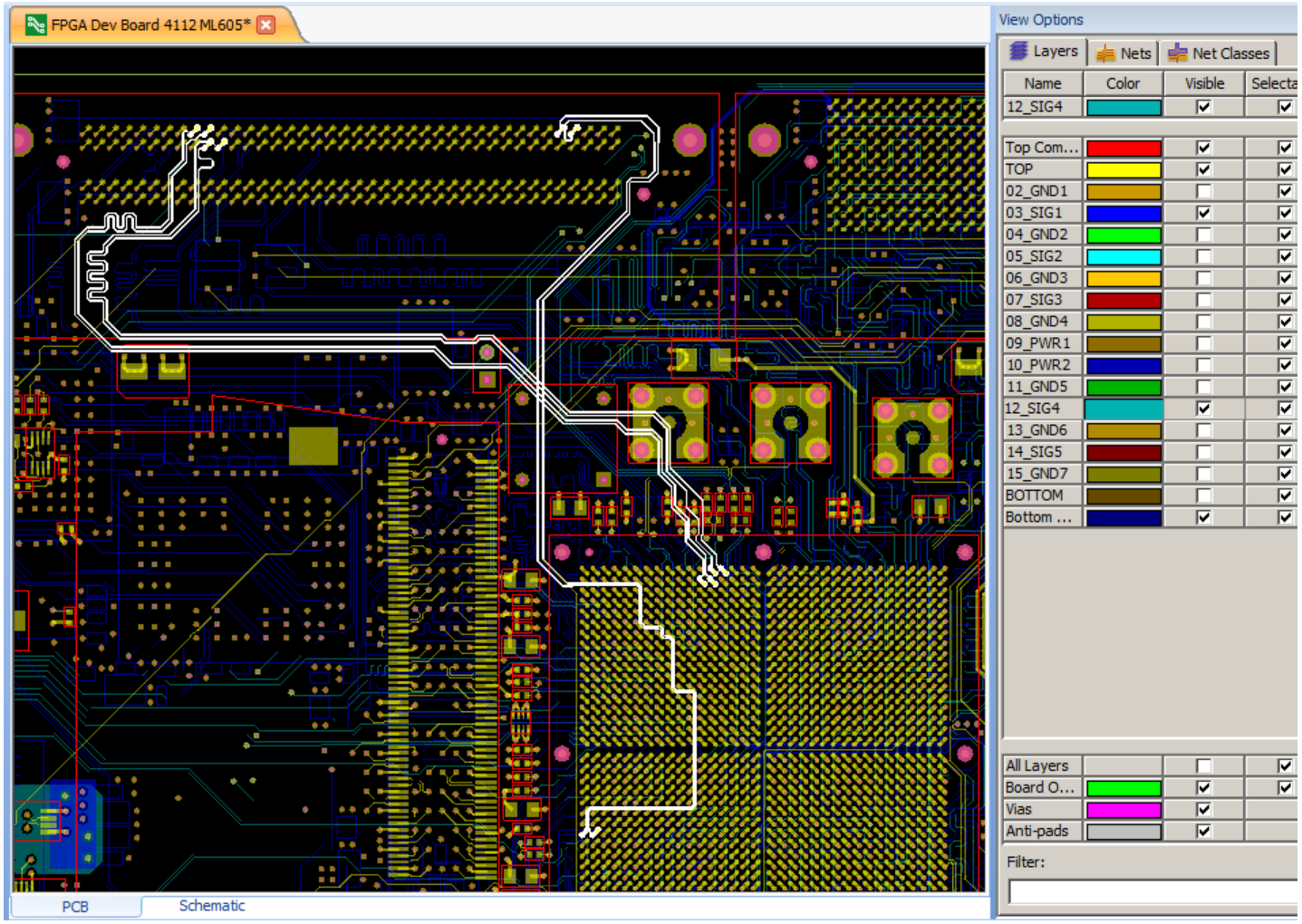


CST Modeling

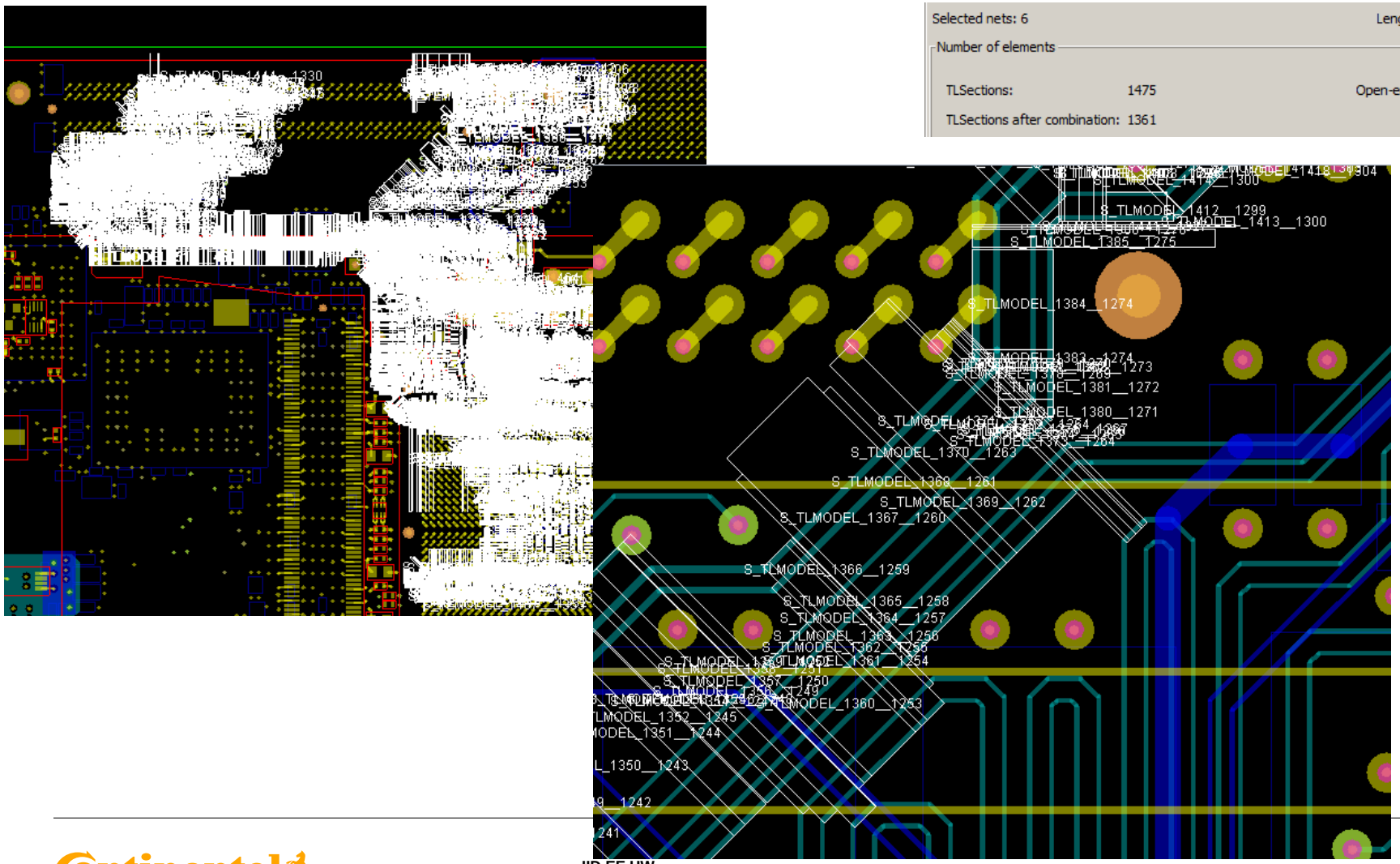


Layer Name	Type	Number	Material	Thickness	Conductivity	Permittivity	Loss Angle ...	Fill	Spacing	Signal Name
SMT	Dielectric	-	FR4	0.0254	-	4.3	0.02	-	-	-
TOP	Signal	1	Copper	0.0508	5.8E7	-	-	Above	-	-
SUBSTRATE-1	Dielectric	-	FR4-4.5	0.0762	-	4.5	0.017	-	-	-
02_GND1	Signal	2	Copper	0.01524	5.8E7	-	-	Above	-	-
SUBSTRATE-2	Dielectric	-	FR4-4.5	0.0889	-	4.5	0.017	-	-	-
03_SIG1	Signal	3	Copper	0.01524	5.8E7	-	-	Below	-	-
SUBSTRATE-3	Dielectric	-	FR4-4.5	0.08636	-	4.5	0.017	-	-	-
04_GND2	Signal	4	Copper	0.01524	5.8E7	-	-	Above	-	-
SUBSTRATE-4	Dielectric	-	FR4-4.5	0.0889	-	4.5	0.017	-	-	-
05_SIG2	Signal	5	Copper	0.01524	5.8E7	-	-	Below	-	-
SUBSTRATE-5	Dielectric	-	FR4-4.5	0.08636	-	4.5	0.017	-	-	-
06_GND3	Signal	6	Copper	0.01524	5.8E7	-	-	Above	-	-
SUBSTRATE-6	Dielectric	-	FR4-4.5	0.0889	-	4.5	0.017	-	-	-
07_SIG3	Signal	7	Copper	0.01524	5.8E7	-	-	Below	-	-
SUBSTRATE-7	Dielectric	-	FR4-4.5	0.08636	-	4.5	0.017	-	-	-
08_GND4	Signal	8	Copper	0.01524	5.8E7	-	-	Above	-	-
SUBSTRATE-8	Dielectric	-	FR4-4.5	0.0762	-	4.5	0.017	-	-	-
09_PWR1	Signal	9	Copper	0.03048	5.8E7	-	-	Below	-	-
SUBSTRATE-9	Dielectric	-	FR4-4.5	0.09144	-	4.5	0.017	-	-	-
10_PWR2	Signal	10	Copper	0.03048	5.8E7	-	-	Above	-	-
SUBSTRATE...	Dielectric	-	FR4-4.5	0.0762	-	4.5	0.017	-	-	-
11_GND5	Signal	11	Copper	0.01524	5.8E7	-	-	Below	-	-
SUBSTRATE...	Dielectric	-	FR4-4.5	0.08636	-	4.5	0.017	-	-	-
12_SIG4	Signal	12	Copper	0.01524	5.8E7	-	-	Above	-	-
SUBSTRATE...	Dielectric	-	FR4-4.5	0.0889	-	4.5	0.017	-	-	-
13_GND6	Signal	13	Copper	0.01524	5.8E7	-	-	Below	-	-
SUBSTRATE...	Dielectric	-	FR4-4.5	0.08636	-	4.5	0.017	-	-	-
14_SIG5	Signal	14	Copper	0.01524	5.8E7	-	-	Above	-	-
SUBSTRATE...	Dielectric	-	FR4-4.5	0.0889	-	4.5	0.017	-	-	-
15_GND7	Signal	15	Copper	0.01524	5.8E7	-	-	Below	-	-
SUBSTRATE...	Dielectric	-	FR4-4.5	0.0762	-	4.5	0.017	-	-	-
BOTTOM	Signal	16	Copper	0.0508	5.8E7	-	-	Below	-	-
SMB	Dielectric	-	FR4	0.0254	-	4.3	0.02	-	-	-

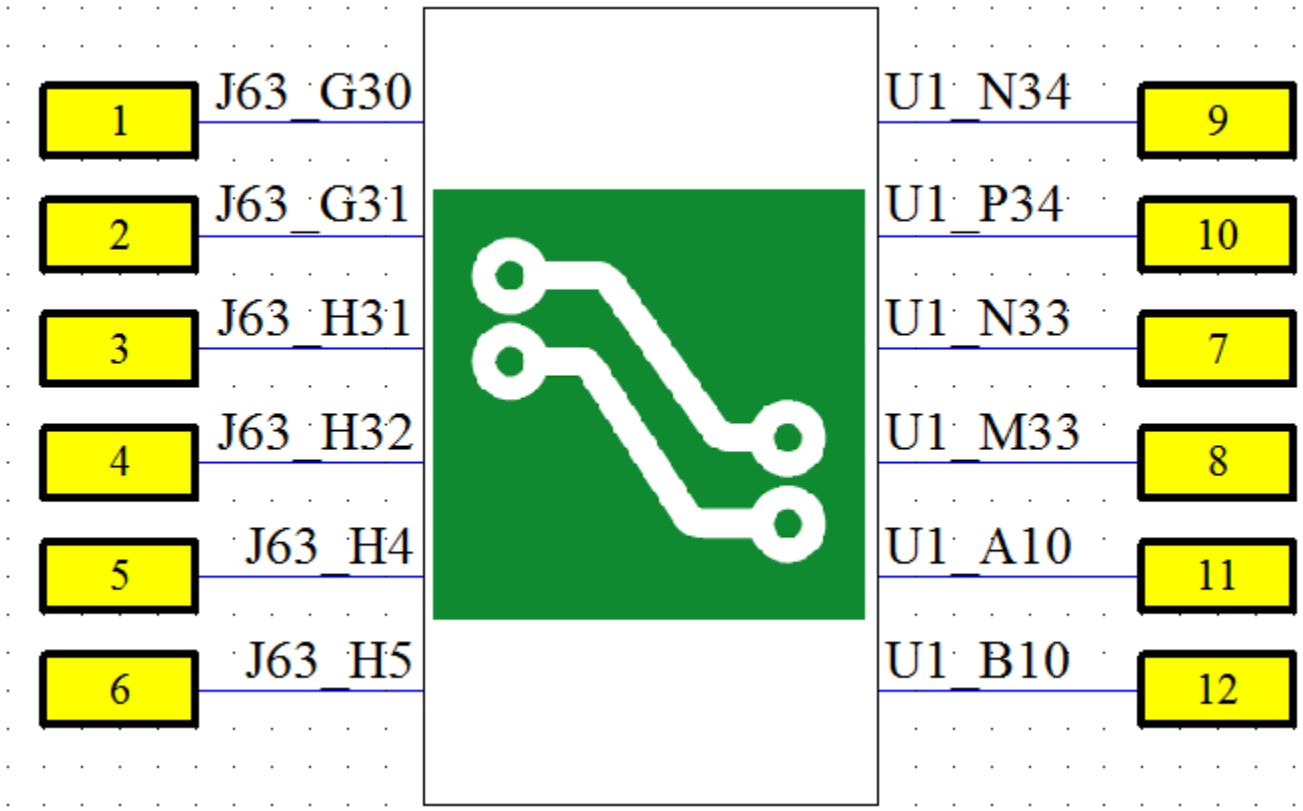
CST Modeling



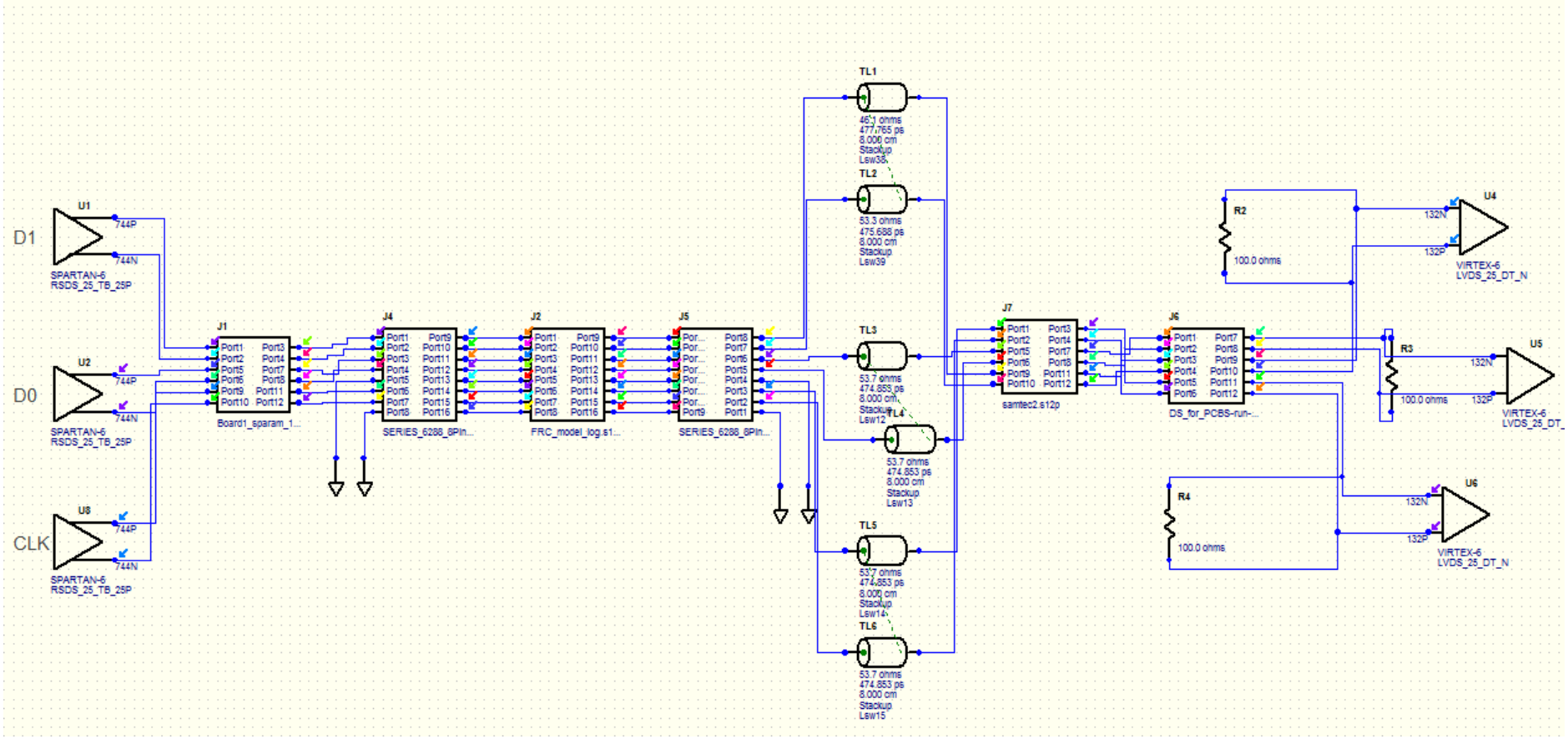
Meshing


Selected nets: 6
Length units: mm
Number of elements
TLSections: 1475
Open-ended terminals: 60
TLSections after combination: 1361
S_TLMODEL_1384__1274
S_TLMODEL_1381__1272
S_TLMODEL_1380__1271
S_TLMODEL_1370__1263
S_TLMODEL_1368__1261
S_TLMODEL_1369__1262
S_TLMODEL_1367__1260
S_TLMODEL_1366__1259
S_TLMODEL_1365__1258
S_TLMODEL_1364__1257
S_TLMODEL_1360__1253

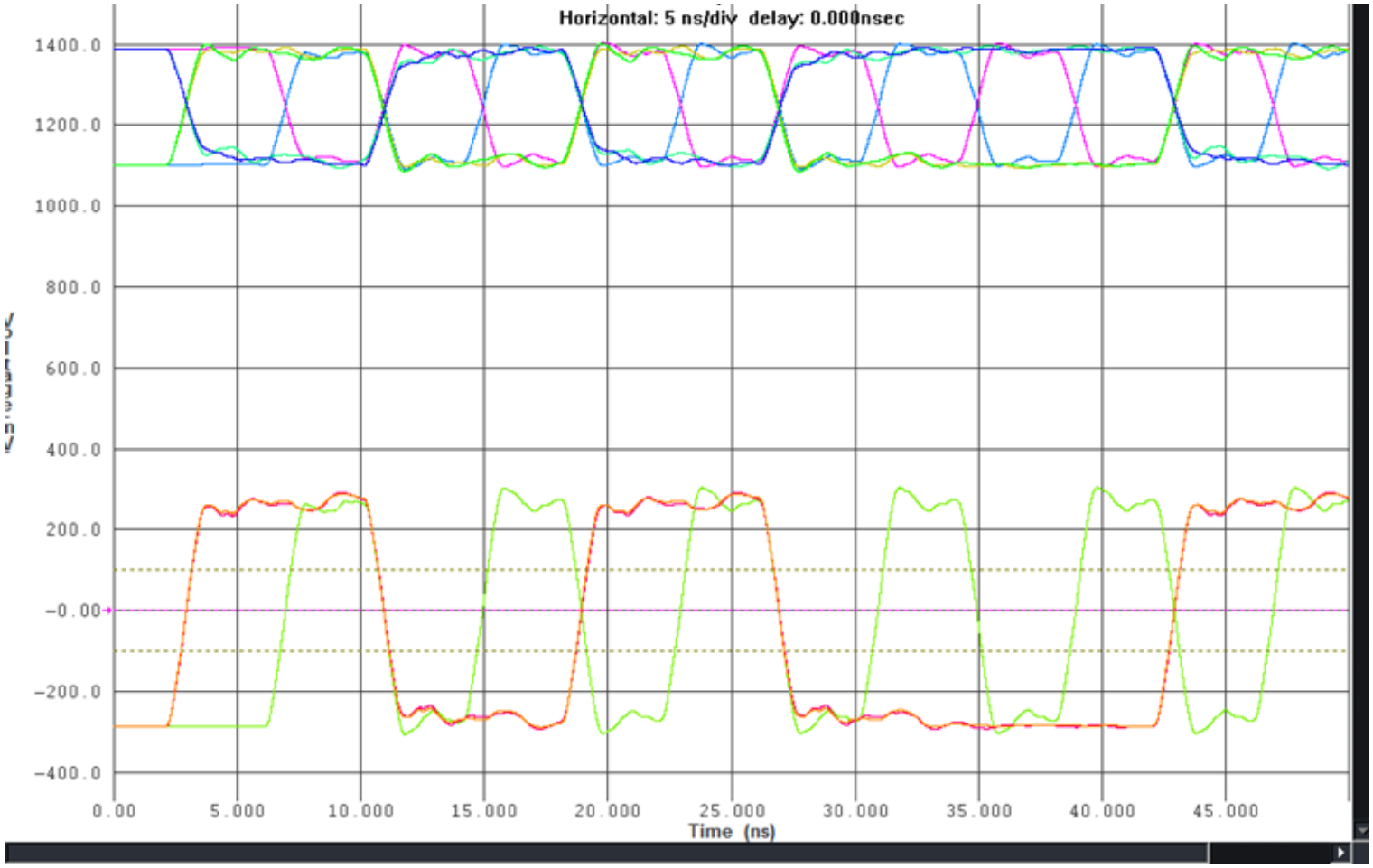
….. some hours later



Full Hyperlynx system schematic



A first look at the signals in TYP



Next TIEplus edition

TIE Plus workflow

- **Publication of subject**
  - The subject content will published on the TIE website in a separate form “TIE Plus”. Also contest topics, recommended bibliography and contest regulations will be available.
  - At this stage only the subject text and block diagrams will be public. The simulation models, datasheets and other details will be available for download only after the contestant is registered.
- **Contestant registration**
  - The registration will be done using an on-line application form. The provided information will be analyzed by the technical committee and a notification email will be sent to the applicant (accepted \ rejected as a contestant for TIE Plus). After acceptance the contestant will receive user login information on the TIE plus platform. Based on this he will be able to download all necessary files associated with the subject.
- **Solving the subject**
  - Solving the subjects will be done by own\university\supported technical means (hardware and software).
  - The technical solution will be posed as R&D report document that shall be uploaded on the web platform.
- **Assessment of the solutions**
  - The contestants are required to prepare a short presentation (15-20 min.) that will be exposed to the technical committee during an evaluation meeting. The presentation content must be in full agreement with the uploaded R&D report.

Timeline and place for solution assessment are not fixed, but will be announced prior to registration.
Keep an eye on the www.tie.ro for upcoming news on TIE PLUS.

TIE Plus topics

- Transmission line theory.
  - Line impedance.
  - Propagation delay.
  - Reflections
- Single ended and differential data transmissions
  - Terminations
  - Eye diagrams
  - Routing topologies
- Crosstalk
  - Coupling mechanisms
  - Near-End and Far-End crosstalk
  - Crosstalk induced ISI
- IC modeling for SI simulations
  - IBIS Modeling
  - I\O buffer impedance analysis
  - Package parasitics modeling
- Passive components & interconnect modeling
  - S-parameters
  - Touchstone modeling
  - Capacitor model
  - Via hole modeling
  - 2D\3D Field solver extraction
- PCB Stack-up definition
- Timing analysis
  - Interface budget planning
  - Interconnect propagation delays
  - Jitter characterization
- Signal Integrity simulation
- Power Integrity simulation

TIE Plus recommended bibliography

- *Signal Integrity Issues and Printed Circuit Board Design*, Douglas Brooks, Prentice Hall PTR
- *High-Speed Digital Design "A handbook of Black Magic"*, H. W. Johnson, Prentice Hall PTR
- *High-Speed Circuit Board Signal Integrity*, Stephen C. Thierauf, Artech House
- *Advanced Signal Integrity for High-Speed Digital Designs*, Stephen Hall, Howard Heck, IEEE-Wiley, 2009.
- *Frequency Domain Characterization of Power Distribution Networks*, Istvan Novak, Jason R. Miller, Artech House, Boston, 2007.
- *Signal Integrity – Simplified*, Eric Bogatin, Prentice Hall, New Jersey, 2004.
- *Signal Integrity Characterization Techniques*, Mike Resso, Eric Bogatin, IEC, 2009.
- *Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages*, Brian Young, Prentice Hall, 2000.
- *Timing Analysis and Simulation for Signal Integrity Engineers*, Greg Edlund, Prentice Hall, 2007.

START HERE !

TIE Plus evaluation criteria

› Modeling approach (using the right field solver for a specific problem)

› Modeling fidelity (how close does the simulation model gets to the physical system)

› Exposure of numerical results (e.g. variation timing parameters vs. trace length)

› Correctness of simulation problem formulation (transposing interface requirements and datasheet information in to a simulatable system)

› Formulation and argumentation of layout directives (clarity of directives; applicability in to a real design)

› Applicability of the provided solution to a PCB (complies with generic IPC and is implementable using conventional fabrication processes)

Continental
The Future in Motion

Thank you for your attention.

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