An Overview of Electronic Manufacturing Technology Evolution and Trends

Joseph Fjelstad
Verdant Electronics

A Brief History of PWBs

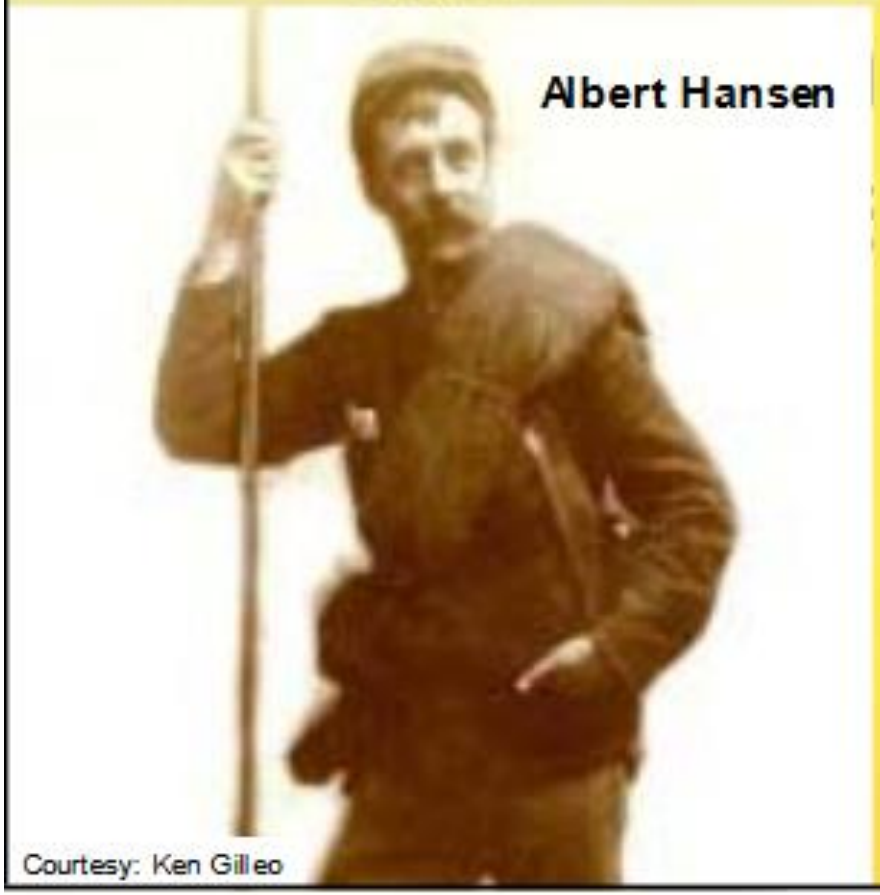
- 1903 Flattened Wires on Paraffin Paper
  - Albert Hansen of Berlin, Germany
- 1904 - Conductors on Dielectrics
  - Thomas Edison & Frank Sprague
- 1913 – Print and Etch Heater Circuit
  - Arthur Berry

N° 4681 A.D. 1903

Date of Application, 27th Feb., 1903
Complete Specification Left, 23th Dec., 1903—Accepted, 27th May, 1904

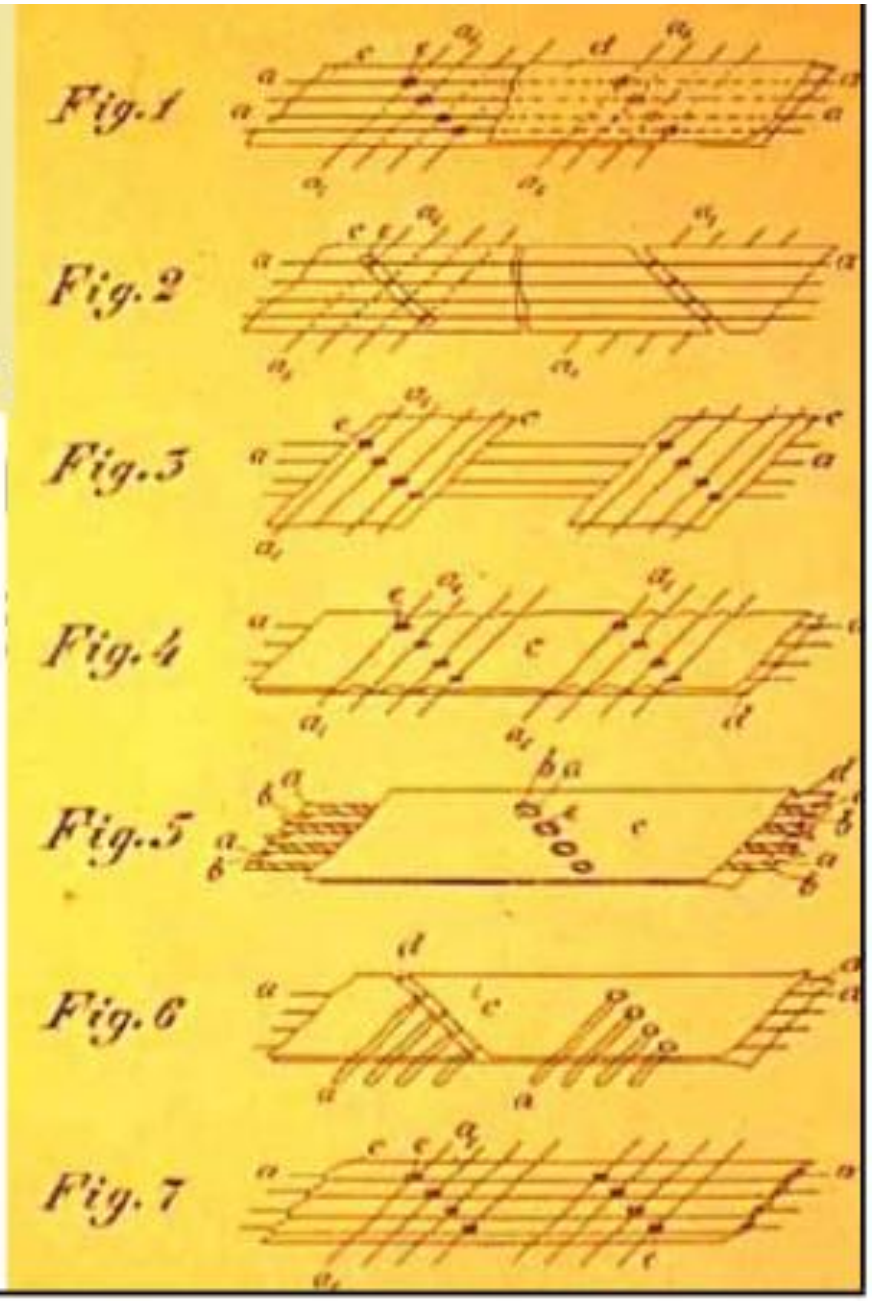
PROVISIONAL SPECIFICATION.

Improvements in or connected with Electric Cables and the Jointing of the same.

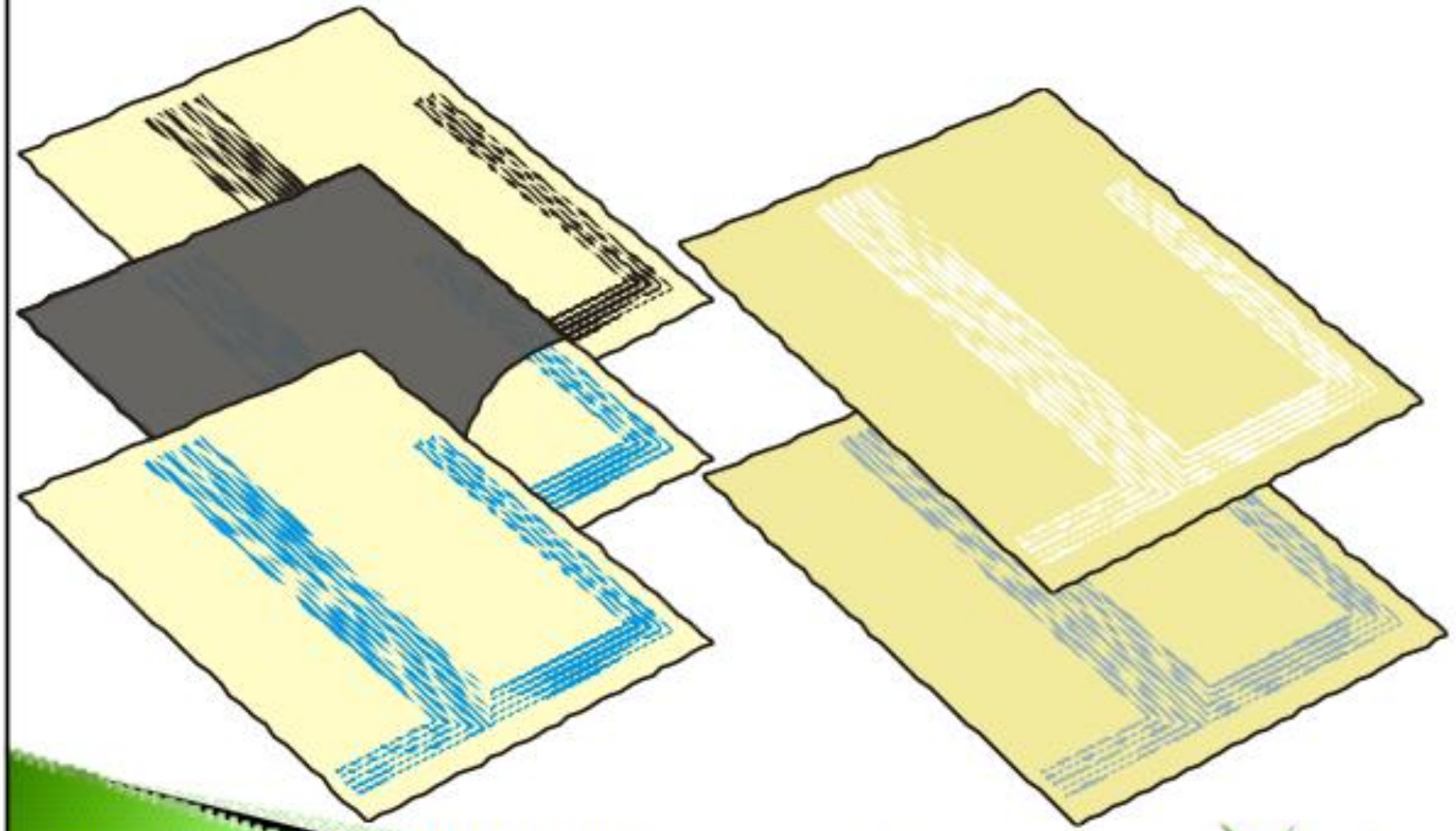


Albert Hansen

Courtesy: Ken Gilleo



Thomas Edison, USA – 1904

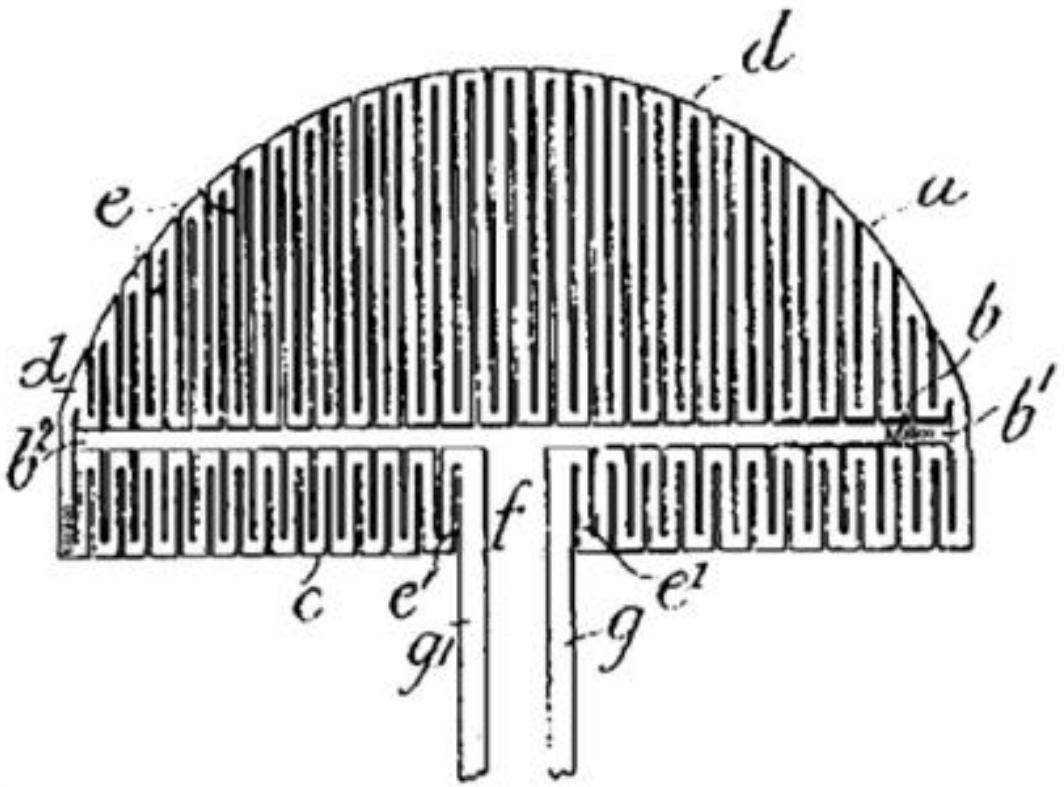


Printed adhesive carbon dust process

Patterned silver reduction process

Verdant ELECTRONICS

Arthur Berry, UK 1913



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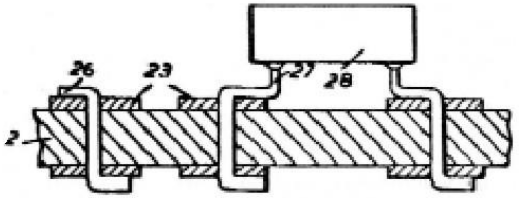
- 1925 - Transfer Plated Conductor
  - Charles Ducas
- 1936 - The Print and Etch Circuit

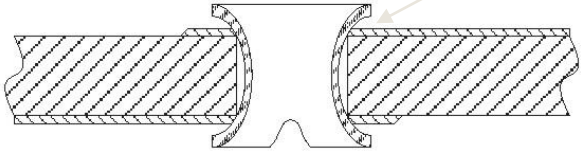
  Paul Eisler
- 1940's - Mass Production
  - US Army
- 1950's - The Plated Through Hole
  - Hughes, Photocircuits, Shipley

PTH Evolution

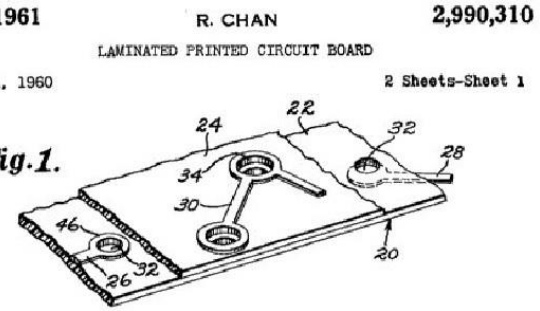
Z wire

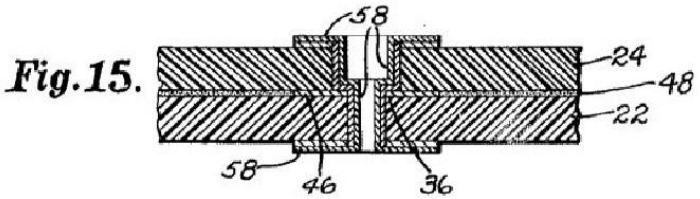


Eyelet

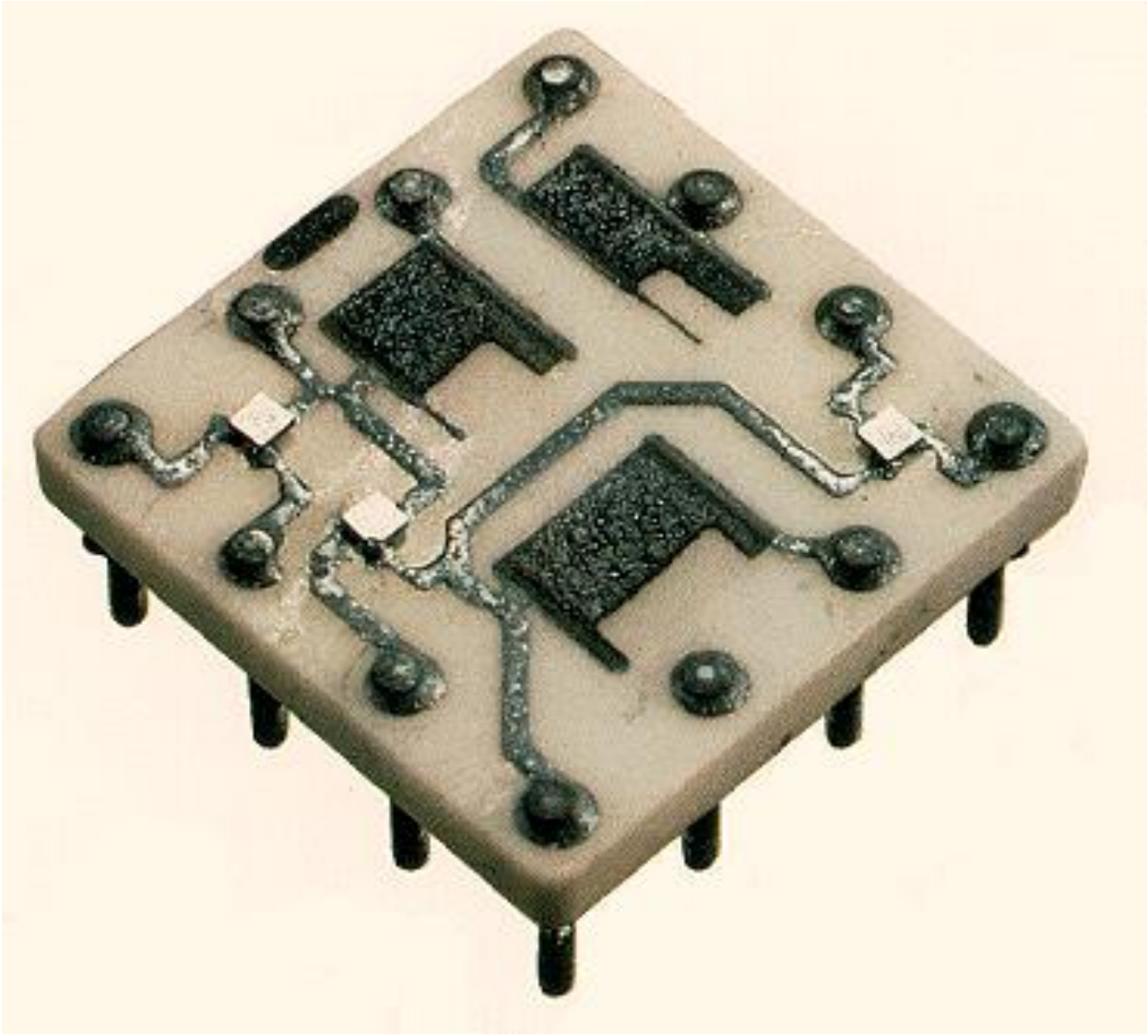


MLB PTH





Ceramic (Hybrid) Printed Circuit



courtesy IBM

A Brief History of PWBs

- 1956 - The Multilayer PCB
  - Tally and Dahlgren, Sanders Associates
- 1961 - The Plated Through Multilayer
  - Richard Chan, Burroughs
- 1970's - The Rigid Flex Board
  - Sanders Associates, Hughes, Lockheed, GD
- 1970's-80's - Chip On Board

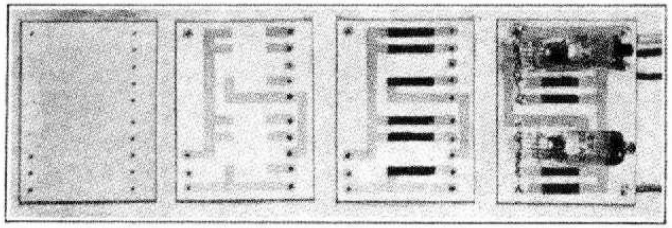
  Several different companies
- 1990's - MCM-L and Chip Scale Modules
  - MCM-L (High Density COB)- Numerous companies
  - Grid based substrates - 3M, Sheldahl, Tessera
- **2000s** – Chip and Wafer Stacking, TSV technologies

Early PCB Advertisements 1940's

1946

WIRING . . Printed electric circuits for instruments, electronic equipment

Source: CENTRALAB DIV., GLOBE-UNION INC. 902 E. Keefe Ave., Milwaukee 12, Wis.



The company announces availability for civilian use of a method developed during the war by which electric circuits and certain circuit components are printed upon steatite ceramic plates as a means of conserving space requirements and simplifying the wiring problem. The company is prepared to supply the plates with specified circuits and components for built-in replaceable application in instruments and electronic equipment in quantity production.

The wiring is produced by application of a silver paste which is printed or stenciled on the steatite and then is fired to bond it permanently. Resistor material composed of a carbon and resin mixture is sprayed or screened to form integral parts of the circuit as required. Small paper-thin, ceramic-disc capacitors are soldered directly to specified silver leads. Sub-miniature electronic tubes are similarly assembled by soldering. Wire leads are brought through holes from the back of the plate to be soldered at the terminals of the printed silver.

The illustration shows the new product in the steps which make up the process starting with the steatite plate which is fired in equipment the company has installed for this purpose. The fired plate is printed and again fired to set the silver leads as shown next toward the right. The resistor material is added and fixed. It shows as black sections of the silver circuits. Finally the components are soldered in position as shown at the right.

1948

ELIMINATE WIRES

through use of

DU PONT CONDUCTIVE COATINGS

Easily and rapidly applied by spray, brush, dip, stencil to metals and non-conductors, they give a conductive surface of low resistance. One troy ounce covers about 3 sq. ft. Use them in printed circuits for radios, amplifiers, switchboards, meters; for capacitors and couplings; for static shielding to replace foils and cans; for resistors and solder seals. Save hours of time, $$$$ of cost! For more information, send for Bulletin CP-2-1247. E. I. du Pont de Nemours & Co. (Inc.), Electrochemicals Dept., Wilmington 98, Delaware.

DU PONT ELECTROCHEMICALS

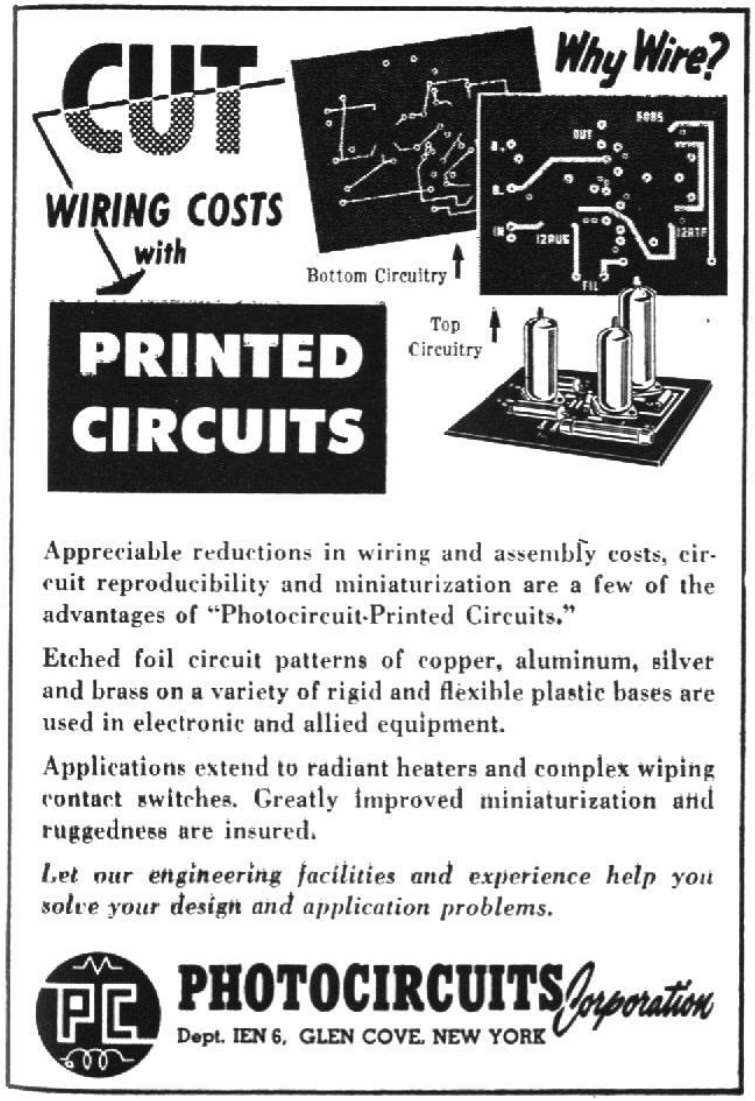
DU PONT

REG. U.S. PAT. OFF.

BETTER THINGS FOR BETTER LIVING . . . *THROUGH CHEMISTRY*

Early PCB Advertisements 1950's

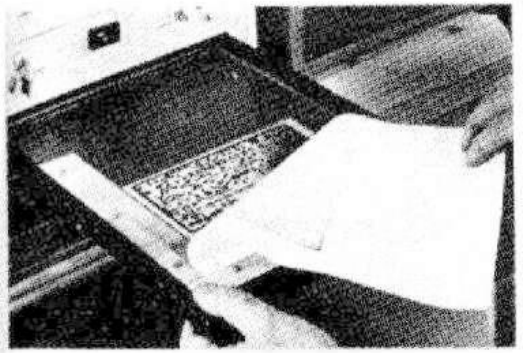
1951



1956

Electrostatic printing equipment prepares printed circuit to etch

HALOID COMPANY
2-20 Haloid St., Dept. IEN, Rochester 3, N. Y.



Copper-clad plastic laminates can be prepared with the aid of XeroX equipment for printed electrical circuit production by etching in a new set-up of this equipment. The powder image, that characterizes xerography, is transferred from a XeroX selenium plate to a sheet of transfer paper and from there to the face of a copper-clad laminate sheet.

The powder forms a photo-exact resist pattern that is not subject to chemical attack. Acid eats away the copper that is not protected by the resist so the only metal left is that of the original circuit drawing. The xerographic powder is then removed by a solvent and the completed circuit print is ready for processing.

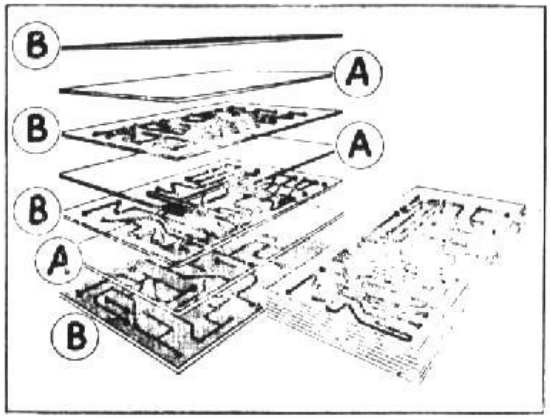
A laminate can be prepared for etching, in about 10 min., from the original opaque drawing or about nine times faster than that of the usual photo-resist method and about 14 times faster than by silk screen. The operation is dry except for the final etching. Size limit, that can be put through the equipment, is 8½ by 13 inches.

Early PCB Advertisements 1960's

1962

PRINTED CIRCUIT LAMINATE

dry-bonded, from 3 to 8 circuits



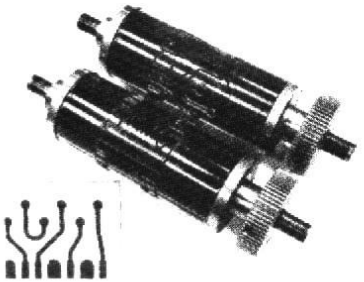
Individual etched circuits are laminated together to form a multi-layer circuit system. Each circuit is etched on a copper-clad epoxy-glass sheet. Base material can be etched on one or two sides. Thickness is 0.003 to 1 inch. Laminate layers are bonded together by an epoxy-resin-impregnated woven glass-fiber cloth. No solvent or wet bonding agents are used. New Dri-Pli circuits provide a system for module interconnection. Plated through-hole and clearance-hole circuits can be produced.

Source: New England Laminate Company
481 Canal St., Dept. IEN, Stamford, Conn.

1966

ELECTRIC CIRCUIT

die-cut at 72,000 per hour rate



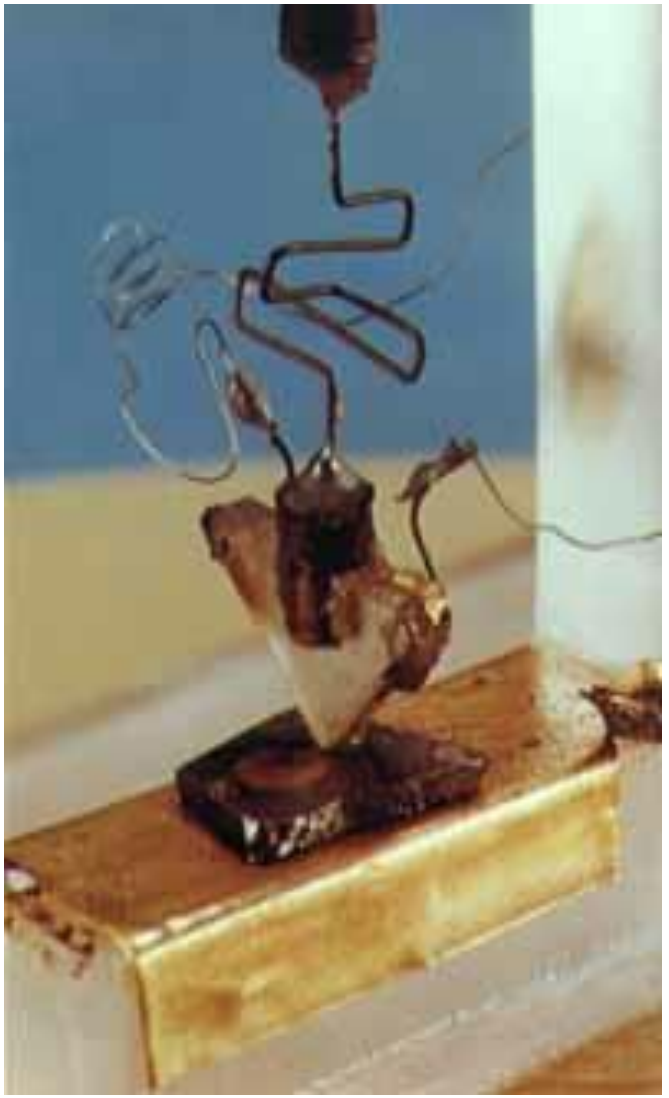
Continuous production of a printed circuit is done in a rotary die-cutting press. It utilizes stripping and rewind stations for rolls of circuits or stripping and cut-off stations for sheets. Lamination or heat-sealing also is employed. New Mactac process is quick, dry and clean. Circuit configurations include crossover or layered. Stripped copper is reclaimed completely. Accuracy is inherent.

Patented fabrication method starts with copper foil adhered to a DuPont Mylar release backing. Rotary dies contact this plastic film, severing the desired printed circuit sections and stripping excess metal foil from the backing. One die provides about 20 million cuts. Printed-circuit portions retain their position on the backing sheet. A second Mylar insulating sheet (blue), also die-cut, is parted from its backing paper and superimposed in register over the metal circuit. Finished product thus is a die-cut flexible printed circuit sandwiched between Mylar sheets. The backing may be removed leaving an adhesive layer which can be pressed against a carrier board or panel. Need for fasteners is thereby eliminated. Circuitry is protected by the top insulating sheet and bottom adhesive layer.

Source: Morgan Adhesives Company
4560 Darrow Road, Dept. IEN, Stow, Ohio

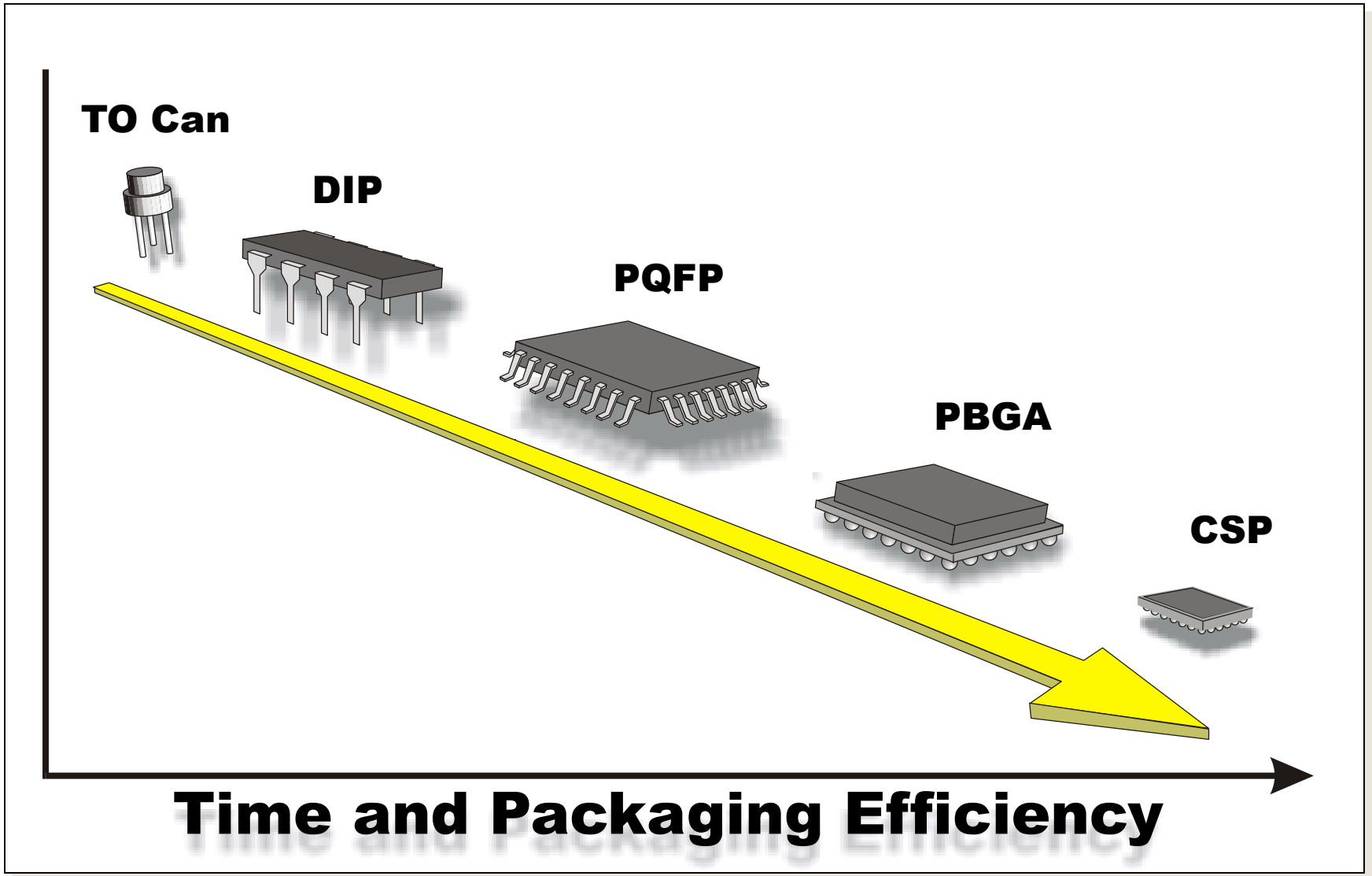
The invention of the transistor sparked the wholesale development of the PCB industry.

…before the integrated circuit printed circuits interconnected discrete transistors

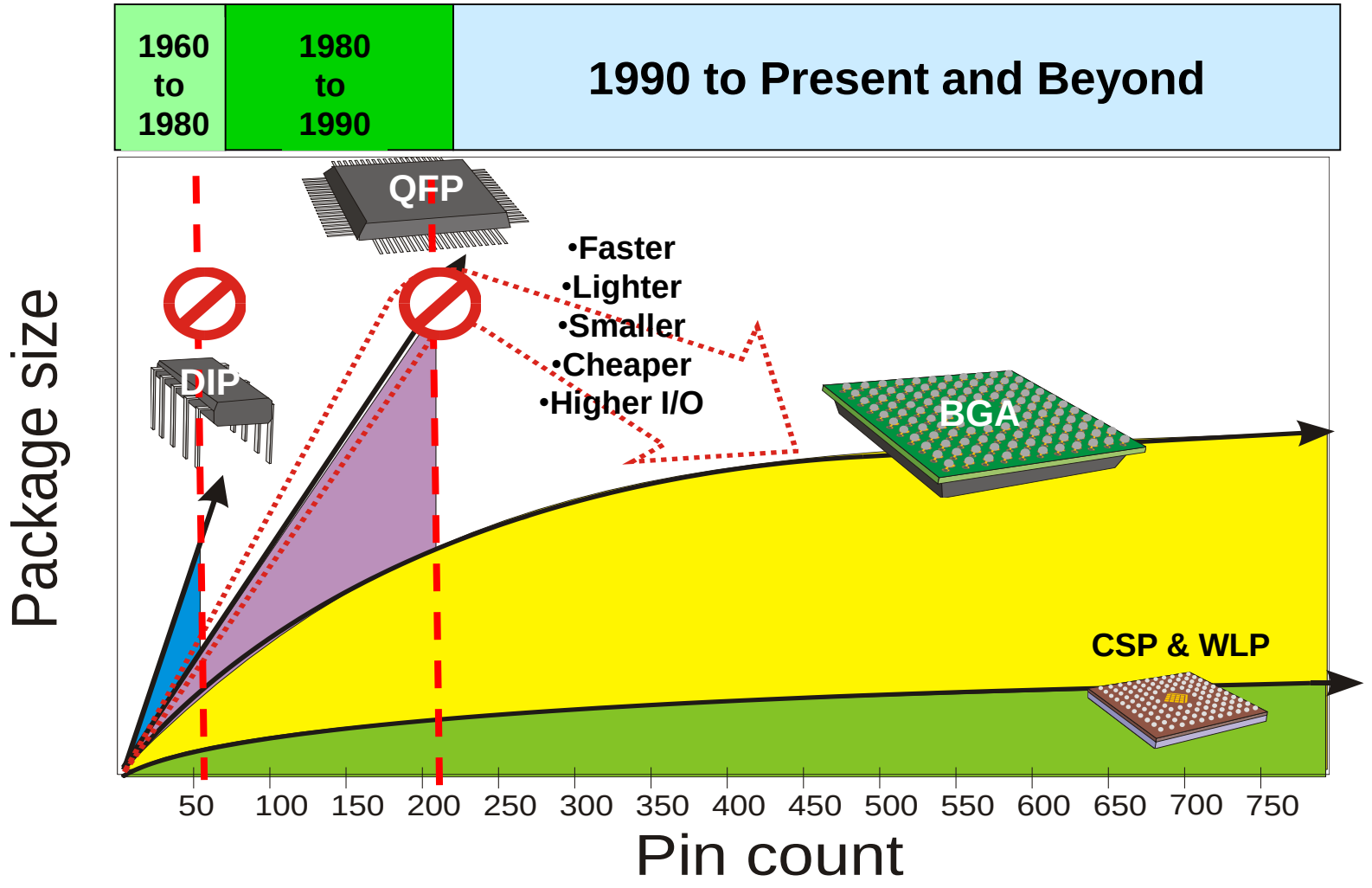


The First Transistor

Evolution of IC Packaging

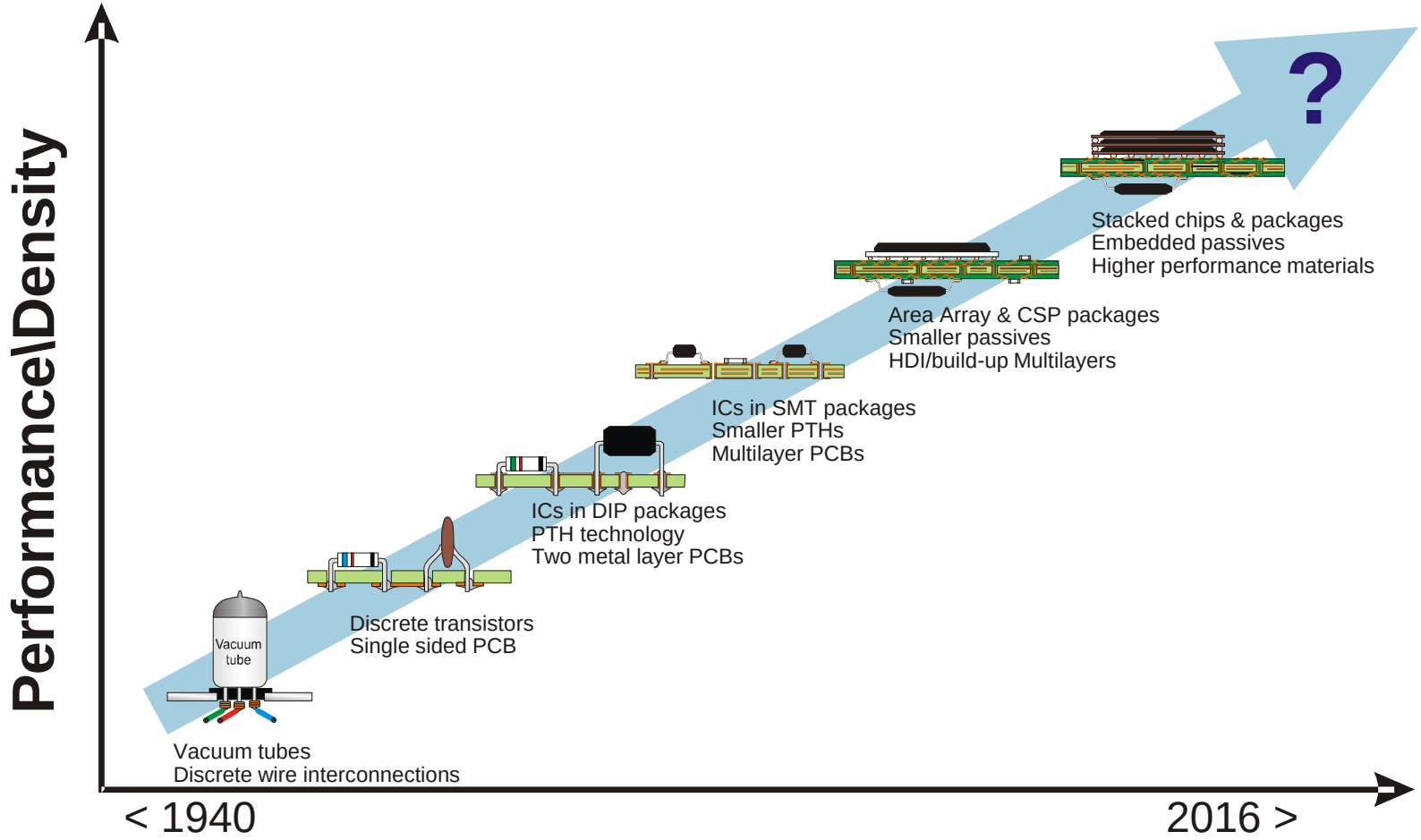


Packaging Responds to Market Trends



Individual comparing early 16 Kb vacuum tube memory module to 16Kb IC chip under the microscope

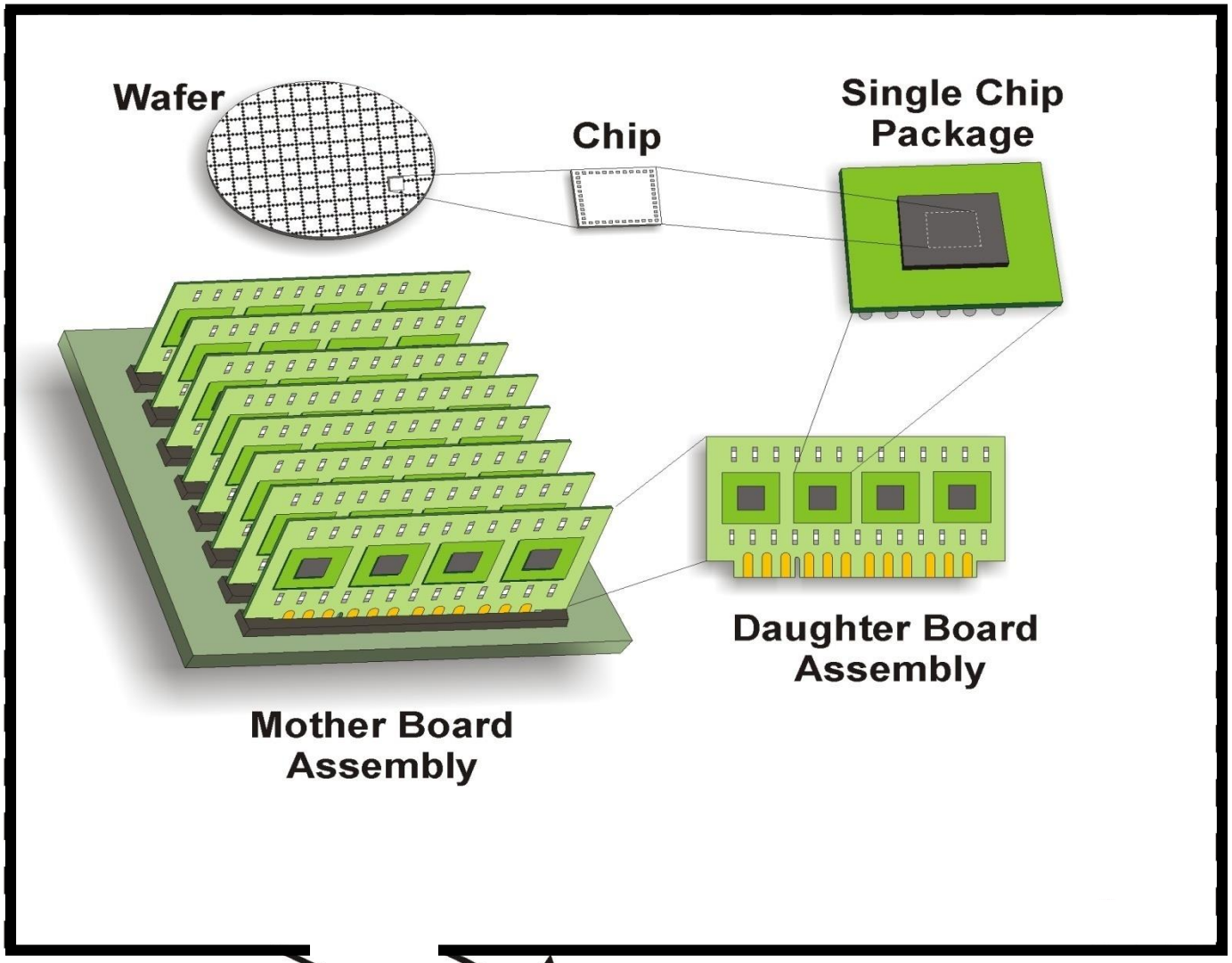
The Evolution of Electronic Assembly



The Industry's Terminology Challenge

- The electronics industry continues to explore and develop new methods to fabricate and interconnect its electrical and electronic devices.
- Establishing an understanding of how various elements fit together hierarchically is vital to extracting full benefit of technological progress in interconnection design architecture
- Trying to keep pace in classifying and incorporating the various approaches to new interconnection schemes is proving quite challenging (e.g. new 2.5 and 3D solutions)
- The commonly accepted approach to illustrating how the elements of the electronic interconnection fit is rooted in a hierarchy that was developed in the 1960 & 70s
- Unfortunately it no longer works for today's more complex approaches to the interconnection of electronic elements

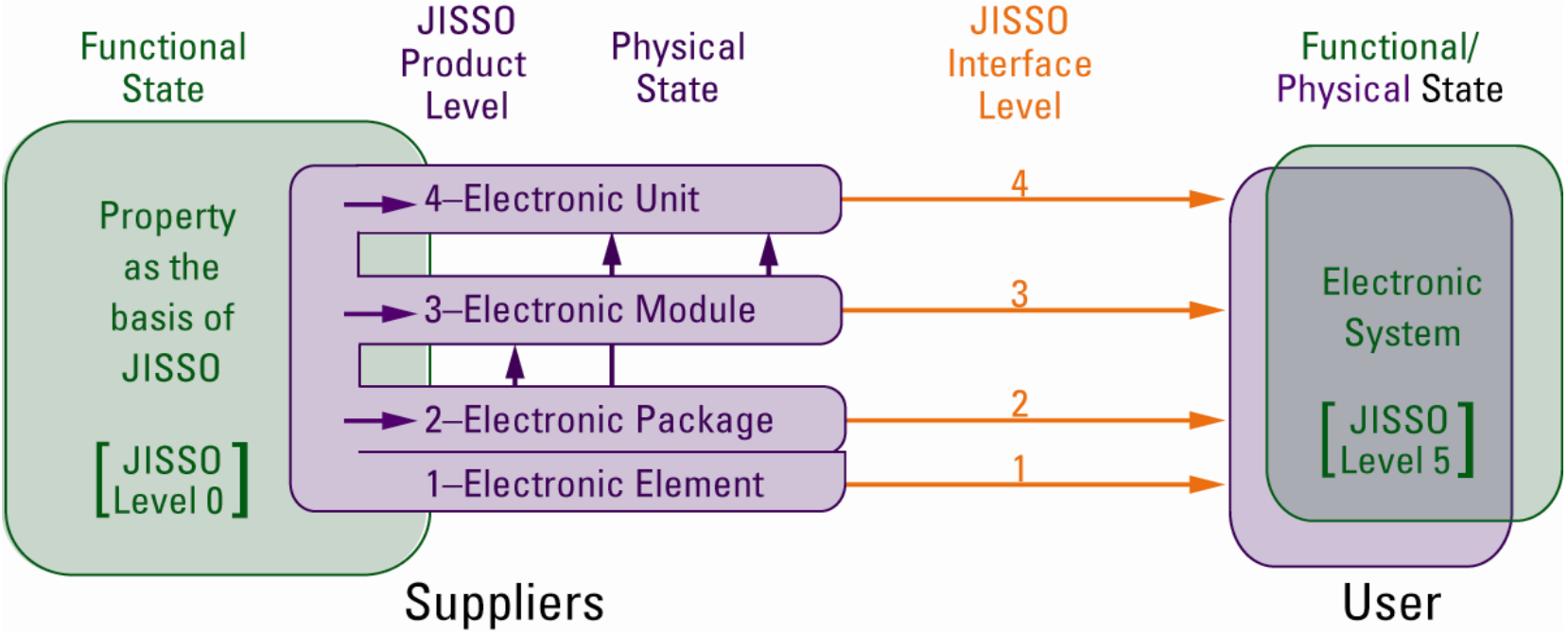
Traditional Hierarchy of Interconnections



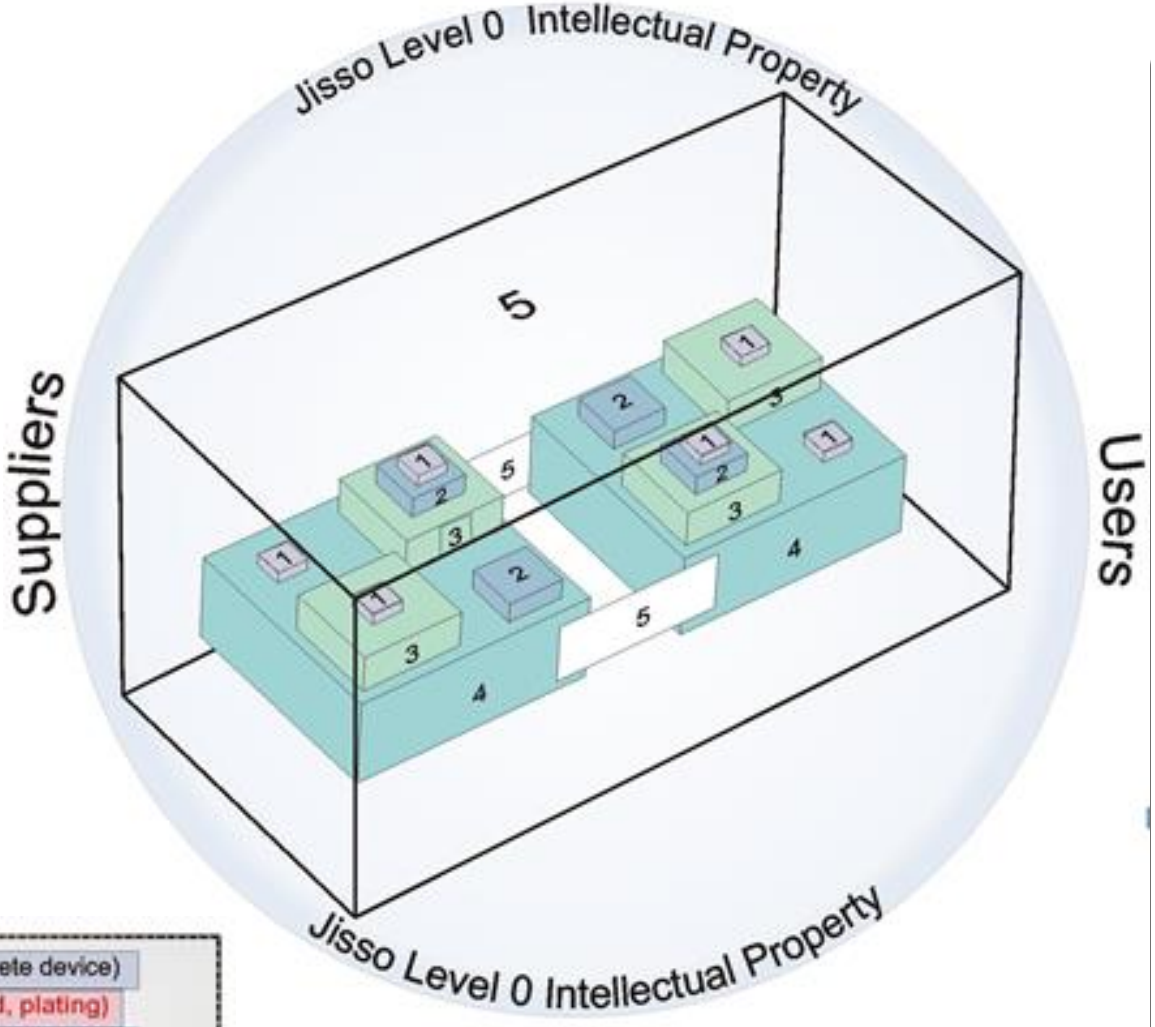
Jisso Interconnection Levels and The Evolving Hierarchy of Interconnections

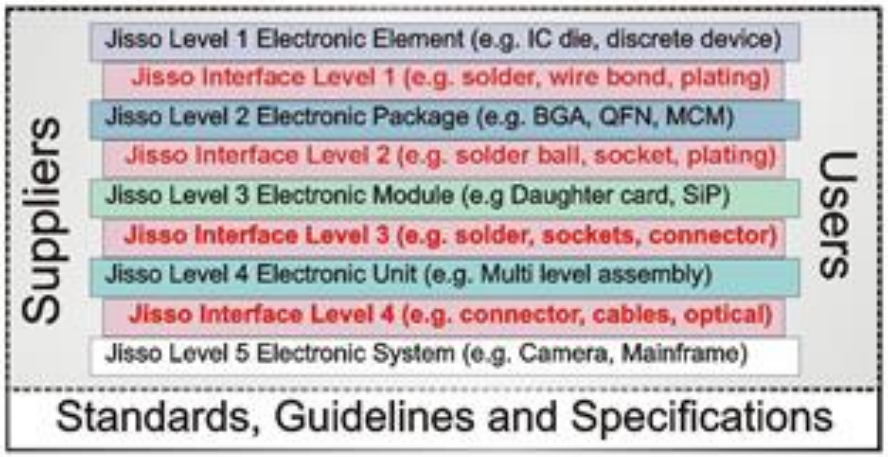
- Jisso is a Japanese term which is used to describe the electronic interconnection hierarchy in Japan
- Jisso levels are similar to traditional levels but there is also a Level 0 which covers intellectual property matters
- The objective of defining Jisso levels is to assist in the communication between electronic product suppliers and users by illustrating how electronic elements are hierarchically assembled and identify standards which facilitate communication process
- Unfortunately, gaps are being created by what might be viewed as "interconnection technology plate tectonics"

JISSO Level Concept

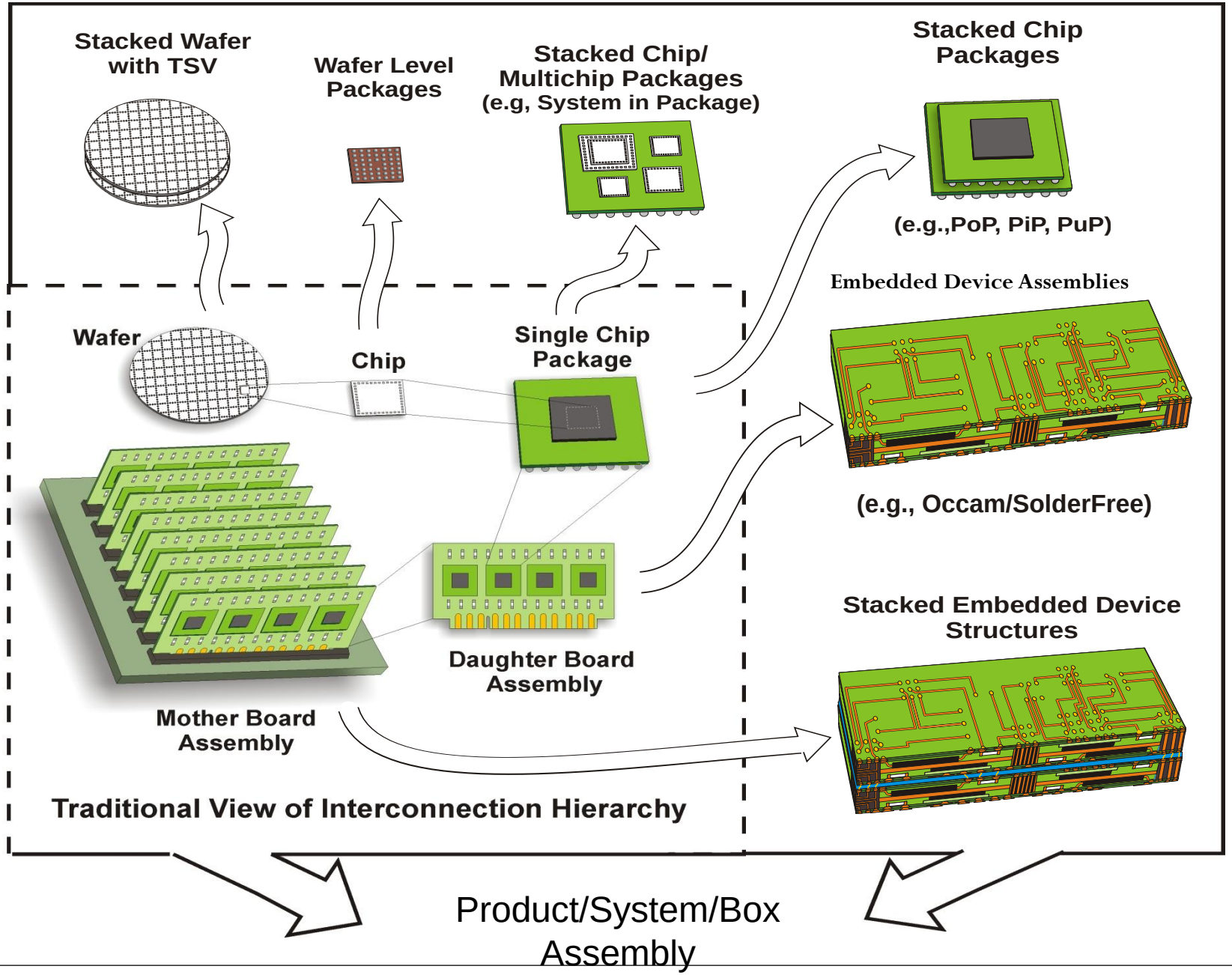


JISSO Level Concept… Alternate view



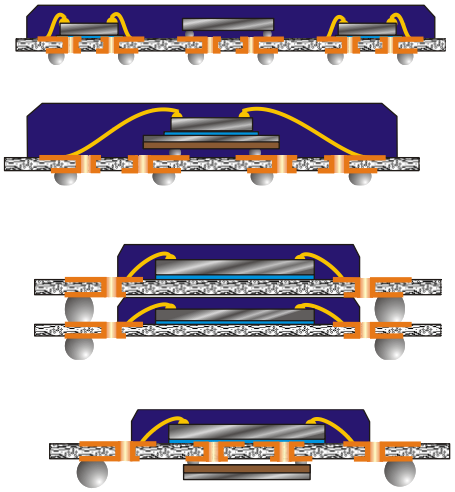


The Evolving Hierarchy of Interconnections



Evolving Technologies are Difficult to Neatly Categorize

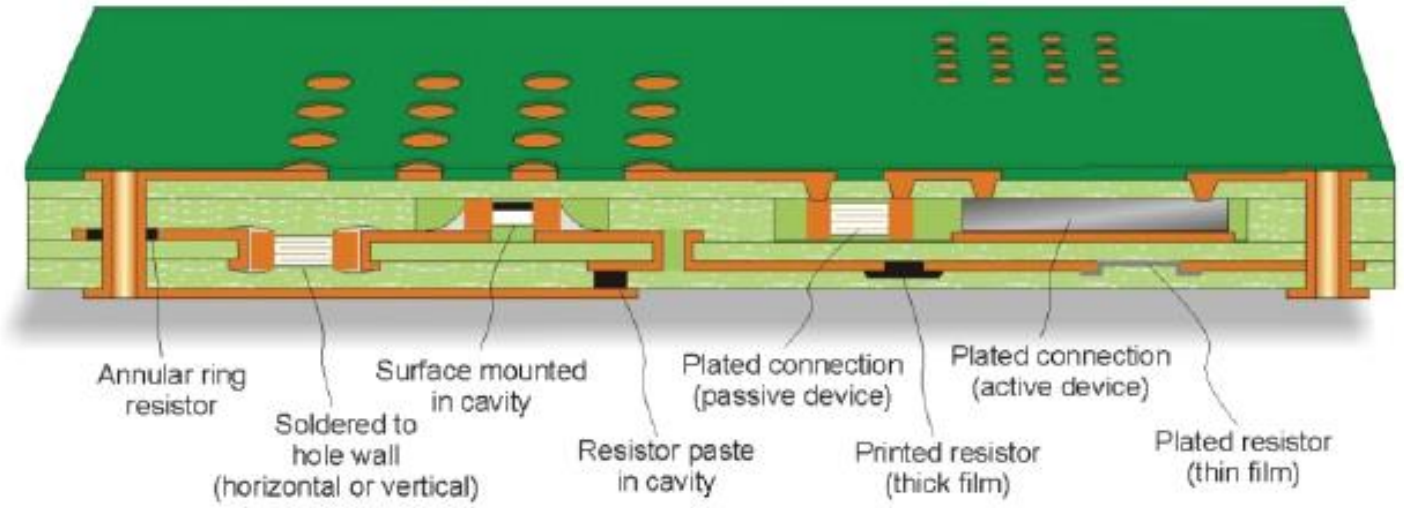
- Many different solutions are being introduced
- Wafer stacking, Chip Stacking, TSV
- Multichip Packages
  - System in Package (SiP)
  - Package in Package (PiP)
  - Package on Package (PoP)
  - Package under Package (PuP)



- Embedded device solutions

Numerous Embedded Device Approaches

- **Formed**
  - **Resistors**
    - Thin Film
      - Plated
      - Deposited
    - Thick Film
      - Carbon filled
      - Mixed fill
  - **Capacitors**
    - Clad Laminates
      - Unfilled
      - Filled
    - Thin Film
      - Ceramic Thick film
      - Ceramic Filled Photopolymer
    - Thick Film
      - Metal oxide pastes
      - Ceramic pastes
  - **Inductors**
    - Etched
    - Printed
- **Placed**
  - **Active Devices**
    - Bare die
      - Flip Chip
      - Wire Bond
      - Plated connection
    - Packages
      - Solder
      - Conductive adhesive
      - Plated connection
  - **Discrete devices**
    - Resistors
      - Solder
      - Conductive adhesive
      - Plated connection
    - Capacitors
      - Solder
      - Conductive adhesive
      - Plated connection
    - Inductors
      - Solder
      - Conductive adhesive
      - Plated connection



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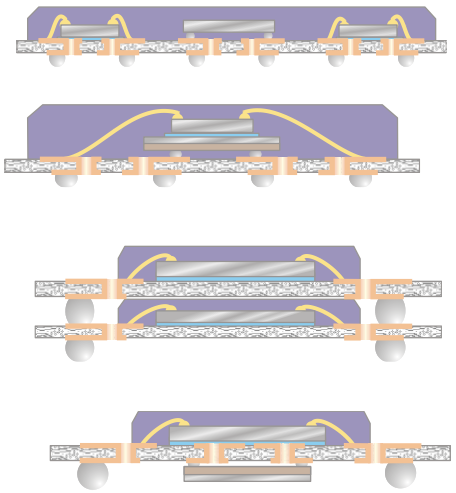
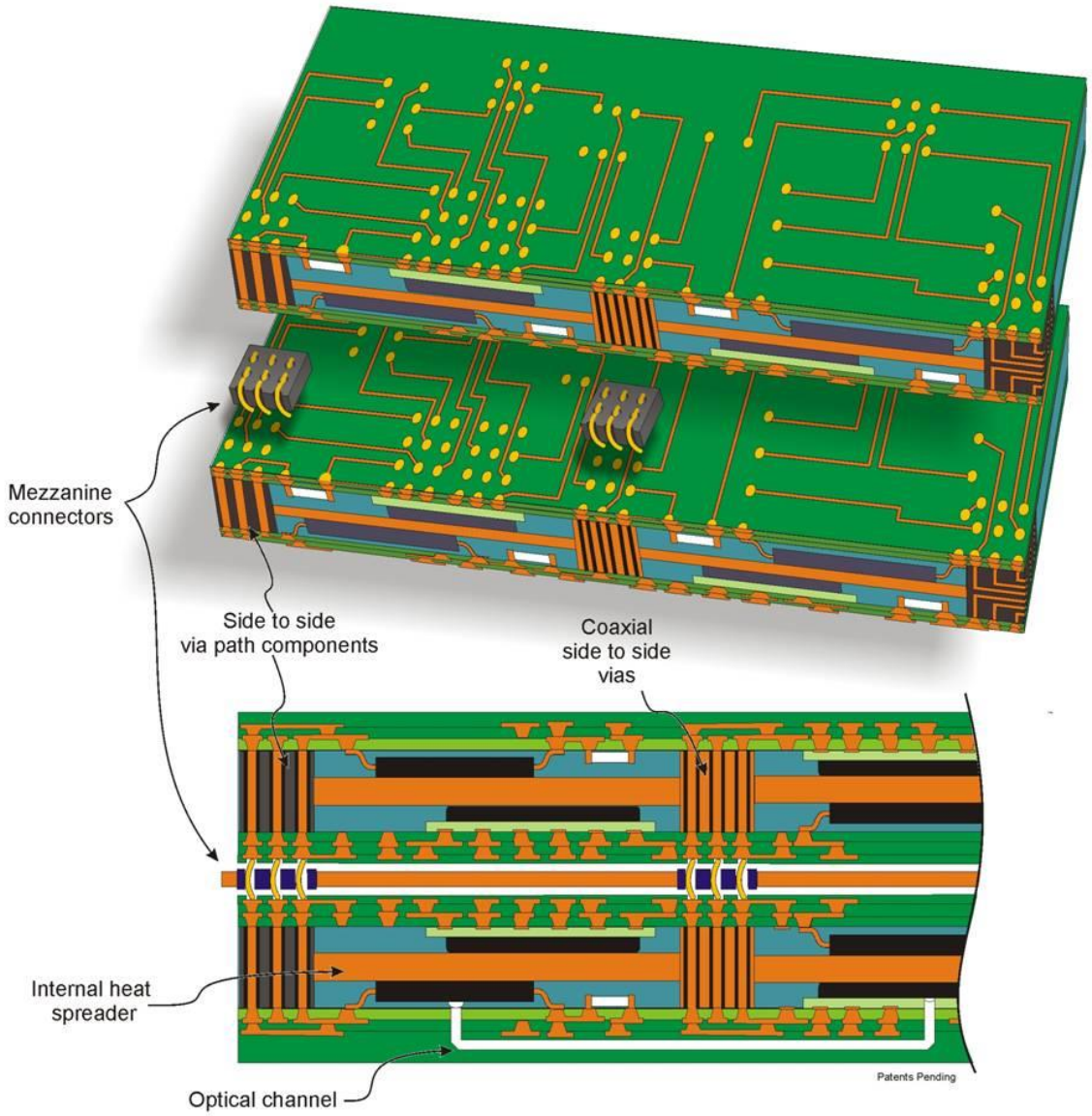
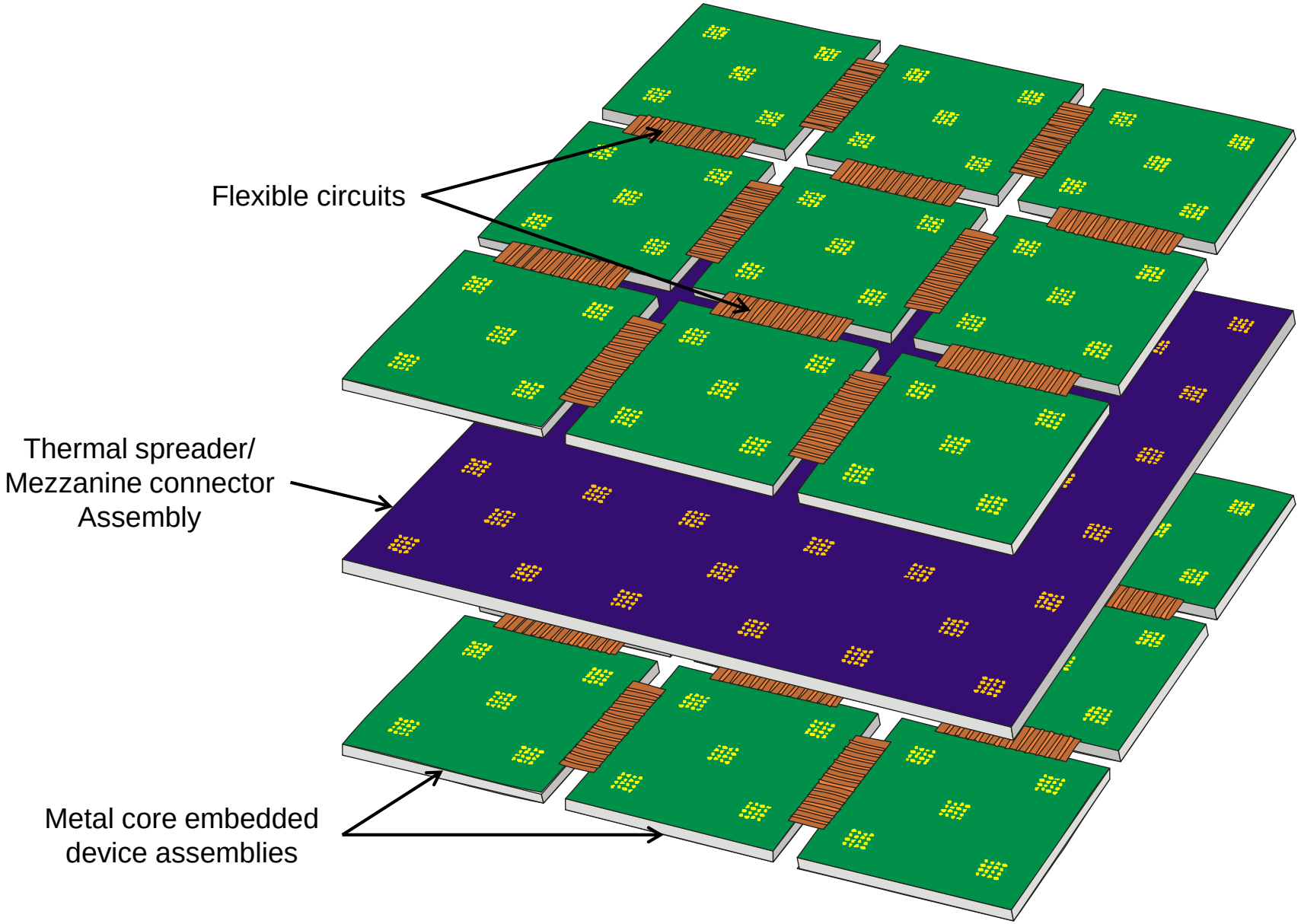


- Embedded device solutions
- Solder Alloy Free Electronics (SAFE)

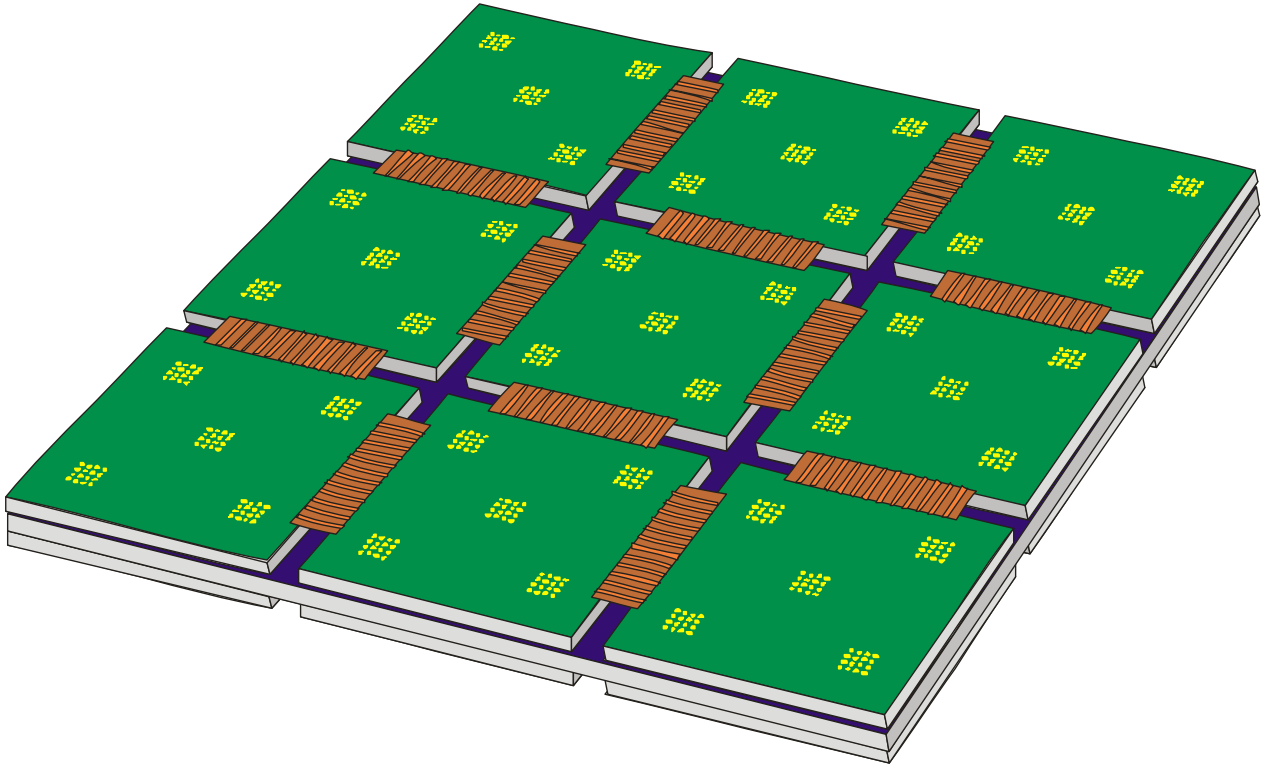
Solderless Assembly for Electronics (SAFE)



Yet To Be Defined Interconnection Structures



Multi-Module Assembly (MMA)?



Terminology Gap Challenge

Unfortunately traditional levels do not clearly define the various interconnection technology gaps and the differences they entail…

The question for the industry is: How might the electronics industry respond this ongoing challenge and capture the changes?

Possible Solution 1

Increase the number of defined levels?

- Level 1 **On chip interconnections (includes discrete devices)**
- Level 2 **Off chip interconnections (either side)**
- Level 3 **Chip to chip interconnections (any method)**
- Level 4 **Chip to package interconnections (any direction)**
- Level 5 **Package to package interconnections (any direction)**
- Level 6 **Embedded device structures (with or without solder)**
- Level 7 **Package to substrate interconnection (with solder)**
- Level 8 **Substrate to substrate interconnection (any direction)**
- Level 9 **System interconnections**

Possible Solution 2

Create intermediate levels?

- Level 1 **On chip interconnections (includes discrete devices)**
- Level 1a **Off chip interconnections (either side)**
- Level 1b **Chip to chip interconnections (any method)**
- Level 1c **Chip to package interconnections (any direction)**
- Level 2a **Package to package interconnections (any direction)**
- Level 2b **Embedded device structures (with or without solder)**
- Level 3a **Package to substrate interconnection (with solder)**
- Level 3b **Package to substrate interconnection (socket, connector)**
- Level 4 **Substrate to substrate interconnection (edge card, 2 piece)**
- Level 5 **System interconnections (cables, connectors)**

Summary

- **The realm of electronic interconnections is evolving rapidly and has evolved and is still evolving in some unpredictable and unforeseen ways.**
- **To assure reliable communication between package and system designers, developers and fabricators while simultaneously allowing them to access the latest technologies, there will be need to understand, adapt to and embrace the rapid pace of change occurring in the electronics packaging and interconnection industry.**
- **These new solutions offer great promise but do also require a good amount of understanding and discipline to implement and harness their benefit**
- **Good communications will be key to the success of all**