| Contestant name | | | | | |
|---|---|---|---|---|---|
| **Requirement** | **Description** | **Details** | **Grading** | **Max points** | **Given Score** |
| SCH-002 | New library | | | 1 | |
| | Name of new library | family_name | | 1 | |
| | U1,U2 | check terminal name(PDF or SCH) and numbering,check marking of inverting terminal (any marking is allowed) = 15p | -1p/terminal | 15 | |
| | LCD 1 | check terminal name and numbering,check marking of inverting terminal (any marking is allowed) = 5p | -1p/terminal | 5 | |
| SCH-003 | Corectness of schematic project | more or less ICs | -10p/IC | 50 | |
| | | more or less discrete components | -5p/comp. | | |
| | | more or less connections (except those caused by more or less components) | -5p/connection | | |
| | | wrong or missing values | -1p/value | | |
| | Schematic aspect | overlapped symbols/wires/labels, text direction, logic layout, sheet info | -1p/error, but zero for more than 5 errors | 8 | |
| PCB-002 | Double layer, clearance, width (1+1+1) | check settings if no routing, else check layers, clearance and width using DRC. | -1p/criterion | 3 | |
| PCB-003 | Vias 0.3/0.7 | check settings | zero for any error | 2 | |
| | LCD 1, SW1, SW2, SW3, SW4 (3p +3p+3p +3p+3p) | placed on top and fixed position | 3p +3p+3p +3p+3p | 15 | |
| | all components clearance from holes | placement avoiding 7mm radius(check placement, or settings if placement is | zero for any error | 4 | |
| | all components | All TH components on top, SMDs on bottom | zero for any error | 4 | |
| PCB-005 | footprints according to BOM | check with table 1, BOM | -1p for each category wrongly associated | 7 | |
| | U1/ LCD/Relay/SW/ Y1/Y2/C+ | pads: number, size, spacing (2+2+2) | 6p+6p+3p+2p+1p+1p+1p | 20 | |
| | | keepout, contour | 1p+1p+1p+1p+1p+1p+1p | 7 | |
| | U2 | SOIC-20 | 1p | 1 | |
| | TP | Check size (>0.9mm), clearance (>0.6mm to components, >0.3mm to board edge), status (check if is set as test-point) | -1p for each TP uncomplying with recommendations | 2 | |
| PCB-006 | 24V and return path | track width > 0.55 mm | 2p for each net | 4 | |
| PCB-007 | USBD+ and USBD- | differential (length, simmetry) | 5p+4p | 9 | |
| PCB-008 | USB1..USB8 | matching length same layer | 2p for each net (if all signals are routed) | 16 | |
| PCB-009 | Solder thief pads U2 | 2 pads near by pins 10 and 11. | 4p for each pad | 8 | |
| | U1 orientation | 45 deg. Orientation for LQFP | 2p if done in PCB | 2 | |
| PCB-010 | copper clearance, components clearance | min. 1mmSMT, SMB/min. 2mm to board outline. | 2p+2p for each criterion | 4 | |
| PCB-GEN | Placement into functional blocks | U1, U2, relays, inputs, outputs | 5p+5p+5p+5p+5p, -1 for any error | 25 | |

| | | | | | |
|---|---|---|---|---|---|
| | Symbol-to-footprint correspondence | Check polarized components: capacitors, diodes, MOSFETs connectors, and ICs | 2p+2p+2p+2p+2p, zero on each criterion for any error | 10 | |
| | Decoupling placement | Check proximity to supply pins (as close as possible) | 4p for each capacitor | 8 | |
| | Connectors placement | Check edge placement and corresponding block proximity | 1p for each connector | 6 | |
| | Placement restrictions | Check for components overlapping, placement outside board | -2p for each error | 4 | |
| | Routing restrictions | No traces around mounting holes (7mm diameter) | 4p, zero on each criterion for any error | 4 | |
| | Partial/complete routing | | Partial = 1p, complete = 3p. | 3 | |
| MEC-001 | Board geometry | Length, width(<=dimension) | 2p +2p | 4 | |
| MEC-002 | Shape | Fit panel? | zero for any error | 4 | |
| MEC-003 | 4 holes | Check position, size, nonplating | 4p +1p +1p, zero for any error | 6 | |
| TST-001 | Test grid spacing | Check placement not settings (=2.54 mm) | -1 for any error | 8 | |
| TST-003 | Global fiducials | Check number (=3), layer(botom) (=copper),position (board corners), size (1.5mm-round), soldermask(>=3), shape=round | 1p + 1p + 1p +1p +1p +1p | 6 | |
| TST-004 | Local fiducials | Check presence, soldermask (any shape/size, center or corner position, same side as component). | 1p+1p for U1 and 1p+1p for U2 | 4 | |
| Only for complete routing or <= 5 nets unrouted | | | | | |
| FAB-001 | Gerber files | TOP, BOT, SMT, SMB, SST, SSB, DRD | 1p for each file (7 files) | 7 | |
| FAB-002 | NPT/PTH holes | | 4p for two files, zero for any error | 4 | |
| FAB-003 | PnP file | Check for PnP file, check centered insertion points | 1p + 1p | 2 | |
| FAB-004 | TST file | | 1p | 1 | |
| **TOTAL** | | | | **294** | |

| **Evaluation team** | Name | Signature |
|---|---|---|
| Evaluator 1 | | |
| Evaluator 2 | | |
| Student | **I agree with the evaluation of my subject and I accept my final score!** | |